INVITED PAPER

The Emergence of Silicon Photonics as a Flexible Technology Platform

This paper presents a brief history of the field of silicon photonics, encompassing a discussion of the key devices, with a focus on the key performance milestones that were instrumental in demonstrating the potential of silicon photonics.

By Xia Chen, Milan M. Milosevic, Stevan Stanković, Scott Reynolds, Thalía Domínguez Bucio, Ke Li, *Member IEEE*, David J. Thomson, Frederic Gardes, and Graham T. Reed

ABSTRACT | In this paper, we present a brief history of silicon photonics from the early research papers in the late 1980s and early 1990s, to the potentially revolutionary technology that exists today. Given that other papers in this special issue give detailed reviews of key aspects of the technology, this paper will concentrate on the key technological milestones that were crucial in demonstrating the capability of silicon photonics as both a successful technical platform, as well as indicating the potential for commercial success. The paper encompasses discussion of the key technology areas of passive devices, modulators, detectors, light sources, and system integration. In so doing, the paper will also serve as an introduction to the other papers within this special issue.

KEYWORDS | Optical modulator; photodetector; photonic integration; photonic packaging; silicon-on-insulator; silicon photonics

I. INTRODUCTION

Silicon photonics, originally expected to be a combination of the revolutionary optical communication networks and the enormous complementary metal–oxide–semiconductor (CMOS) industry, is becoming a major platform for much more than this, including optoelectronic integrated circuits (OEICs), nonlinear optics, and more recently, lidar, mid-infrared sensors and quantum photonics circuits. This is mainly because of its potential for high density of integration, low cost at large production volume, extremely large bandwidth and high speed data transmission offered by optical communications, its compatibility with CMOS processes, wide transmission window, and good nonlinear properties. Many challenges have been addressed with innovative ideas in the last few decades [1]–[9], which pave the way for the practical deployment of silicon-based optoelectronic devices and integrated photonic circuits in computing and communication systems.

The commercialization of silicon photonics, originally driven by potential applications in telecommunication networks and intrachip communications, is now driven predominantly, but not exclusively by the increasing demand for low-cost short-range optical interconnects in data centers and the computing industry. Many products are already available in the market and have been widely deployed in the field. For example, the 100G CWDM4 (coarse wavelength division multiplexing 4-lane) QSFP28 optical transceiver and the light peak technology by Intel [10], the 2 × 100G-PSM4 (parallel single mode fiber 4-lane) embedded optical transceiver by Luxtera [11], etc. There are also emerging activities in longer reach applications, notably the applications pioneered by Acacia [12], such as the recently released AC200-CFP2-LH module targeted for long-haul dense wavelength division multiplexing (DWDM) networks which can reach a distance of 2500 km.

Silicon offers many advantages over alternative material systems (InP, GaAs, lithium niobate, etc.). One major

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The authors are with the Optoelectronics Research Centre, University of Southampton, Highfield, Southampton SO17 1BJ, U.K. (e-mail: xia.chen@soton.ac.uk).

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advantage is the low cost that silicon photonics can potentially offer because it can be manufactured in large scale using the widely available CMOS foundries developed for the microelectronics industry. The huge investment in CMOS fabrication technology and the high quality of SOI wafers have meant that it offers higher yield than is possible with alternative material platforms. Another advantage is the high refractive index contrast between the silicon core and silicon dioxide cladding based on silicon-on-insulator (SOI) wafers, which enables submicrometer confinement of light and tight bending of optical waveguides, although multimicrometer platforms are also available, as pioneered by Bookham Technology, Kotura, and more recently, Rockley Photonics. High-density integration of photonic circuits on the SOI platform is thus feasible. Furthermore, silicon is a very versatile platform. It is possible to monolithically integrate not only optical components, but also electronic circuits and even microelectromechanical systems (MEMS) in the same platform at ultrahigh density [13], or in conveniently copackaged offerings, for example, using flip-chip techniques [14].

In this paper, we discuss the history of silicon photonics from the early research papers in the late 1980s and early 1990s, to the potentially revolutionary technology that exists today. The paper encompasses a brief discussion of the key technology areas of passive devices, modulators, detectors, light sources, and system integration, with a focus on the key technological milestones that were crucial in demonstrating the capability of silicon photonics.

II. WAVEGUIDE AND PASSIVE COMPONENTS

The origins of integrated optics date back to the 1960s and 1970s with the demonstration of the first 2-D waveguides on planar substrates and 3-D optical waveguides, which are the basic elements for guiding light in integrated circuits [15]–[24]. In the early years, there was a considerable research effort in ferroelectric materials such as lithium niobate ($LiNbO_3$) and III/V semiconductors such as indium phosphide (InP) and gallium arsenide (GaAs). $LiNbO_3$ was attractive because of its good electro–optic coefficient enabling optical modulation, and the ease of processing. Alternatively, InP and GaAs were interesting since they offer a good prospect of optical amplification, laser development, and electronic integration. However, while being successful for long-haul applications, these platforms were less suited to mass markets due to associated fabrication costs. In the mid-1980s, Soref *et al.* [25]–[28] proposed silicon as a material platform for integrated photonics. The authors stated: "Silicon is a 'new' material in the context of integrated optics even though Si is the most thoroughly studied semiconductor in the world." Subsequently, single-crystal silicon waveguides [25], [26] were soon demonstrated, initially fabricated using highly doped silicon substrates. Various substrate configurations, such as silicon-on-sapphire (SOS) [29], silicon germanium [30], and SOI [9], [31], [32] were also studied. The SOI platform among them, first reported for optical applications in 1988 [31], has by far, become the most popular among the silicon-based waveguide systems.

In the late 1980s and early 1990s, Separation by IMplantated OXygen (SIMOX) and Bond and the Etch-back SOI (BESOI) techniques were the two main methods for SOI wafer fabrication [22], [33]–[39]. Initially, very large propagation losses (~30 dB/cm) from a 2-μm-thick planar waveguide [37] were demonstrated in these wafers. Rapidly, Rickman *et al.* improved propagation losses to respectable levels by investigating the influence of buried oxide thickness (BOX). The results showed that a BOX layer thickness of greater than 0.4 μm was necessary to prevent substrate leakage losses for a silicon layer of several microns. Around 1989, Kurdi *et al.* [31] and Davis *et al.* [33] reduced propagation losses to acceptable levels achieving 4 and 1 dB/cm, respectively. Multiple-layer waveguiding structures using SIMOX fabrication technology were also demonstrated [22], [32], [35]. During the1990s, most of the attention was turned to rib waveguides, structures that could confine light in both dimensions. In the early days, the majority of the work was conducted on relatively large waveguides, of the order of several micrometers in cross-sectional dimensions. Silicon waveguides with propagation loss $<$0.5 dB/cm were demonstrated in 1991 [40]. By 1994, Reed's group at the University of Surrey had achieved an even lower loss value, for both transverse electric (TE) and transverse magnetic (TM) mode at a wavelength of 1.532 μm [41]. These papers demonstrated that silicon was not only a viable waveguiding material, but that the propagation loss was not going to be a serious issue in the development of the technology.

Desirable properties of an optical waveguide are single-mode propagation, polarization independence, and low propagation loss. Significant research effort was dedicated in these areas [42]–[46]. In early 1991, Soref *et al.* [42] were the first to propose a simple expression for the single-mode condition of an SOI rib waveguide. Several years later, Chan *et al.* [47] derived equations to predict single-mode and polarization independence for relatively small rib waveguides. It was found that the quasi-TM single mode boundary is more restrictive than quasi-TE, and hence provides guidance on the geometrical limitations to retain single-mode behavior. In the following years, this was studied by several groups [48]–[52], taking into account the influence of the upper oxide cladding on single-mode and polarization dependence of rib waveguides. The authors defined more rigorous equations for both near and mid-infrared silicon photonics that started to appear in the literature around 2008.

During the 2000s, submicrometer rib, strip, and photonic crystal waveguides were fabricated on 220-, 340-, and 400-nm SOI platforms. Typical losses for rib waveguides with large cross section (1–3 μm^2) at the operating wavelength of 1.55 μm were 0.2 dB/cm [53]. Strip

waveguides with small cross-sectional area (~0.11 μm^2) exhibited significantly higher losses (1–2 dB/cm) and losses increased exponentially when the waveguide width was decreased [54]–[63]. Photonic crystal waveguides on SOI were demonstrated in 2000 [64], [65], guiding the light in a line of defects in the 2-D photonic crystal, which offer many additional functionalities. Around the early 2010s, in order to reduce the propagation losses further, small cross-sectional etchless/LOCal Oxidation on Silicon (LOCOS) ridge waveguides were investigated and small losses for the TE mode, of only 0.3 dB/cm, were demonstrated [53]. Despite the low losses, these waveguide did not become mainstream due to complications in other performance parameters such as bending loss. Since the early demonstration of a silicon wire waveguide with a subwavelength grating (SWG) metamaterial core in 2006 [66], metamaterial SWG waveguides have attracted strong interest in academia and industry. Many advanced silicon photonics devices with unprecedented performance have been demonstrated [67], [68] with minimum feature size greater than 100 nm, compatible with deep-up lithography.

Currently, the light scattering at waveguide' sidewalls still represents the dominant cause of optical loss in conventional waveguides in the SOI platform. Device fabrication technology (i.e., immersion lithography) and postfabrication treatments such as reoxidation of the waveguides are continually improving. 200-mm silicon photonics manufacturing is transitioning toward 300-mm wafers due to growing demand for a variety of applications by academic and industrial sectors. Recently, a small submicrometer 457 × 220 nm^2 strip waveguides, fabricated using 45-nm mask technology and 193-nm immersion lithography on 300-mm SOI platform, demonstrated very low losses of 0.7 dB/cm for the TE mode [69]. The TM mode losses are still two to four times higher, while rib waveguides fabricated by the same technology experienced much lower losses (~0.1 dB/cm for 700 × 220 nm^2, 70-nm-thick silicon slab layer) [69]. These results represent the current state of the art and are expected to improve even more in the future as new designs and improved fabrication technologies emerge.

SOI has undoubtedly been the leading material platform for passive devices. It has allowed the implementation of passive components with outstanding performance including waveguides, splitters [70]–[72], interferometers [73], resonators [74], [75], (de)multiplexers [76], polarization management devices [77], grating couplers [78]–[92], etc. However, their functionality is limited to spectral wavelengths in which both silicon and silicon dioxide are transparent (1.1–3.8 μm) [93]. Also, the high thermo–optic coefficient of the Si core makes them strongly sensitive to temperature variations, while the presence of two-photon absorption (TPA) and induced free-carrier absorption makes them potentially inefficient for nonlinear applications [94], [95] or other high power density applications. However, it is possible to achieve temperature-independent operation [96] or limit the free-carrier absorption induced by TPA [97], [98] with more sophisticated waveguide designs. Nevertheless, there is an increasing interest in exploring alternate materials with relatively high index contrast that will extend the operation range and applications of passive photonic devices.

Some of the CMOS-compatible materials that have been considered for the near-infrared and the visible wavelength regime include polycrystalline silicon [99], [100], amorphous silicon [101]–[103], doped silicon dioxide [104], silicon oxynitride [105], [106], and silicon nitride (SiN) [107], [108]. Among them, SiN has drawn attention for a variety of photonic devices. Its key properties are a wide transparency window covering the visible to the mid-infrared (MIR), low nonlinear losses, a relatively low thermo–optic coefficient, and an easily tunable composition. These features make it an ideal candidate to complement the SOI platform. Devices fabricated on SiN have shown high insensitivity to temperature variations while achieving propagation losses below 2 dB/cm in the MIR and well below 1 dB/cm in the visible and telecom wavelength ranges [108]–[111]. Furthermore, SiN with a high silicon content has demonstrated the potential for fabrication of devices with enhanced nonlinear response and low nonlinear losses such as photonic crystal waveguides and cavities [112], [113].

Other material platforms investigated in recent years to extend the operational wavelength range of passive silicon photonics devices to the MIR include silicon-on-sapphire [114], silicon-on-porous silicon [115], suspended silicon [116]–[120], silicon-germanium-on-silicon [121], and germanium-on-silicon [93]. All these platforms have improved performance within transparency windows in the 2–16-μm wavelength range. These platforms exhibit complementary characteristics related to their cost, fabrication complexity, and device footprint that makes them dominant for different wavelength regions of the MIR.

III. MODULATORS

Silicon does not exhibit a Pockels electro–optic effect as used in modulators formed in more traditional photonic materials. However, optical modulation in silicon photonics can be achieved through different means. The majority of the earliest demonstrations and probably still the most popular today use the free carrier plasma dispersion effect in silicon. This effect was characterized into useful practical equations for near-infrared wavelengths by Soref and Bennett in the 1980s [122] and extended out into the MIR by Nedeljkovic *et al.* in 2011 [123]. As the name suggests, this approach involves modifying the density of free carriers present in the material through which the light propagates, causing a modulation of real and imaginary parts of the refractive index.

This modification can be induced optically, the so-called light by light modulation approach for example [124]. More commonly electrical diode like structures are implemented in and/or around the waveguide structure where

the electron and hole densities in the waveguide can be controlled electrically. Early modulators of this type used free carrier injection structures which consist of a pin diode formed across the waveguide. Early demonstrations were limited to speeds in the megahertz range [125] but improvements in performance achieved over time were made by scaling down device dimensions and design optimization with the first proposed gigahertz modulator design published by Png *et al.* in 2004 [126]. Carrier injection devices are efficient enough to permit device lengths on the order of hundreds of micrometers and are simple to fabricate using standard CMOS techniques, but their main limitation is the operation speed with the fastest demonstrations on the order of a gigahertz [127] (although faster may be achieved through a preemphasis drive technique as first proposed by Png *et al.* [126], and later implemented by Lipson *et al.* in a ring resonator format [127]).

In order push to higher device speeds, other electrical structures have been proposed and demonstrated. The first demonstrated gigahertz modulator was reported in 2004 [128] and employed the carrier accumulation structure (or MOSCAP as it is also known). In such a device, free carriers are accumulated on either side of a thin insulating layer positioned within the waveguide. This type of device provides reasonable efficiency together with high-speed operation, the issue being that it requires a more complex fabrication process than either carrier injection or depletion structures (see below in the following paragraph). A particular challenge is the introduction of the thin insulating layer within the waveguide while having silicon with good optical and electrical properties on either side.

In 2005, Gardes *et al.* proposed the first waveguide-based carrier depletion device predicting speeds into the tens of gigahertz [129]. In this type of device, free carriers are depleted from a pn junction which is positioned so that the depletion width interacts with the light propagating in the waveguide. Such a device requires a simpler fabrication process as compared to the accumulation modulator and provides high-speed operation, but its efficiency is low, meaning that device lengths are typically on the order of millimeters. Intel was the first to demonstrate modulation at 40 Gb/s from a depletion device in 2007 albeit with a 1-dB extinction ratio [130]. In 2011, Thomson *et al.* then demonstrated 40-Gb/s modulation with a 10-dB extinction ratio [131]. In the same year, Gardes *et al.* showed that 40-Gb/s modulation could be achieved with a 6.5-dB extinction ratio for both TE and TM polarizations [132]. In 2012, Thomson *et al.* showed 50-Gb/s modulation with a 3-dB extinction ration from a silicon depletion modulator for the first time [133]. In recent years, modulation rates up to 60 Gb/s [134], [135], 70 Gb/s [136], and 90 Gb/s [137] have been reported.

In recent years, there have been numerous demonstrations of carrier depletion devices with optimizations of different performance metrics. They remain the most popular techniques in silicon photonics and the one used in silicon photonics multiproject wafer (MPW) services worldwide.

As mentioned above, the free carrier effect changes both the real and imaginary parts of the refractive index, however devices are more effective when implemented as a phase modulator (at least in the near infrared). Intensity modulation is then achieved using an optical interference or resonance structure to translate from the phase modulation produced. The Mach–Zehnder modulator (MZM) is the most commonly used interference-based structure providing good thermal stability and a wide operating wavelength range as a modulator. The ring resonator (RR) is the most commonly used resonant structure, and can provide a much more compact and lower drive power solution than the MZM. However, it is highly sensitive to temperature, fabrication tolerances, and has a narrow operating wavelength range, which means that a tuning/stabilization technique is required for practical use. Slow light structures provide another means for reducing the power consumption and/or foot print of the phase modulator, but again at the cost of reduced optical bandwidth and increased fabrication and temperature sensitivity [138].

Other mechanisms to achieve modulation in an "all silicon" regime are through the use of the thermo–optic effect [139] and MEMS-based structures [140], however these are mostly limited to lower speed applications. Another interesting technique has been the use of stress to invoke the Pockels effect in silicon, although to date rather large drive voltages are still required [141], [142].

The introduction of other materials onto the silicon photonics platform provides another means to achieve high-performance modulation in silicon. For example, the use of III/Vs [143], graphene [144], EO polymers [145], $LiNbO_3$ [146], and SiGe [147], [148] have been demonstrated. The use of SiGe, to form both quantum confined stark effect (QCSE) [149] and Franz–Keldysh (FK) [147] effect modulators is particular attractive since it retains CMOS compatibly.

In recent years, focus has moved away somewhat from developing the speed of the modulator, and looking at modulation formats which can fit more data into a modulator with a fixed bandwidth. Popular techniques have included pulse amplitude modulation (PAM) [150], quadrature phase-shift keying (QPSK) [151], quadrature amplitude modulation (QAM) [152] and discrete multitone (DMT) [153]. Concentration has also shifted heavily toward the power consumption of the modulator and design which can be operated with low drive voltages.

IV. PHOTODETECTORS

Photodetectors are one of the key components of optical links in integrated circuits as they convert light into electricity. Over the last 30 years, a tremendous amount of work has been focused on pushing the capabilities of detector materials and their integration to associated devices. The particular emphasis of the development has been on high-speed, large-bandwidth, and low-noise char-

acteristics to target the telecommunication market in the O optical band (1260–1360 nm) and the C optical band (1530–1565 nm). A variety of material systems currently exist, where specific structures are targeting an optimum integration with traditional CMOS driving circuitry. The "standard" semiconductor materials currently competing for large-scale, low-cost "CMOS" integration are group IV materials silicon (Si), tin (Sn) germanium (Ge), or more complex compounds for extended wavelength detection such as InGaAs and HgCdTe. Moreover, less conventional 2-D materials have also created a lot of interest recently such as graphene, carbon nanotubes, or MoS_2. Currently, the majority of the work is focused on data transmission in the 1300–1550-nm wavelength range, corresponding to the historical window of minimum optical loss for silica optical fibers. Nevertheless more work is being undertaken to expand the capability of detection and to cover a wide spectrum range going from visible to mid-infrared. The established trend for ideal photodetectors is to optimize features or at least obtain the best tradeoff in metrics such as: high responsivity or sensitivity, high detection speed, large bandwidth, high quantum efficiency (QE), low dark current, and low applied voltage bias.

Group IV materials such as Si, Sn, or more particularly Ge are the most commonly integrated photodetection material on the CMOS platforms. For Ge, liquid phase epitaxy [154], [155] and a two-step epitaxial growth technique has been developed to directly grow Ge on Si to alleviate the issues linked to the lattice mismatch and enable to obtain dislocation density of $\sim 10^6$–10^7 cm^{-2} [156], [157]. Coupling the Ge photodiode to a waveguide through edge coupling or evanescent coupling led to responsivity larger than 1 A/W [158], [159], with bandwidth beyond 30 GHz [159], [160], and dark current as low as 0.2 nA [161]. Recently, with the help of GeSn active layers, high-performance Ge $p-i-n$ photodiodes (PDs) have been fabricated to extend the photodetection to the longer wavelengths up to 1800 nm and beyond [162], [163]. Ge-on-Si avalanche PDs are also of great interest as they combine the optical absorption of the Ge layer with the carrier-multiplication properties of Si [164], [165]. In the case of Si, the relatively large indirect bandgap corresponds to a cutoff wavelength below 1100 nm [166], which makes the material mostly suitable for visible light and infrared detection. Nevertheless, a substantial amount of work on the material engineering aspect has provided mechanisms to perform detection at near-infrared through methods such as mid-bandgap absorption (MBA) [167], [168], surface-state absorption (SSA) [169], internal photon emission (IPE) [170], and TPA [171]. MBA PDs are developed based on the fact that high energy particles could introduce defect states located within the bandgap of the intrinsic Si crystal, thus enabling detection of sub-bandgap optical radiation. SSA PDs are based on a similar principle as MBA PDs, but in this case, surface states are introduced into the bandgap of the intrinsic Si, providing a path to optical absorption at longer wavelengths. IPE PDs rely on the principle that photo-excited electrons in metal can gain energy higher than the Schottky barrier and subsequently move into the conduction band of the semiconductor. TPA PDs are based on the nonlinear TPA process where an electron can absorb two photons (having individual energies below the semiconductor bandgap) approximately at the same time, and reach the excited state in the conduction band.

$In_xGa_{1-x}As$ alloys are currently the most mature material system for photodetection due to the alloy variable bandgap where the absorption edge wavelength can be varied between 0.85 and 3.6 μm, making it ideal for near-infrared photodetection [172]. Nevertheless flip-chip integration is currently the most common process used to integrate the III/V layers with the SOI substrate [173]–[177] with recent efforts focused on extending the capability of InGaAs APDs for error-free, high-speed modern communication ($\sim$50 Gb/s) as well as single photon detection systems [178]. The flip chip technique is nonideal as the integration process must be carried out through dice bonding at wafer level, a process that is time consuming and therefore expensive. An alternative solution to bonding could be a new heterogeneous integration approach using a metal-organic chemical vapor deposition (CVD) technology. The epitaxy of a $In_xGa_{1-x}As$ absorption layer is showing the promise of selectively grown III/V on Si substrate [179].

In terms of material properties, HgCdTe is probably the most promising semiconductor to cover infrared to mid-infrared photodetection with a detection spectrum between 0.7 and 25 μm. APDs for photodetection at 1060, 1300, and 1550 nm have all been fabricated using liquid phase epitaxy or molecular beam epitaxy [180]–[182]. Nevertheless, integration to CMOS circuitry is more problematic as high-quality HgCdTe is usually grown on CdZnTe substrate, which is a difficult material to integrate with the silicon readout circuit due to different thermal expansion coefficients and a 19% lattice mismatch [183], [184]. The fabrication cost associated with the CdZnTe substrate is also much higher than Si and Ge.

Different from bulk materials, low-dimensional materials provide some unique properties when used as photodetectors. Interesting properties (such as exciton parameters), which are often negligible in bulk materials, are greatly accentuated in low-dimensional materials. These unique electronic and optical properties make photodetection promising even in an extremely small nanostructure that is only one atomic-layer thick (graphene or MoS_2) [185] or just a few nanometers (carbon nanotube) [186].

V. INTEGRATED LIGHT SOURCES

Light sources are essential components in photonic integrated circuits (PICs). Silicon, however, is a very inefficient light emitter due to its indirect bandgap. Therefore, making an efficient light source in silicon photonics has

proved to be one of the most challenging tasks for many years. Lack of such sources has prevented this technology showing its full potential. Although using an external, off-chip light source (optically coupled to a silicon PIC) is an acceptable approach in some applications, development of low power consumption on-chip light sources for silicon photonics is desirable for optical interconnects that are targeting datacom applications where both low power consumption and high bit rates are needed.

Although lasing in bulk silicon was achieved in 2004 via stimulated Raman scattering and optical pumping [187], this approach offers neither high-level integration nor the relatively high power efficiency, needed for optical interconnects [188]. Some research effort has been directed to modifying silicon in order to transform it into a light emitting material, such as introducing light-emitting centers in Si or SiO_2 substrates [189], [190], mostly based on rare-earth element doping [191]. Although, an optically pumped CMOS-compatible laser has been demonstrated using this approach [192], realization of electrically pumped devices remains very challenging.

Most of the research efforts in this field have been focused on integrating efficient light emitters (primarily based on III/V semiconductors) onto the SOI platform. Based on the integration techniques employed, we can distinguish three different approaches taken by researchers: 1) hybrid integration based on copackaging of III/V laser die and SOI PICs; 2) monolithic integration, based on various epitaxial growth techniques; and 3) heterogeneous integration, based on wafer bonding techniques.

The oldest approach taken was hybrid integration where a prefabricated optical source (laser or LED) is mounted and fixed on a common substrate and optically coupled to the PIC. The most common technique used for this is flip-chip bonding, based on a solder bump and attachment process [193]. This technique has been used for integration of vertical cavity surface emitting lasers (VCSEL) on CMOS circuits since the late 1990s [194]. However, integrating VCSELs emitting at telecommunication wavelengths (1310 and 1550 nm) with silicon PICs has proved to be challenging and progress has only recently been reported [195].

A more conventional approach involved integration of longitudinal cavity lasers based on InP and corresponding alloys. In 2010, Luxtera demonstrated a 40-Gb/s optoelectronic transceiver, based on a single III/V continuous-waveform (cw) laser enclosed in an optical micropackage (including a lens and isolator) that was flip-chipped onto the underlying silicon die and optically coupled to the photonic chip via grating couplers [196]. Further evolution of this device led to the demonstration of the first 100-Gb/s optical transceiver, where a micropackaged distributed feedback (DFB) laser was epoxy-bonded onto the chip [197].

Another approach based on copackaging was to form an external cavity laser by placing a III/V die, acting as a semiconductor optical amplifier (SOA), and optically coupling it to the silicon PIC that provided the wavelength-selective optical feedback. Following this approach, external cavity hybrid silicon lasers were demonstrated by Kotura [198], Fujitsu [199], and Oracle [200], [201].

Despite being relatively straightforward from the fabrication perspective, hybrid integration usually requires time-consuming and costly alignment schemes, and has obvious limitations when high-density integration is required.

Monolithic integration is based on epitaxial growth of high-quality layers of, mostly, III/V semiconductors on top of silicon or SOI substrates. The grown material is subsequently processed to form hybrid lasers, which are lithographically aligned to the underlying SOI PICs. This approach requires no active alignment and allows high-density integration and wafer-scale processing. However, there are many challenges in its practical implementation, primarily due to the lattice constant mismatch between most III/V materials and silicon, as well as the difference in thermal coefficients of expansions (TCEs). Several growth techniques were employed in this field. Researchers reported lasers based on GaSb grown on misoriented Si substrates, operating both in pulsed [202], [203] and continuous-wave regimes [204], as well as GaAs-based quantum dots (QDs) in a well laser, emitting at 1.3 μm [205]–[208]. Recently, reported InAs/GaAs QD lasers demonstrated record-low threshold current density and excellent aging test results [209]. Combined with less sensitivity of QD lasers to threading dislocations compared to standard quantum-well (QW) lasers, this approach is offering a promising way for fabrication of high-quality light sources on the silicon photonics platforms.

Certain efforts were focused on developing hybrid lasers in Ge-on-Si material systems, with the idea of growing a tensile-strained, n-type germanium on a silicon substrate in order to achieve a direct bandgap light emission [210]. Using this approach, both light-emitting diodes (LEDs) [211] and electrically pumped lasers [212] were demonstrated, but only in the pulsed regime and with a very high threshold current density.

Another promising approach in monolithic integration is based on direct growth of III/V nanowires on SOI platform forming a photonic crystal cavity [213], [214]. This approach does not require growth of any buffer layer and allows fabrication of small-footprint lasers with a high Q-factor.

However, a general drawback of monolithic integration is that growth temperatures are generally above 400 °C, which is not compatible for back-end-of-line (BEOL) processing in a CMOS foundry. Germanium–silicon–tin ($Ge_{1-x-y}Si_xSn_y$) has recently emerged as a promising material for low-temperature growth on silicon [215], [216], but further improvements are needed to achieve a direct bandgap in this material.

Heterogeneous integration based on bonding techniques is another promising technology for large-volume, wafer-scale fabrication of lasers in silicon photonics. This approach combines the best elements of hybrid and

monolithic integration by bonding high-quality III/V material (in the form of wafers or individual dies) onto SOI substrates. Subsequent processing of III/V material is carried out to form hybrid III/V/Si lasers. In this way, alignment between the III/V layers and the silicon waveguides is achieved via photolithography on a wafer scale, while the technologically challenging growth of III/V materials on a silicon substrate is avoided.

The most common wafer bonding technique used for this integration is plasma-assisted, low-temperature direct bonding. Adhesive bonding based on use of the thermosetting polymer divinylsiloxane–bisbenzocyclobutene (DVS–BCB) and various metal bonding techniques are also employed.

The first hybrid III/V/Si optically pumped laser based on direct bonding and evanescent coupling was reported in 2005 [217], followed by an electrically pumped Fabry–Perot (FP) laser in the following year [218]. Following this approach, researchers reported DFB [219], distributed Bragg reflector (DBR) [220], racetrack [221], and microring lasers [222], [223]. In 2010, using this technique, Intel demonstrated first four-channel silicon photonics link operating at 50 Gb/s [224]. Using DVS–BCB-based adhesive bonding and the same principle of evanescent coupling, both FB [225] and DFB lasers [226] were reported, followed by lasers with more advanced hybrid cavity designs and lower threshold currents [227], [228]. Also, microdisk hybrid III/V/Si lasers, with a very small footprint and large free spectral range, were demonstrated using both direct [229] and DVS–BCB bonding [230].

Metal bonding techniques have also been used for the fabrication of hybrid III/V/Si lasers [231], [232]. In 2013, Skorpios Technologies reported the first III/V/SOI hybrid laser fabricated in a commercial foundry, based on the metal bonding of a III/V die onto SOI [233].

In order to economically utilise relatively expensive III/V material, researchers have focused on development of multiple die-to-wafer bonding techniques. One of the most promising approaches in this type of bonding is transfer printing [234]. This technique was used to fabricate electrically pumped AlGaAs/AlInGaAs double QW FP lasers [235] and InGaAsP/InP-based VCSELs on SOI substrates [236].

VI. PACKAGING AND COUPLING

Fibers are the high-speed transmission lines that make up the backbone of most optical communication systems. When coupling to fibers from the PICs used by silicon photonics, loss is critical and must be minimized. Losses are the result of many mechanisms particularly from reflections when light transfers between media. Alignment to PIC waveguides is also critical, made particularly difficult by the size difference between fibers and typical submicrometer silicon photonic waveguides where the spot size produced by a standard telecommunications fiber is approximately 630 times larger. Coupling between these structures is comparable to aligning a basketball-sized pipe to a pea-sized tube, causing the majority of light to be lost. Larger waveguide platforms also exist without such a large mode size mismatch, such as those pioneered by Bookham Technology [237], the first Silicon Photonics company, Kotura [238] and more recently, Rockley Photonics [239]. For coupling to submicrometer waveguides, engineered structures on the fiber and waveguide will reduce losses; a lens at the fiber tip will focus the light to a smaller spot, significantly improving transmission, however, a smaller spot size makes the physical alignment of the fiber even more difficult, which normally requires a precision of a few hundred nanometers. Tapering of waveguides increases their surface area, however, with the scale of nanophotonic fabrication, structures as large as fibers are difficult to fabricate on-chip. Furthermore, vertical tapering on chip is difficult, and requires local thickening of the waveguiding structure. Consequently, many coupling setups use a combination of these methods to produce acceptable results.

Edge or butt coupling via a polished facet at the edge of a PIC is a common method for coupling, but the invention of grating couplers in the 1970s [240] allows the option to align a fiber near normal to the surface of the PIC. Grating couplers phase match the fiber mode to a waveguide mode, permitting optical coupling, whereas an unaltered surface would merely reflect or transmit the light. Many detailed modifications can improve coupling efficiency for both edge coupling [241]–[246] and grating coupling [78]–[92], but for mass market applications, cost is of crucial importance, which means that active alignment techniques applied to more traditional long haul photonics, are too costly for these applications..

Photonic packaging is the process of using the aforementioned coupling methods in a commercially viable way. Traditional optical telecommunications requires relatively low volumes, permitting high precision, active alignment that is high cost and time consuming. Recent trends in silicon photonics are pushing toward mass markets and therefore a high volume production environment, requiring automated, high-speed, cost-effective packaging processes.

The first demonstration of commercial silicon photonic packaging was in 2008 with the start of ePIXpack; using glass blocks for support, a fiber array was manually aligned to grating couplers and glued in place with epoxy [247]. This approach has been used a number of times since, improving on the concept [248], [249]. Passive alignment was first demonstrated by Galan *et al.*, who used v-grooves to align a fiber to an inverted taper. They demonstrated an added loss of 1.5 dB with a total insertion loss of 7.5 dB [250].

In 2012, Bernabe *et al.* published work using a v-groove capping chip which holds and positions fibers above a grating coupler, using a facet at the v-groove end to reflect light down to a grating coupler on the chip surface. With an added loss of 4 dB, this approach has the advantage of providing in-plane alignment that is semipassive, using computer vision for alignment [251]. Researchers at the

Tyndall Institute have developed a process using angled fibers positioned above grating couplers, where the angled facet is used to redirect the coupled light [252]. This actively aligned solution has a total coupling loss of 4.5 dB.

In 2015, significant improvements were achieved in coupling efficiency with work from Lindenmann *et al.* [253], [254]. They showed a coupling loss of 1.7 dB, using a novel method of 3-D writing waveguides in polymer much like a wire bond. In the same year, Barwicz *et al.* from IBM [255] produced a design similar to [250], utilizing v-grooves and optical mode converters. However, instead of typical inverted tapers, suspended subwavelength metamaterial mode converters [246] are used, which employ the subwavelength metamaterial mode converter demonstrated previously at NRC Canada [66], [243] and a suspended silicon dioxide layer [246] as additional mode guiding layer for an improved coupling efficiency. The IBM team demonstrated multichannel passive alignment with 1.3-dB insertion loss. Packaging has received very little research interest compared to most other disciplines within silicon photonics, even though the package will often contribute a large portion of PIC production cost. Regardless, packaging has shown a positive trend toward lower loss and reduced assembly time, which will only improve as industrial interest in silicon photonics continuous to grow.

VII. INTEGRATION

Integration of photonics and electronics is one of the key subjects for the development of silicon photonics. During 2006–2007, Luxtera [256], [257] successfully demonstrated the approach of monolithic optoelectronic integration, where multiple channels of an optoelectronic transceiver were implemented at 10 Gb/s per channel in a 0.13-μm CMOS SOI process. With the monolithic integration approach, the cofabrication of optical devices and CMOS transistors on the same silicon wafer provides versatile possibilities of new optoelectronic functions and dramatic improvement for system footprint and power dissipation. For example, in 2015, based on the 90-nm SOI process node, IBM introduced the CMOS9GW silicon photonic platform, and a 16-Gb/s full transceiver link has been demonstrated in [258]. Based on the same platform, the speed has been boosted to 56 Gb/s by using the four-level PAM approach [259]. Meanwhile, several designs based on the 45-nm SOI platform [260]–[262] have been reported, including the first single-chip processor that communicates directly using light [261]. In addition to this, IHP introduced the SiGe:C platform, which is based on the 0.25-μm BiCMOS technology, and a 13-dB extinction ratio 28-Gb/s nonreturn-to-zero (NRZ) transmitter was reported in 2016 [263].

In general, the monolithic integration approach enables the shortest possible electrical interconnects between optical and electrical devices, which hence minimizes otherwise unavoidable parasitic effects due to the packaging. However, the SOI substrate used in these silicon photonics platforms differs from the substrate used for standard CMOS technologies. Monolithic integration with photonics would require major process changes, which are not normally compatible with the time scale of technology evolution in electronics technology [264]. Currently, the most advanced monolithic silicon photonics platforms are based on a 45-nm SOI CMOS process, whereas the standard CMOS technology has evolved into the 10-nm node. Therefore, a two-wafer solution is usually desirable, which means the electrical design can fully utilize the high-speed and low-power consumption advantages from the state-of-the-art CMOS technologies, while the optical design can be realized with lower cost, more mature processing platforms. Furthermore, this approach means that large photonic devices do not consume expensive real estate in the most expensive CMOS platforms, and also enables electronic circuits to be upgraded to better CMOS platforms without necessarily abandoning the photonic designs in a tried and tested platform. Therefore, this approach is likely to continue in the short term, until a more flexible and cost-effective method of monolithic integration can be found.

The most traditional low-cost packaging solution to combine the electronics and photonics chips is the wire-bonding-based approach, which inevitably suffers from parasitic effect introduced by the bonding wires. Due to its simplicity and costs effectiveness, it is of the interest to many research groups to demonstrate initial concepts on the codesigning optoelectronic functions, but seriously limits the data rate for commercial devices. In contrast, flip-chip-based 3-D integration approach [14], [265]–[268] has become one of the alternative techniques, which can significantly reduce the parasitic effect introduced by the packing and increase the interconnection density. A representative example is the 10-Gb/s transceiver described in [14], in which the electronic design is realized with 40-nm CMOS and many 25-μm pitched microsolder bumps are deposited as interconnect between the optics and electronics. For more advanced integration, through silicon vias (TSVs) or through oxide vias (TOVs) [268] have been introduced into the silicon photonics integration in 2015, where an order of magnitude reduction in parasitic capacitance and two orders of magnitude higher interconnect density have been reported. Meanwhile, during 2015–2016, STMicroelectronics has introduced a design based on the fine pitch copper pillar interconnect while realizing the electronics in 65-nm CMOS or 55-nm BiCMOS technologies [264]–[266]. The reported maximum data rate was 56-Gb/s NRZ transmission with power consumption at 300 mW.

With increasing complexity, it has become clear that integration of photonics and electronics requires codesign between the optical and electrical functions. This means that neither the electrical devices nor the optical devices can be treated as a standalone component and indeed the realization of system functionality depends on the integration of these functions at the design stage. A simple example is the wavelength stabilization system design for a microresonator [269]–[271], where a

dedicated thermal control loop is designed to compensate for temperature drift and errors due to fabrication tolerances. The more advanced examples are segmented modulator and driver systems [262], [263], [272]–[275], where advanced modulation formats (such as PAM-4 and QAM-16) or optical signal shaping (such as feedforward equalization) become the system requirement. The trend of this electrical–optical codesigned system may significantly broaden the application area of silicon photonics as well as dramatically change the structure of existing optoelectronic transceivers.

VIII. POWER EFFICIENCY

The power efficiency of a silicon photonics transceiver is a critical and yet complex issue. It can be traded off with many other parameters, such as extinction ratio, optical loss, linearity, optical-signal-to-noise ratio (OSNR), and system stability. Generally, the power efficiency of an optical transceiver is calculated by dividing the power consumption with its maximum data rate, and expressed in Joules per bit. For instance, the first monolithically integrated optoelectronic transceiver [256], [257] presented by Luxtera (fabricated with the 130-nm CMOS technology node) consumed 1.25 W at 10 Gb/s, equating to a power consumption of 125 pJ/bit. This power consumption figure includes the power consumed in the Serializer/Deserializer (SERDES), driver, and TIA for a point-to-point transmission, but not the more complicated signal processing elements analog-to-digital converter (ADC)/digital-to-analog converter (DAC) and digital signal processing (DSP) normally required for a long-haul communication network. Within that optoelectronic transceiver, the most power-hungry device is the MZM driver, which consumes 575 mW. This is mainly because the driver circuit uses double matching resistors at both ends of the MZM electrodes.

To enhance the power efficiency of an MZM driver, there has been some work [265]–[267] in recent years to increase the data rate of the transmitter by using more advanced fabrication processes, such as the 28-nm CMOS or the 55-nm BiCMOS technology node. For example, a data rate of 56-Gb/s ON–OFF keying (OOK) was achieved at 300 mW [266] fabricated with the 55-nm BiCMOS technologies, which equivalent to 5.4 pJ/bit. On the other hand, several designs [259], [262], [263], [272]–[275] adopted advanced modulation formats (such as PAM-4 or PAM-16) with segmented MZM approaches, with each segment of the MZM treated as a lumped capacitive element, thus eliminating the need for termination resistors. For instance, the power efficiency for segmented MZM is 0.25 pJ/bit for 40-Gb/s PAM-16 in [272]. However, it is difficult to claim these approaches are superior since the use of advanced modulation formats will inevitably suffer from worse OSNR performance and will require additional decoding circuits at the receiver side.

Besides the MZM, the ring-resonator-based modulator is a well-known device for low power consumption. It not only eliminates the use of 50-Ω matching resistors, but also features an exceptionally small footprint, which is preferred for monolithically integrated photonic circuits. For example, power consumption as low as 0.17 pJ/bit for the OOK mode [260] and 0.042 pJ/bit for the PAM-4 mode [262] has been demonstrated for the ring-resonator-based modulator, which is one order better than for MZMs. However, as has been mentioned in Section III, thermal stability, fabrication tolerances, and the narrow operating wavelength range limit its utilization. Control of these factors to make the use of a ring-resonator-based modulator practical would cause additional power consumption which needs to be considered when assessing the overall power benefits.

IX. RECENT TRENDS

Beyond the devices in optical communication wavelengths, silicon photonics at mid-infrared wavelengths is now emerging as a new frontier. Many groups around the world have started to work in this area because of the potential applications envisaged for chemical and biological sensing, trace-gas detection, environmental monitoring, etc. [93]. The potential of seamless integration of multiple components on a single chip offers an attractive solution for applications at mid-infrared wavelengths. Soref *et al.* theoretically studied various types of optical waveguides for longer wavelength transmission in 2006 [276]. Subsequently, various designs of grating couplers [277]–[280] and waveguide devices [114]–[116], [119], [121], [281] based on various platforms have been experimentally demonstrated at mid-infrared wavelengths, such as silicon-on-sapphire, air-cladded silicon (suspended silicon), Ge-on-Si, and Ge-on-SOI. A silicon cascaded Raman laser was demonstrated by Rong *et al.* in 2008, with a potential to make room-temperature lasers at mid-infrared wavelengths [282]. Raman amplification in mid-infrared was demonstrated in bulk silicon [283], with an amplification of 12 dB demonstrated at 3.39-μm wavelength. The absence of TPA at mid-infrared wavelengths also offers intriguing opportunities for the study and application of nonlinear optical effects, which may find applications in novel laser systems, gas sensing devices, or quantum photonic systems. More recently, there have been also studies investigating high-speed modulators [123] and detectors [167] beyond 1550-nm wavelength in order to potentially increase communication systems capacity.

Silicon has now been developed into a truly versatile platform with superior performances. It has been used as a platform for many other applications that had not been envisaged in the early years, such as photonic phased arrays [284], [285], microwave photonics systems [286], [287], and integrated optical gyroscopes [288]. Integrated quantum photonics and optomechanical devices on SOI platforms are also attracting great interest recently. Integrated optomechanical devices have the potential to integrate novel nano–opto–electro–mechanical systems on

chip. A detailed review is presented by Van Thourhout and Baets [289]. Quantum photonic circuits are also the subject of a great deal of emerging research for applications in secure communications, sensing, and computing systems. Silicon photonics has been proved to be the preferred platform to realize compact and scalable integrated quantum photonic circuits [290], [291].

The high cost of fabrication facilities has started a trend toward "fabless silicon photonic" [292], similar to the development of CMOS technology. In this approach, a research group or startup company can design photonic circuits and have them fabricated in a silicon photonics foundry. Some foundries offer cost sharing between users utilizing the so-called MPWs. This enables users to fabricate devices and circuits at a modest entry cost, typically starting at only a few tens of thousands of U.S. dollars, a small fraction of the total cost of the fabrication process of full SOI wafers. The equipment needed for fabrication of integrated photonic circuits is prohibitive for all but the largest companies, and therefore the shared platforms have facilitated a huge body of research work worldwide. Organizations which offer the ability to build passive and active photonic circuits in an MPW environment include, for example, the EPIXfab in Europe (now via Europractice) [293], IME in Singapore [294], and the CORNERSTONE project in the United Kingom [295], and has given affordable access to a photonics fabrication facilities for academia and industry alike.

X. CONCLUSION

Although origins of integrated optics date back to the early 1960s and 1970s, with a variety of materials and material platforms being investigated, the SOI platform still remains the most popular platform for silicon photonics. Device fabrication technology and postfabrication treatments are continually improving, and propagation losses as low as 0.7 and 0.1 dB/cm were demonstrated at 1550-nm wavelength for submicrometer strip and rib waveguides, respectively. The SOI platform is well suited for realizing the current and potential commercial products. As a complement to the SOI platform, a wide variety of materials have been considered for the visible and near-infrared wavelength regimes, including polysilicon, amorphous silicon, doped silicon dioxide, silicon oxynitride, and silicon nitride. Additionally, several other platforms such as silicon-on-nitride, silicon-on-sapphire, and germanium-on-silicon, among many others, are currently being investigated to enable and improve the performance of silicon photonic devices at longer wavelengths (2–16-μm wavelength range).

The cost of silicon photonic products is now dominated by the packaging process. An accurate and expensive active alignment process is generally required currently for silicon photonic devices. Although a lot of effort was spent to reduce the cost by developing low-cost passive alignment techniques or simplified/optimized active alignment techniques, the progress is modest, and no single "best" solution exists today. There are always some performance tradeoffs.

Regarding active components in silicon photonic circuits, monolithic integration of a viable laser source is not yet achieved. Hybrid III/V/Si lasers based on different bonding techniques have shown promising results, with multiple die-to-wafer bonding approach being pursued as the economically viable technique for industrial-volume fabrication. On the other hand, further progress in direct growth of QD or nanowire III/V lasers on SOI platform might eventually lead to fabrication of integrated light sources suitable for commercial applications. The integrated modulators and detectors in silicon photonics have been very successful in the last decade, and many commercial products are available. However, the modulation speed and power consumption of the current carrier-depletion-type modulators, and the sensitivity of the photodetectors are still not satisfactory for the ever-growing need for data capacity in the communication and computing network. ■

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ABOUT THE AUTHORS

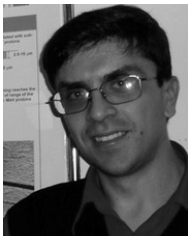
Xia Chen received the B.Eng. and Ph.D. degrees in electronics engineering from the Chinese University of Hong Kong, Hong Kong, in 2006 and 2010, respectively.

After graduation, he worked on the U.K. Silicon Photonic Project at the University of Surrey, Guildford, U.K. and the University of Southampton, Southampton, U.K. In 2013, he joined Huawei Technologies Co. Ltd as a Senior Engineer to work on photonic packaging. He rejoined the Silicon Photonics group at the University of Southampton in 2015. Currently, he is a Senior Research Fellow at the Optoelectronics Research Centre, University of Southampton. He has authored and coauthored over 90 papers in technical journals and international conferences and four patents.

Dr. Chen was awarded the TSMC Outstanding Student Research Award in 2010 and the Newton International Fellowship by the Royal Society in 2011.

Milan M. Milosevic received the Ph.D. degree from the University of Surrey, Guildford, U.K.

Currently, he is a Research Fellow at the Optoelectronics Research Centre, University of Southampton, Southampton, U.K., working on both industry and research council funded projects, led by Prof. G. Reed. Previously, he was working as an Engineer and Technology Consultant in the United States and Japan, and as a Research Fellow at the University of Surrey, where he received the Vice-Chancellor's Award for Early Career Excellence in 2012. He is particularly involved in high-speed optical transceiver technology and is one of the pioneers in mid-infrared silicon photonics technology for emerging applications.



Stevan Stanković received the Dipl.Ing. and M.Sc. degrees in optoelectronics from the Faculty of Electrical Engineering, University of Belgrade, Belgrade, Serbia and the Ph.D. degree in electrical engineering from Ghent University, Ghent, Belgium.

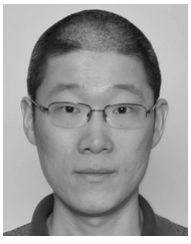
Since 2006, his research focused on silicon photonics, working initially on passive devices suitable for mid-infrared applications. From 2008 to 2012, he was working in the Photonics Research Group, Ghent University, where he designed and demonstrated evanescently coupled hybrid III/V/Si lasers, based on adhesive bonding. In January 2013, he joined the Silicon Photonics Research Group at the University of Southampton, Southampton, U.K., as a Postdoctoral Research Fellow. Currently, he is a Technical Manager of Silicon Photonics Capability at the University of Southampton. His research interest includes light sources and hybrid integration techniques in silicon photonics and, in general, technical challenges in fabrication of photonic integrated circuits. He authored and coauthored more than 35 journal and conference papers in the field of silicon photonics.

Scott Reynolds received the B.S. degree in electronics and computer engineering from the University of Surrey, Guildford, U.K., where he joined the silicon photonics group as a Ph.D. student in 2011

Subsequently, he joined the Optoelectronics Research Centre, University of Southampton, Southampton, U.K., where he is currently a Research Assistant, specializing in silicon photonic packaging. During his time there, he has been included as an inventor on a patent, coauthored a book chapter, and has contributed toward more than 19 journal and conference publications. He is working with his colleagues, industrial partners, and the versatile Southampton facilities to produce a packaging solution which is viable for mass market application.

Thalía Domínguez Bucio received the B.S. degree in electronic and computer engineering from the Monterrey Institute of Technology (ITESM), Atizapán de Zaragoza, Mexico, in 2012 and the M.Sc. degree in photonic technologies from the University of Southampton, Southampton, U.K., in 2013, where she is currently working toward the Ph.D. degree in optoelectronics.

Her research interests cover the development of a new material platform consisting of silicon nitride photonic applications.



Ke Li (Member, IEEE) received the MSc. degree in radio-frequency communications engineering and the Ph.D. degree in electronic engineering from the University of Southampton, Southampton, U.K., in 2005 and 2010, respectively.

He has nine years (14 chips) silicon proven experience in fully customized analog and microwave signals (>40 Gb/s) CMOS IC design down to 28 nm by using variety industry standard processes. He is currently a Research Fellow with the Silicon Photonics Group at the Optoelectronics Research Centre, University of Southampton. He is also working with the Wireless Communication Group in the School of Electronics and Computer Science to investigate the physical implementation of fully parallel LDPC/Tuobe decoders. His research interest includes design of high-speed modulator driver and TIA circuit, modeling and design of ultrawideband VCO and PLL circuit.

David J. Thomson joined the University of Surrey, Guildford, U.K., in 2001, as an undergraduate student studying electronic engineering and subsequently undertook Ph.D. studies under the guidance of Prof. G. Reed investigating optical switching devices in silicon.

Currently, he is a Royal Society University Research Fellow and Principal Research Fellow within the Silicon Photonics Group of the Optoelectronics Research Centre, University of Southampton, Southampton, U.K. He leads research in the area of photonics for computing systems. His career in photonics began with a year in industry at Nortel Networks, Paignton, U.K. From 2008 he worked as a Research Fellow at the University of Surrey on a number of projects and different optical devices in silicon although focusing mainly on high-speed active devices and their integration with other photonic and electronic devices. He moved to the University of Southampton in 2012, taking up the role of Senior Research Fellow. He has published over 40 journal papers, ten patent applications, and around 100 conference papers in the area of silicon photonics.

Dr. Thomson has served on four conference committees including the IEEE Group IV Photonics and SPIE Photonics West.

Frederic Gardes is an Associate Professor at the Optoelectronics Research Centre, University of Southampton, Southampton, U.K., and heads research on group IV material epitaxy and heterointegration for photonic and electronic devices and systems. His previous research covers Si photonics and in particular high-speed active optical devices in Si and Ge. In 2005, he initiated work on Si optical depletion modulators and was the first to predict operation above 40 GHz. In 2011, together with his collaborators, he demonstrated optical modulation in Si of up 50 Gb/s and a 40-Gb/s modulator. His recent work focuses on low index waveguiding systems for multilayer photonics and tunable material integrated to SOI. The latter includes the first ever demonstration of multiple crystalline SiGe on insulator wire of different concentration on a single chip using a single deposition process. He is a project expert reviewer for the European Commission, and has authored more than 190 publications, five book chapters, and eight patents.

Prof. Gardes is a member of several international conference programme committees.

Graham T. Reed is a Professor of Silicon Photonics and Group Leader. He joined the University of Southampton, Southampton, U.K., in 2012 from the University of Surrey, Guildford, U.K., where he was Professor of Optoelectronics, and was Head of the Department of Electronic Engineering from 2006 to 2012. He is a pioneer in the field of silicon photonics, and acknowledged as the individual who initiated the research field in the United Kingdom. He established the Silicon Photonics Research Group at the University of Surrey in 1989. The first silicon photonics company in the world, Bookham Technology Inc., was founded by Reed's Ph.D. student, Dr. A. Rickman, and adopted the research developed in the Group. The Silicon Photonics Group has provided a series of world leading results since its inception, and is particularly well known for its work on silicon optical modulators. He has published over 350 papers in the field of silicon photonics.

Prof. Reed is a regular invited and contributing author to the major silicon photonics conferences around the world. He has served on numerous international conference committees. He is currently a member of five international conference committees.