INVITED PAPER

Silicon-on-Insulator Substrates as a Micromachining Platform for Advanced Terahertz Circuits

This paper considers the development of terahertz systems-on-chip using micromachining techniques based on silicon-on-insulator technology.

By N. Scott Barker, *Senior Member, IEEE*, Matthew Bauwens, *Member, IEEE*, Arthur Lichtenberger and Robert Weikle, II, *Senior Member, IEEE*

ABSTRACT | This paper presents a comprehensive overview of the development and utilization of a micromachined silicon-on-insulator (SOI) fabrication process that has enabled the development of terahertz (THz) frequency superconducting-insulator-superconducting (SIS) and hot-electron bolometer (HEB) mixers, broadband directional couplers, on-wafer probes, as well as several multipliers. Through the detailed presentation of these circuits, it is demonstrated that ultrathin silicon is able to provide the required characteristics to enable the heterogeneous integration of multiple device technologies that is likely to be required for future THz system-on-chip (T-SoC) development.

KEYWORDS | Heterogeneous integration; micromachining; on-wafer probes; silicon-on-insulator (SOI); submillimeter wave; terahertz (THz)

I. INTRODUCTION

Terahertz (THz) electronics has been a topic of research and development for many years, motivated largely by the technological needs of the radio astronomy and remote sensing scientific communities. Over the past decade, however, this field has experienced dramatic growth and intense, renewed interest due to the establishment of a commercial infrastructure that has made test and measurement instrumentation available to the engineers and scientists working at these frequencies. Moreover, the recent development of transistors operating beyond 1 THz and the emergence of complementary metal–oxide–semiconductor (CMOS) as a potential submillimeter-wave device technology has greatly expanded access to this spectral region by providing circuit designers with a foundation for realizing new THz circuit architectures.

Moving THz technology forward into ubiquitous applications (e.g., short-range high data-rate communications) will likely require the development of a THz system-on-chip (T-SoC) that will accommodate CMOS baseband processing and a THz front-end with multipliers, mixers, and even amplifiers. Such a T-SoC would, by necessity, require heterogeneous integration of one or more compound semiconductor such as GaAs or InP onto a substrate that is mechanically robust, has low dielectric loss, and whose lateral dimensions can be lithographically defined. This paper will illustrate how a micromachined silicon-on-insulator (SOI) fabrication process can be used to produce ultrathin silicon substrates that provide the required characteristics. The paper begins by comparing the relevant material properties of silicon to other candidate substrates along with a brief overview of the micromachined SOI fabrication process in Section II. Section III presents the history of superconducting THz receivers followed by the development of SOI-based circuits for this application. Section IV details the adaptation of the micromachined SOI process for the successful development of on-wafer probes operating to over 1 THz. Finally, Section V covers current progress in heterogeneously integrating THz electronic devices (specifically GaAs Schottky diodes) onto ultrathin silicon.

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N.S. Barker, A. Lichtenberger, and **R. Weikle** are with the Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22904-4743 USA, and also with Dominion MicroProbes Inc., Charlottesville, VA 22905 USA (e-mail: barker@viginia.edu).
M. Bauwens is with Dominion MicroProbes Inc., Charlottesville, VA 22905 USA.

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Table 1 Material Properties of Candidate Membrane Materials

Material	Elastic Modulus E (GPa)	Yield Strength σ^{yield} (MPa)	Relative Permittivity ϵ_r	Thermal Conductivity (W/m·°C)	Modulus of Resilience (kJ/m^2)
Fused Quartz [9]	72	48	3.8	1.4	16
GaAs [10], [11]	118	85	12.9	55	30
Alumina [12]	300	330	9.1	30	181
Kapton HN Polyimide [13]	2.5	69	3.4	0.12	952
Silicon Nitride [14]	310	830	5-8	30	1,111
Single Crystalline Quartz [15]	97	1700	4.6	12	14,897
Silicon [16]–[18]	169	4500	11.9	148	59,911

II. SOI FOR FLEXIBLE THz SUBSTRATES

The development of THz frequency planar circuits requires the use of low dielectric-constant and/or ultrathin substrates to limit the substrate thickness to $\lambda_d/10$ or less. This trend is a result of needing to avoid excessive coupling to substrate modes or, in the case of circuits packaged in waveguide blocks, the generation of higher order modes within the package. In addition, planar THz circuits often require coupling to rectangular waveguide and therefore the ability to shape the lateral dimensions of the substrate is desired in order to optimize the waveguide transition for maximum return loss. Fused quartz, due to its low dielectric constant and low dielectric loss at THz frequencies, has often been the substrate of choice. However, as the operating frequency of these circuits increases, the waveguide cross section, and hence chip size and placement tolerance decrease. A displacement of the chip in the waveguide block can result in additional loss, degraded sensitivity, and may give rise to unwanted resonances. The shrinking chip dimensions make it increasingly difficult to make connections to the chip (e.g., DC, IF, and RF ground). These connections are typically made via wire bonds, solder bumps, conductive crush wires, conductive epoxy, or microsprings [1], [2], and cracking of the delicate substrates while mounting, and breaking of epoxy bonds and wirebond joints, can be significant factors in circuit yield and longevity. Finally, quartz is relatively brittle with minimal deformation range and becomes particularly fragile and increasingly susceptible to fracture when thinned below ~50-μm thickness.

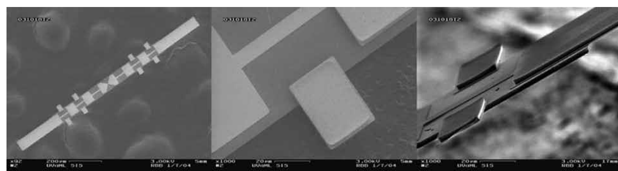


Fig. 1. ***The left-most micrograph shows a top-down view of an ultrathin silicon chip with beam leads and integrated RF circuitry. The middle micrograph shows a closeup of a structural beam lead, while the right-most micrograph shows a 3-μm-thick silicon chip with 2-μm-thick gold beam leads of various lengths protruding from the perimeters. The longest beam lead extends 250 nm beyond the edge of the silicon [23].***

A. Silicon Material Properties

In 2003, building on previous UVA work to develop quartz chips with beamleads [13], [14] and other research with GaAs membranes [15]–[18], UVA researchers developed an alternative chip and packaging architecture utilizing ultrathin silicon chips with Au beamleads for superconducting THz circuits [19]. The limitations of the quartz wafer architecture can largely be overcome by using thin dielectric membranes supported by integral Au beamleads as shown in Fig. 1. Silicon offers several advantages over quartz and other candidate membrane materials for THz chip applications (see Table I). The yield strength σ^{yield}, of single crystal silicon is reported to be as high as 7000 MPa [20]. As a result, thin Si can be handled much more successfully than quartz: beamlead Si chips as thin as 1.5 μm [19] and 1.0 μm [21] have been successfully fabricated and mounted in waveguide blocks. In addition, silicon has a tremendous ability to store strain energy—an indication of the amount of bending a material can withstand without yielding (or fracturing in the case of most crystalline materials) defined as

$$u^y = \frac{(\sigma^{\text{yield}})^2}{2E}$$

where E is the elastic modulus. For applications where the membrane material is required to bend, such as on-wafer probing

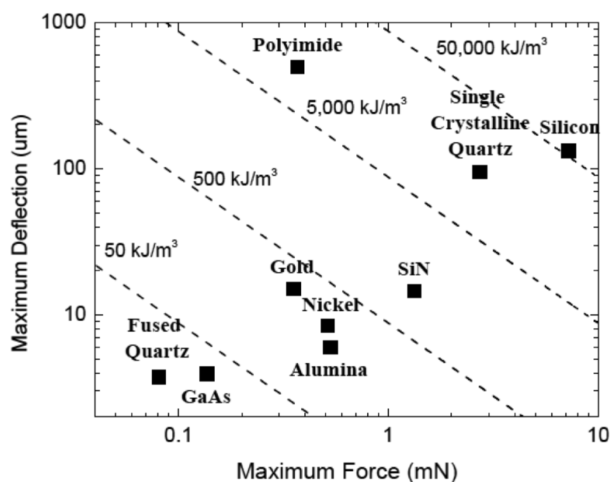


Fig. 2. ***Comparison of the performance of the materials in Table I in a cantilever structure. These results are for a 350-μm-long, 15-μm-wide, and 15-μm-thick cantilever. Contours of constant strain-energy density for the cantilever are indicated by the dashed lines.***

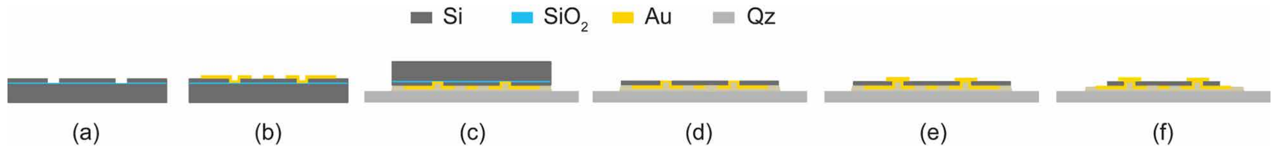


Fig. 3. ***Outline of the micromachined SOI fabrication process: (a) Via-hole definition. (b) Frontside gold. (c) Carrier mounting. (d) Handle and BOX layer removal. (e) Backside gold. (e) Si extents etch.***

(see Section IV), it is also useful to consider the ability of a material to generate a restoring force under a given deflection. Fig. 2 shows both properties (restoring force and strain energy) for a prototypical cantilever beam with dimensions 350 μm $\times$ 15 μm $\times$ 15 μm. As can be seen, silicon is capable of generating significantly more force than the other candidate substrates. The thermal conductivity of silicon (148 W/m·K) [12] is also two orders of magnitude higher than that of amorphous quartz (1.5 W/m·K) [22] which can be critical for cooling superconducting devices as well as room temperature GaAs devices. Silicon has a much larger dielectric constant ($\epsilon_r = 11.9$) than fused quartz ($\epsilon_r = 3.8$), but since Si chips can be made with micrometer thickness, this does not present an impediment to the design of THz circuits as will be demonstrated in the following sections.

B. Fabrication Process

Many of the typical methods for realizing DC, IF, and RF connections (e.g., wire bonds, solder bumps, conductive crush wires, or microsprings) cannot be employed when using micrometer-thick silicon chips as the chips would shatter. Instead, Au beamleads extending from the perimeter of the chip are used to provide electrical, thermal, and mechanical connections without the need for any direct connections to the Si membrane. The mechanical rigidity of the plated beam leads is sufficient to support the chip between the two halves of a split waveguide and across the middle of a waveguide channel. This beamlead mounting approach provides a natural method of making the electrical and thermal connections to millimeter and submillimeter circuit chips, simplifies the block design and machining through the straightforward grounding approach of clamping the grounding beamleads between block faces, and avoids the need for small ledges/shoulders in one of the split blocks to suspend a quartz chip. The beamleads are robust enough to handle the rigors associated with assembly, even when extended several hundred micrometers beyond the perimeter of the chip.

The UVA ultrathin Si chip architecture utilizes SOI material [21] with a thin Si device layer of high resistivity (>10 000 Ω-cm) Si, on 1 μm of SiO_2 buried-oxide (BOX) insulator, on a thick Handle layer of silicon. The details of the UVA SOI processing approach for superconducting detectors can be found in the literature [19], [23]–[26]. The thick Handle Si layer provides a robust carrier for easily handling and processing the thinner device Si layer. In summary, the frontside circuitry, detector, and plated Au beams (extending beyond the intended perimeter of the chip) are defined on the frontside of the thin Si device layer [Fig. 3(a) and (b)]. The SOI is temporarily frontside-down mounted to a carrier wafer using an adhesive, and the thick Si handle layer and the SiO_2 BOX layer removed [Fig. 3(c) and (d)]. The revealed backside of the device Si layer is patterned with resist to define the intended chip extents and the Si dry etched, revealing the Au beamleads, and defining the chip extents [Fig. 3(e) and (f)]. Finally, the membrane chips are dismounted by dissolving the adhesion layer with a solvent.

Though the backside SOI fabrication requires additional processing steps, it still saves a substantial amount of time compared with lapping and precision dicing a quartz wafer. Since the typical device Si thickness for THz detectors is 3–8 μm, a standard Si RIE dry etch can be used to realize the finished chip size accurately ($\pm$0.2 μm) without need for a special BOSCH [27]–[29] or cryo-etching process [30], [31]. The important registration of circuitry to the chip depends on the backside alignment. For thin device layers, prior to the chip extents step, the Si locally covering the alignment markers can be etched away [26], revealing the original frontside alignment marks and allowing for a better than $\pm$1-μm true frontside alignment between these front and backside features. The beamleads can be realized to better than $\pm$0.2-μm size. Mounting of the chip in the waveguide block, given the above chip and beamlead tolerances, essentially becomes a drop in assembly with little to no further manual alignment. The SOI process also allows for nonrectangular chip geometries [21] that could not be realized with the conventional quartz dicing-saw approach. This also permits definition of Si beamleads for waveguide alignment with increased physical ruggedness in chip mounting [32].

III. SOI FOR SUPERCONDUCTING THz RECEIVERS

A. Historical Background—Superconducting THz Receivers

In the half century since the first demonstration [33] of the superconducting Josephson effects in 1963 [34], superconducting electronics has made significant strides. The development of Josephson junction technology has led to millimeter- and submillimeter-wavelength heterodyne and bolometric mixers with nearly quantum-limited sensitivity, superconducting quantum interference devices (SQUIDS) as highly sensitive detectors of magnetic fields, magnetic resonance imaging (MRI) systems, amplifiers, voltage standards,

oscillators, and digital electronics [e.g., rapid single flux quantum (RSFQ)]. Other developments in superconducting electronics include transition edge sensors (TESs), kinetic inductance detectors (KIDs) for X-ray spectroscopy and radio astronomy, and Josephson-based magnetic memory. However, superconducting THz electronics, to date, has primarily been focused on superconducting mixers.

Compared to semiconductor Schottky diodes, high-quality superconducting–insulating–superconducting (SIS) tunnel junctions have extremely nonlinear electrical characteristics. For millimeter-wave mixers using SIS junctions, classical mixer theory must be modified to include quantum effects. The first SIS mixers [35]–[37] used simple circuits with lead-based SIS devices and relatively thick Si or quartz substrates. SIS mixing is described by quantum mixer theory, originally developed by Tucker [38], [39], where Tien and Gorden [40] photon-assisted tunneling must be taken into account in the mixing process. This theory, in concert with robust materials, and repeatable SIS junction fabrication, revolutionized millimeter-wave radio astronomy through the development of receivers with unprecedented sensitivity. The first SIS mixers used in radio astronomy [41]–[44] employed lead-based junctions and quartz substrates with manually adjustable waveguide tuners. The Gurvitch process [45], [46], using partially oxidized Al overlayers for the tunnel barrier, allowed the transition from the lead SIS technology, which is sensitive to moisture and ESD, and difficult to process, to the more physically robust and processing compatible niobium mixers [47]–[52], and subsequently to more complicated circuit designs with integrated tuning elements, obviating the need for mechanical tuners [53]–[56].

SIS mixers are now the low-noise heterodyne–receiver technology of choice for radio astronomy at frequencies from about 100 GHz to 1.2 THz, and are employed on all the world's major millimeter- and submillimeter-wave observatories, including the recent major international astronomical projects: Herschel HIFI [57], [58] and ALMA [59]–[66]. All of the above referenced superconducting papers (except [35]) used conventional rectangularly diced and thinned quartz substrates suspended across a waveguide.

Alternative approaches to the quartz substrate and waveguide configuration have been pursued including, in the 1990s, silicon micromachining, using preferential crystal plane wet etching techniques to form micromachined Si frames with thin SiN_4 membranes [67] for superconducting quasi-optical SIS mixers with integrated Si horns [68], [69], and a waveguide mounted SIS mixer with SiN_4 membrane and Si frame [70]. However, as computer numerical control (CNC) machining technology has improved over the past several decades, the advantages afforded by a waveguide approach have eclipsed the membrane/Si-horn architecture for superconducting detectors.

B. SOI-Based Superconducting Mixers

In 2004, JPL reported the development of a SOI process with a much thicker 25-μm Si membrane [71]. UVA reported the first SOI-based superconducting mixer using a hot electron bolometer [23], [72], while Caltech reported the first SOI-based SIS mixer shortly thereafter [73], [74]. The SOI architecture, in addition to having advantages over quartz particularly at higher frequencies, is also attractive for receiver arrays and astronomical facilities with multiple antennas such as ALMA where the mounting of a significant number of mixer chips is required. SOI-based SIS chips were used in the array receivers Supercam [75], [76] and KAPPA [32], and a 350–500-GHz SIS mixer [77] that met the ALMA Band-8 noise temperature requirements. Other SOI-based HEB mixers have been reported by UVA [72], [78], JPL [79], [80], and Chalmers [81] where a double SOI stack process was developed to realize a frame support for the HEB SOI chip, and Köln with a 450-GHz balanced mixer [82] and a 4.5-THz HEB SOI mixer [83].

Two of these mixer designs are examined here in more detail to illustrate the detector design options with SOI. The first design is for SuperCam, a 64-pixel heterodyne camera designed for astrophysical observations in the important 870-μm atmospheric window. Astronomical interest in array receivers stems from their increased efficiency at mapping extended sources, such as molecular clouds, compared with a single-pixel receiver. SuperCam is constructed by stacking eight 8-element rows of fixed-tuned SIS mixer preamps, each with its own pyramidal feed horn. The RF and local oscillator signals enter each mixer via its feed horn and are coupled to the SIS junction via a broadband radial probe connected to the microstrip circuit. To match the SIS junction to the waveguide probe an end-loaded stub is employed (Fig. 4). The RF circuit was designed using Pcircuit [84], a superconducting linear circuit simulator originally written by Zmuidzinas and Bin [85], in combination with Sonnet em [86], modeling the superconducting thin film transmission lines as described in [87]. The low impedance section of the end-loaded stub is tapered to minimize the fringing capacitance of the transition.

The substrate that supports the single 1.13-μm^2 SIS junction (RnA = 22.6 Ω-μm^2) and RF matching network is 3-μm-thin Si with Au beamleads. The SIS junction design for SuperCam was conservatively based on the mature UVA Al-oxide barrier technology to minimize risk and because

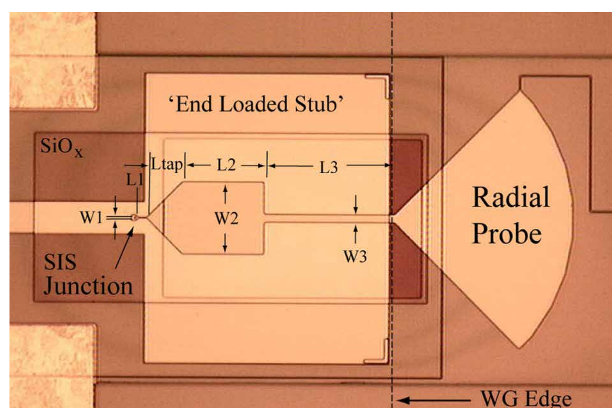


Fig. 4. ***1000x photomicrograph of the radial probe transition and junction area. The meandering IF/DC return line across the waveguide is 2 μm wide.***

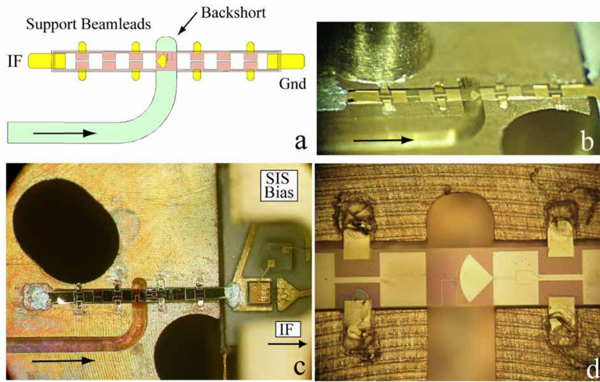


Fig. 5. ***Composite view of the SuperCam waveguide-to-microstrip transition. The eight-side beamleads are important in determining the Z-dimension. The SIS DC/IF return may be accomplished via the integrated side beamleads, however this approach was not used in the SuperCam chip design.***

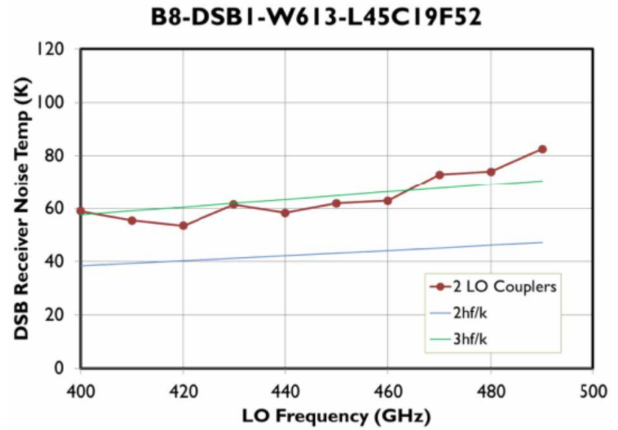


Fig. 7. ***Double sideband receiver noise temperature versus LO frequency for the Si membrane mixer.***

the instrument does not require the larger RF bandwidth possible with a high current density AlN barrier. The choice of a 3-μm Si substrate facilitates scalability to well beyond 1 THz while preventing the propagation of higher order modes in the substrate and its channel. The support beamleads along the sides of the substrate have no significant effect on the RF performance of the circuit. In this design, the beamleads are crucial in aligning the substrate with the center of the waveguide and for securing the chip. The width of the support beamlead channels is 120 μm, leaving a 10-μm space on either side of the beamleads, which in principle could be reduced further for improved drop in alignment. Fig. 5(a) shows a rendition of the SOI chip with its beamleads. Fig. 5(b) is a photograph taken at an oblique angle where the side and IF/DC beamleads are clearly visible. The width of the substrate channel provides a 12.5-μm space on either side of the substrate. The effects of chip misalignment, as is evident in Fig. 5(d), are small when compared with those due to the tolerances in SIS junction and RF circuit fabrication.

The second example of a submillimeter-wave circuit on a silicon membrane is a single pixel 385–500-GHz SIS waveguide mixer with a 3-μm-thick Si chip and 2-μm-thick gold beamleads (Fig. 6) [77]. The design of this mixer is based on that of the ALMA Band-6 (211–275 GHz) mixer described in [88]. The mixer has four 0.78-μm^2 SIS junctions with an inductively coupled plasma AlN tunnel barrier [89], [90] grown from an Al overlayer. The critical current density is 20 kA/cm^2.

To mount the mixer chips in the waveguide block, small amounts of H20E silver epoxy [91] are placed in the beamlead recesses and on the IF/DC contacts at the end of the channel. The beamleads of the mixer chip are then placed on top of the droplets whose surface tension pulls the chip into alignment with little or no adjustment. A glass slide is used to cover the chip and hold it in place while the epoxy cures at 90 °C. This receiver is still in development, however preliminary results are shown in Fig. 7.

C. SOI-Based Directional Couplers

A third example of a membrane and beamlead circuit is the 10-dB coupled-line directional coupler shown in Fig. 8 [92]. Fabricated on a 10-μm-thick silicon membrane and suspended in an E-plane split waveguide block, this coupler is designed to have equal even and odd mode phase velocity in the coupled lines and a flat coupling factor across the WR2.2 band (330–500 GHz) by completely removing the silicon from beneath the coupled lines. The transmission lines for the

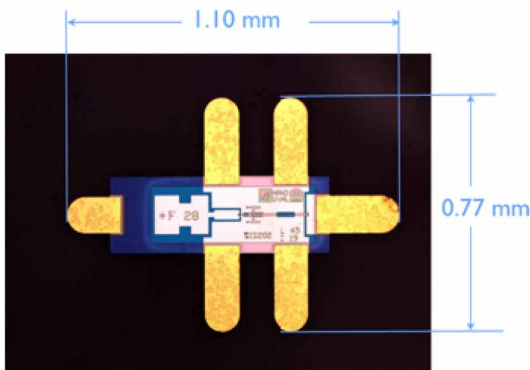


Fig. 6. ***An NRAO-UVA-AZ superconducting mixer for 380–500 GHz on a 3-μm Si membrane substrate with gold beamleads.***

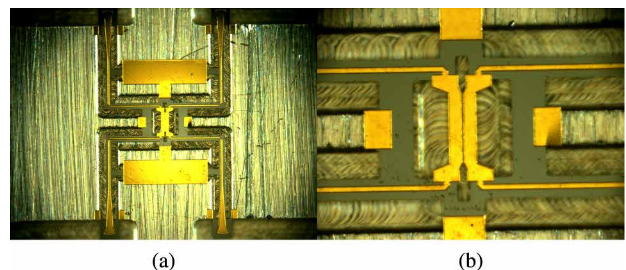


Fig. 8. ***Photomicrographs of the silicon membrane coupler in the machined block suspended by gold beamleads [92].***

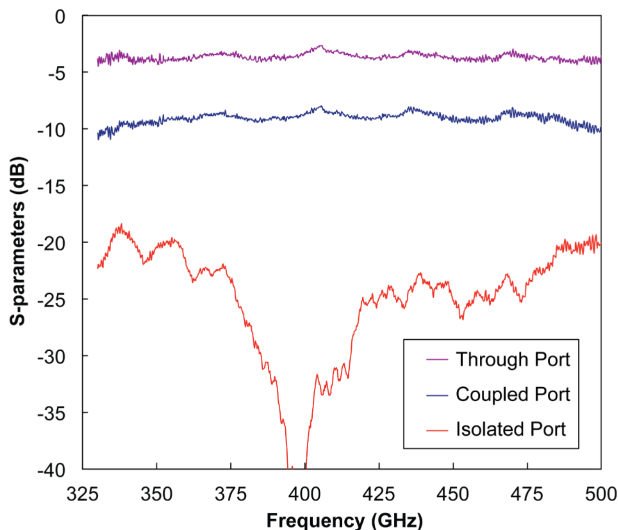


Fig. 9. ***Measured coupler with 3.6-μm coupling gap and suspended 24 μm above the ground plane [92].***

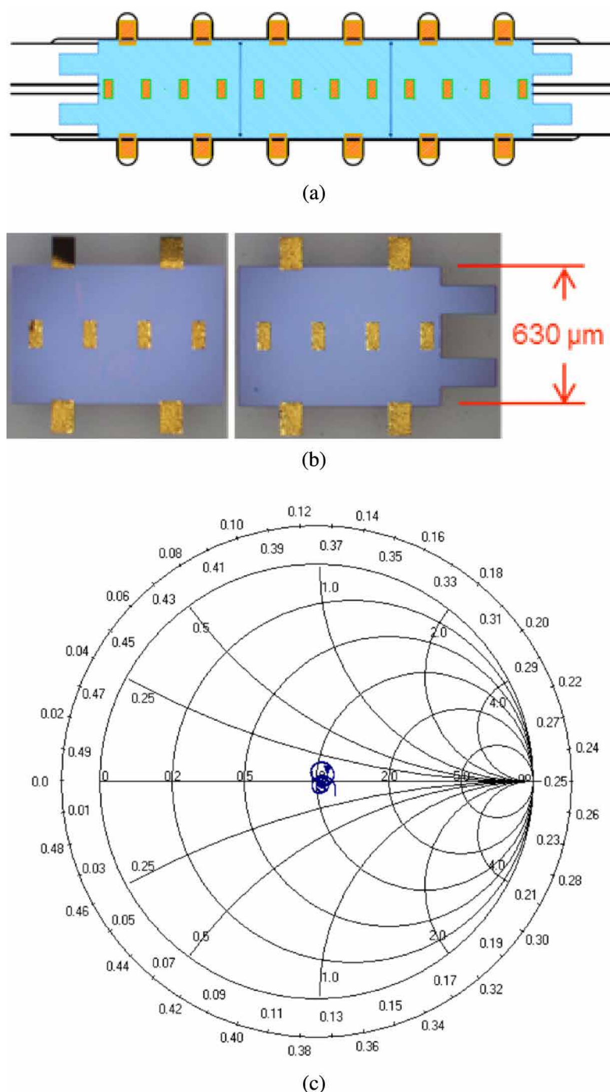


Fig. 10. ***A modular "drop-in" waveguide directional coupler for 385–500 GHz on a Si membrane substrate with gold beamleads. The number of modules can be selected to give the desired overall coupling. The Smith chart shows S11 across the band.***

circuit leading to the coupled lines were designed as hybrid microstrip lines. The silicon membrane is suspended 10 μm above the bottom of the CNC machined block and held in place by the beamleads clamped between the block halves. The resulting characteristic impedance and transmission-line attenuation are 69 Ω and 1.1 dB/mm at 425 GHz, respectively. The dimensions of the channel in which the transmission line is suspended were designed to prevent the propagation of higher order modes. To achieve high isolation, the right-angle bends and waveguide probes were designed for >25-dB return loss across the band. Due to fabrication tolerances (the coupled-line gap was 3.6 μm rather than the designed 3 μm) and machining tolerances (the bottom-half waveguide block channel was 24 μm deep rather than the designed 20 μm), the resulting isolation was >20 dB as shown in Fig. 9 resulting in 10–20-dB directivity.

An alternative coupler design is the modular drop-in waveguide directional coupler shown in Fig. 10 [93]. It was also fabricated with UVA's SOI process and is used as the local oscillator coupler for the previously mentioned SIS mixer. The number of modules can be selected to give the desired overall coupling: 1, 2, or 3 modules give 20-, 16-, or 10-dB coupling. The nonrectangular substrate has Si prongs, visible in the photographs, which extend into the waveguides to improve the return loss at the ports of the coupler.

IV. MICROMACHINED ON-WAFER PROBES

In addition to providing an excellent substrate for the development of thin silicon-membrane THz circuits, silicon can also be used mechanically. As pointed out in Section II-A, silicon is able to store a significant amount of strain energy before fracturing. These characteristics provide a unique foundation for the development of THz direct-contact on-wafer measurement tools. To illustrate the flexibility of this technology for THz metrology, this section describes on-wafer probes developed at UVA using the SOI micromachined silicon process including: a micromachined probe for characterization of devices to 1.1 THz, an integrated balun probe for characterization of W-band differential circuits, and a 750-GHz probe with integrated strain sensors for improved contact repeatability. These micromachined probes are based on the previously described ultrathin SOI process developed at the University of Virginia [23]. The process has been augmented to include metallized vias along with patterned electroplated gold on both the front and back sides of the thin silicon in order to secure the silicon membrane between the two halves of a CNC machined split block without initiating cracking [94]. The success of the SOI-based on-wafer probes led to their commercialization through the start-up company Dominion MicroProbes.

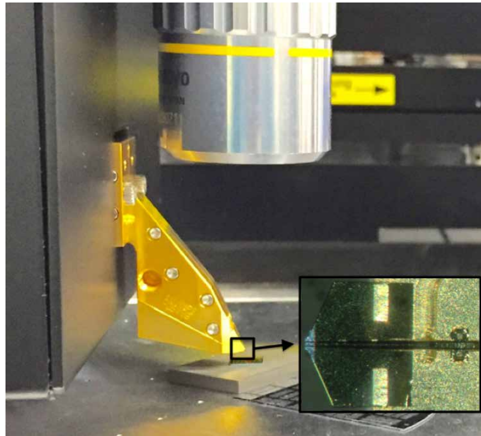


Fig. 11. ***Revised 1.1-THz micromachined probe design. The new design does not require a waveguide twist section and provides access to the full chuck. The inset shows the silicon micromachined chip placed over the waveguide channel.***

The probes are currently marketed and sold as the T-Wave Probe by Cascade Microtech [95].

A. 1.1-THz On-Wafer Probe

Substantial progress has been made recently in the development of THz integrated circuits [96]–[100]. To aid in the characterization of these circuits, an on-wafer probe was designed and fabricated in 2011 using silicon micromachining technology that enabled for the first time on-wafer measurements up to 750 GHz [101], [102]. To further expand the THz measurement infrastructure, an on-wafer probe for the WR-1.0 waveguide band was subsequently developed at UVA using the same silicon micromachining technology to permit characterization of devices and circuits from 750 GHz to 1.1 THz [103].

The micromachined probe design described in [103] utilizes an E-plane split waveguide housing, where the waveguide axis is orientated at 30° and the electric field polarization is parallel to the ground. Our first approach to connect the probe to Virginia Diodes' 1.1-THz frequency extenders [104] was to microfabricate a 90° waveguide polarization twist section [105]. Unfortunately, this twist section introduced considerable loss as well as a discontinuity at the probe's waveguide input. In addition, due to the geometry of the probe housing, the sample under test had to be elevated to the probe tips with a riser and, as a consequence, the sample size that was able to be probed was limited to less than ~ 1.7 in.

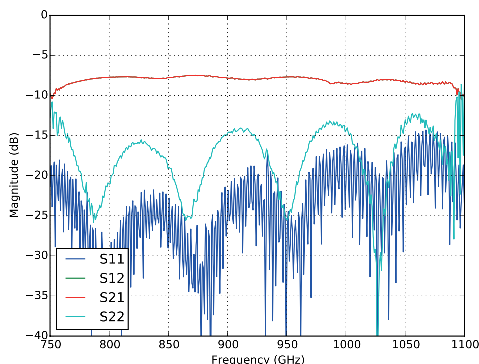
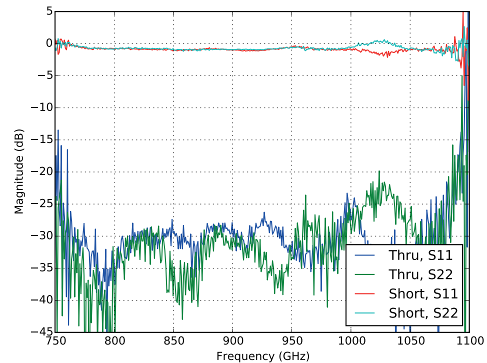
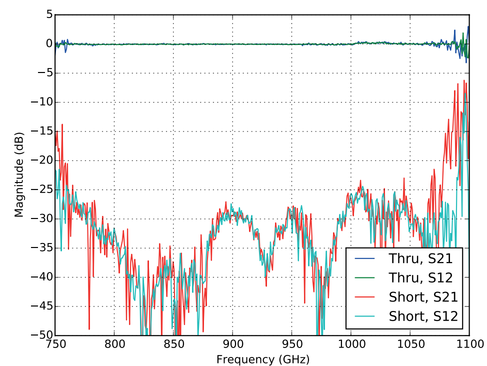


Fig. 12. ***Measured S-parameters of the revised 1.1-THz micromachined probe design. Port 1 is the waveguide input; port 2 is the coplanar probe tip output.***



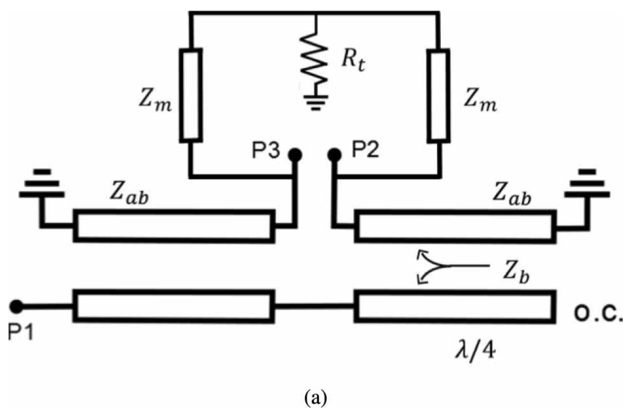
(a)



(b)

Fig. 13. ***Calibrated dynamic range of the 1.1-THz probe system (IF bandwidth is set to 100 Hz). (a) Reflection. (b) Transmission.***

To address these issues, the 1.1-THz micromachined probe design has been revised. The new design, shown in Fig. 11, eliminates the need for the waveguide twist and chuck riser permitting direct chuck access for probing full size wafers. The SOI fabrication process described above allows integration of the waveguide transition, coaxial transmission line, GSG contacts, and DC bias-T all onto a single, lithographically defined chip. The calibrated S-parameters of the probe are shown in Fig. 12, illustrating an insertion loss of better than 10 dB and return loss of better than 12 dB. To evaluate the RF performance of the 1.1-THz probes, an on-wafer multiline TRL calibration is performed using coplanar waveguide transmission line standards. The IF bandwidth is set to 100 Hz, and after calibration, the thru and short are remeasured. The results shown in Fig. 13 illustrate a calibrated dynamic range of approximately 25 dB over most of the WR-1.0 band.



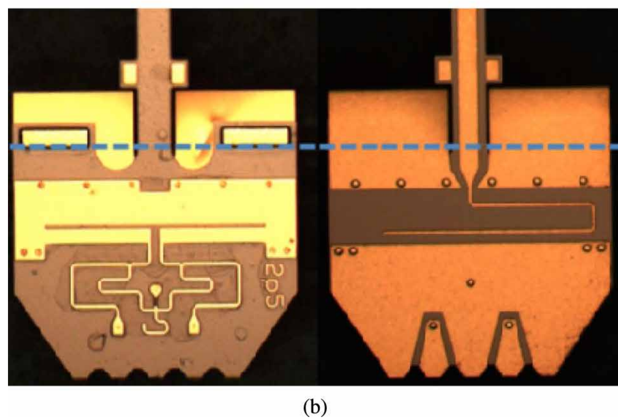
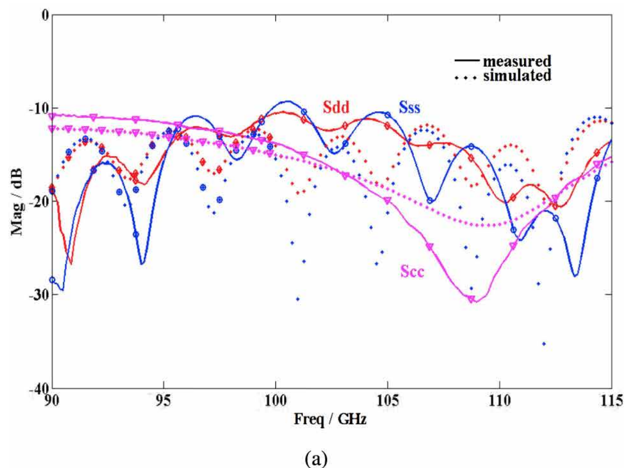


Fig. 14. ***Micromachined integrated balun probe chip [109]. (a) Equivalent circuit. (b) Left: backside showing balanced output and common-mode matching circuitry; right: frontside circuitry showing single-ended input and 100-μm pitch GSGSG contact pads at bottom. The dashed line indicates the location edge of the waveguide housing of the assembled probe. The coaxial transmission line from the waveguide is shown above the dashed line.***



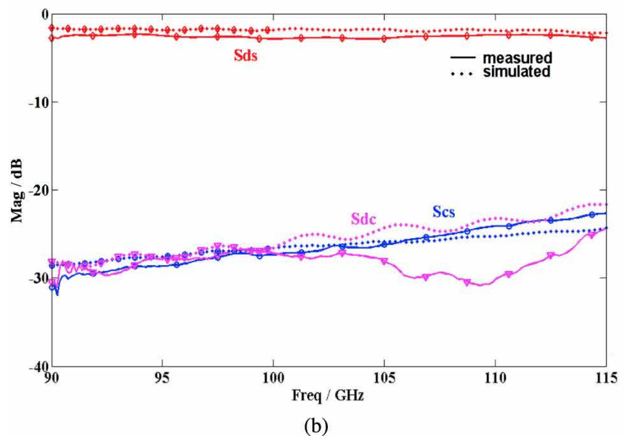


Fig. 15. ***Micromachined integrated balun probe performance. (a) Single-ended, differential, and common-mode reflection coefficients. (b) Mode conversion terms [109].***

B. Integrated Balun Probe

An increasing number of circuits such as amplifiers and oscillators utilizing differential inputs and outputs are being developed for submillimeter-wave applications [106]–[108]. At microwave frequencies, characterization of differential circuits is performed using on-wafer probes having differential probe tip contacts, such as ground/signal(+)/ground/signal(−)/ground (GSGSG). Above 110 GHz, however, differential probes are not available. As a result, the only way to characterize such circuits is to include an on-wafer balun such that the circuit can be excited with a single-ended probe, or to couple to the circuit some other way, e.g., quasi-optically using a differential patch antenna. These structures not only consume valuable wafer real estate, but also must be characterized to estimate the native performance of the device-under-test (DUT). To enable the direct characterization of THz differential circuits, a proof-of-concept on-wafer probe with integrated balun has been developed for W-band applications [109].

The silicon-micromachined integrated-balun probe chip is shown in Fig. 14. At the probe tip, the coaxial mode is converted to microstrip, which feeds the input of a Marchand balun. The balanced output emerges on the back side of the probe tip, where a matching network utilizing a titanium thin-film resistor terminates the common-mode signal. Finally, vias are used to transition the balanced microstrip signal to GSGSG coplanar output pads.

The calibrated S-parameters of the integrated balun probe are shown in Fig. 15. The differential, single-ended, and common-mode matching terms are better than 10 dB over most of the band. The probe exhibits a single-ended to differential mode conversion loss of less than 2.5 dB, while common-mode conversion terms are less than -22 dB. The maximum magnitude and phase imbalances are 1.5 dB and 7°, respectively, demonstrating that the micromachined SOI fabrication process can be used to realize full waveguide-band differential probes. This design is currently being scaled to higher frequencies to enable characterization of differential circuits at frequencies up to 300 GHz.

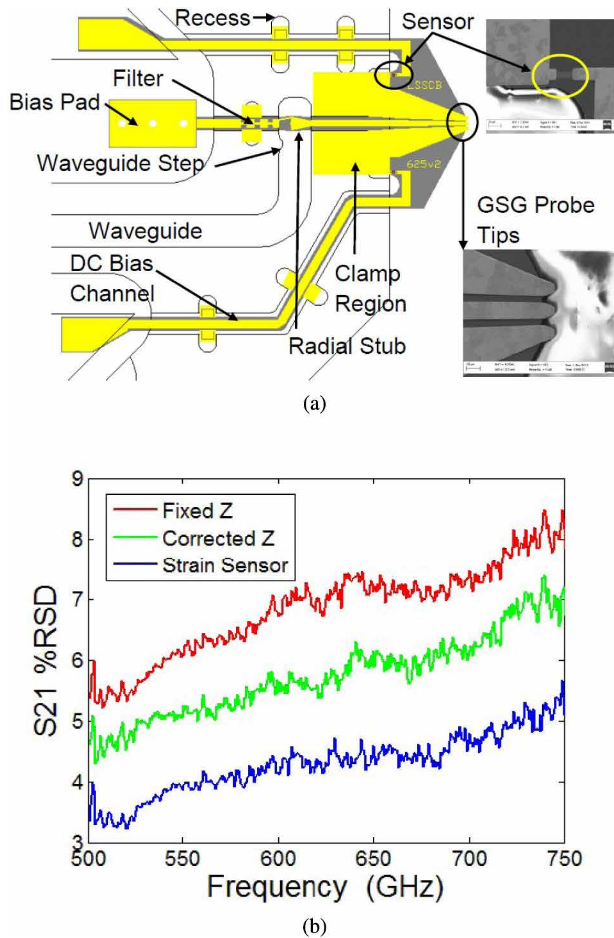


Fig. 16. *(a) Split-block view of micromachined probe with integrated strain sensors [110]. (b) Relative standard deviation of the probe insertion loss using different contact methods.*

C. Integrated Strain Sensor Probe

In addition to transmission line circuits, mechanical sensors can also be directly integrated onto the micromachined Si-membrane. This becomes useful at THz frequencies where the landing repeatability of an on-wafer probe is a significant concern. For example, on silicon, a 1-μm section of coplanar waveguide represents roughly 3° of electrical length at 1 THz. As a result, variations in wafer thickness, probe station chuck planarity, and contact height repeatability play a significant role in the accuracy of THz on-wafer measurements. To investigate a potential mechanism for improving control over probe contact, a silicon micromachined probe with integrated strain sensors was developed [110].

The silicon micromachined strain sensor probe is shown in Fig. 16(a). Two thin-film nickel–chromium (Ni–Cr) sensors are fabricated on each side of the probe tip. As the probe contacts an on-wafer device, the silicon chip deflects generating strain along the probe chip that is greatest toward the portion of the chip clamped by the waveguide block. This strain is measured as a change in resistance of the Ni–Cr film, and by utilizing a pair of sensors any strain imbalance can be detected and used to correct probe tip planarity as well.

To evaluate the effectiveness of the stain sensor probe, an on-wafer calibration routine was performed repeatedly on Cascade Microtech PA200 semiautomatic probe station using three different contact methods. The first method is “fixed-Z” contact, which used a fixed contact height at all points across the sample wafer. The second is “corrected-Z,” which used image processing to determine the focal point at each point on the sample wafer. Variations in focal point due to wafer thickness or chuck planarity were used to adjust the contact height at each point on the sample wafer. Finally, the strain sensor was used to monitor contact force and provide feedback for adjusting the contact height. The results of this experiment are shown in Fig. 16(b). The integrated strain sensor probe provides improved repeatability over both fixed-Z and corrected-Z techniques. The micromachined on-wafer probes clearly demonstrate the use of ultrathin silicon as a mechanically robust and low-loss substrate whose lateral dimensions can be defined lithographically.

V. HETERGENEOUS INTEGRATION OF THz DEVICES USING SOI

The packaging of THz devices to yield complete components and systems has traditionally relied on hybrid assembly methods based on flip-chip mounting, wire bonding, or use of conductive adhesives. Although this approach has proven practical for realizing circuits operating at millimeter wavelengths, it is widely recognized that the uncertainties associated with chip alignment and registration limit the practicality of these techniques when applied to circuits operating at frequencies much higher than 300 GHz. Moreover, the ill-defined geometries associated with manually applied conductive epoxies or solder bumps typically result in parasitic reactance that is not well characterized, yet is significant enough to have considerable impact on circuit performance at THz frequencies.

Heterogeneous integration of submillimeter devices onto a host substrate, such as silicon, offers an alternative approach to packaging and assembly that permits semiconductor devices and associated circuitry to be defined and registered lithographically, eliminating the imprecision and irreproducibility associated with hybrid assembly methods. In addition, as detailed in Section II, the silicon integrated substrate is amenable to postprocessing, permitting an integrated carrier of arbitrary shape to be formed that may incorporate beamlead tabs for electrical connection or alignment and mounting to a housing.

A. Integrated Submillimeter-Wave Diodes

The Schottky barrier diode and its variations (notably, the heterostructure barrier varactor [113]) represent the most mature and important device for noncryogenic applications in the submillimeter region of the spectrum

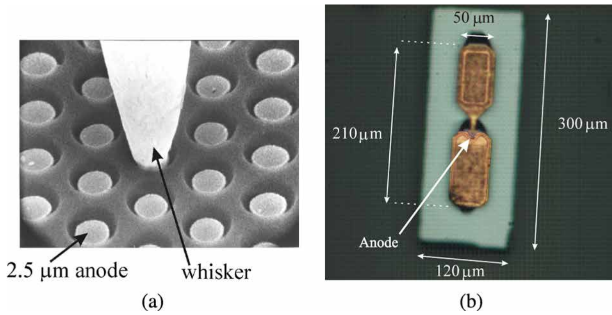


Fig. 17. *(a) Scanning electron micrograph (SEM) of a 2.5-μm diameter whisker-contacted Schottky diode [111]. (b) Geometry of a planar GaAs Schottky diode chip with integrated contact finger [112].*

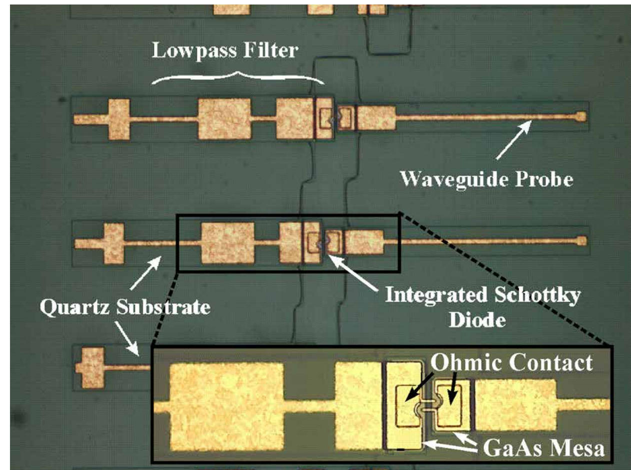
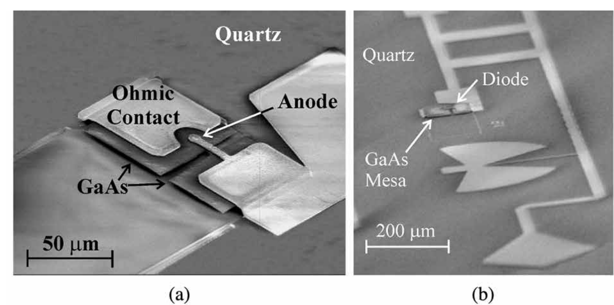


Fig. 18. *Integrated GaAs mixer circuit showing the quartz wafer prior to dicing and illustrating the waveguide probes and filter circuits. The inset shows a GaAs mesa and the antiparallel anode fingers. The background material is the quartz substrate and the GaAs mesas are 3 μm thick [111].*

(300–3000 GHz), serving as the fundamental technology used for heterodyne receivers [111], [114] and frequency multiplier chains [115], [116] that operate in this frequency range. Over several decades, the Schottky diode has evolved from a simple, whisker-contacted geometry [Fig. 17(a)] [117], [118] to a planar chip with integrated finger contact [Fig. 17(b)] [112] and eventually to a fully monolithic component that is amenable to integration on host substrates using epitaxial transfer and bonding techniques [119].

The progression of submillimeter-wave diodes from a whisker-contacted device to a heterogeneously integrated planar device has allowed the development of integrated diode-based circuits that incorporate lithographically defined probes, matching circuits, and associated RF circuitry, resulting in unprecedented levels of performance as well as the realization of complete diode-based submillimeter-wave instruments. The application and potential benefits of heterogeneous integration methods have been well established in the photonics community [120], and various methods for heterogeneous integration of III-V materials on different substrates have been established [121]–[123]. However, their application to implementing submillimeter-wave components is relatively recent.

Initial work on heterogeneously integrated Schottky diodes began at UVA in the 1990s and focused on methods for transferring GaAs epitaxial layers to quartz, which served as a suitable low-loss and low refractive index substrate capable of supporting associated passive circuitry and transmission lines [124]. In this process, the epitaxial transfer is accomplished using a spin-on-dielectric as an intermediate adhesive layer to bond GaAs to the host substrate (quartz). Afterwards, the GaAs superstrate typically is thinned using a combination of dry and wet etching processes in conjunction with an etch-stop layer to form a thin film of GaAs with the required epitaxial stack-up [119]. Subsequently, the GaAs is processed using standard lithographic and etching methods to form isolated mesas and diodes. The final steps of the fabrication process involve formation of the diodes' associated passive circuit structures on the exposed quartz surface (illustrated in Fig. 18) and dicing to separate individual circuits. As an example, Fig. 19 shows a fully integrated phase shifter in which GaAs varactor diodes have been fabricated directly on a quartz-supported circuit using this method of heterogeneous integration to realize a single drop-in chip that is readily mounted to a metallic housing.



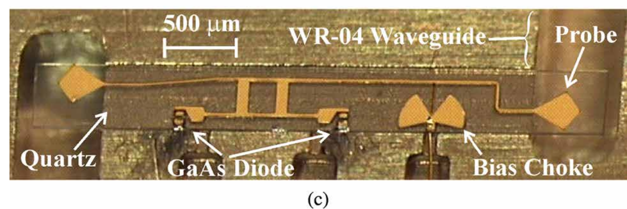


Fig. 19. *A 220-GHz phase shifter integrated on quartz showing (a) the diode, (b) a section of the varactor and integrated circuitry, and (c) the complete phase-shifter mounted to its waveguide housing [124].*

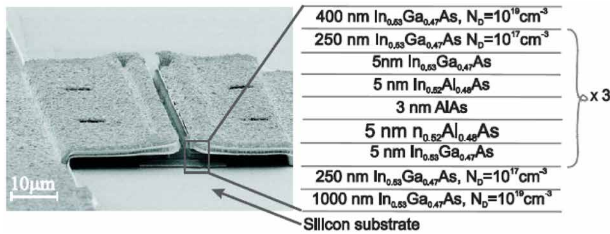


Fig. 20. ***SEM image of an HBV diode integrated on silicon with air bridge connections to the surrounding circuit. The epitaxial layers of the device are provided on the right [125].***

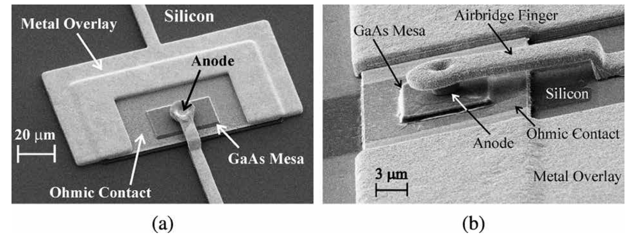


Fig. 21. ***(a) A quasi-vertical Schottky diode heterogeneously integrated on high-resistivity silicon. The ohmic contact of the diode is bonded directly to the silicon and lies beneath the GaAs mesa and anode. (b) A side view of the diode showing the geometry of the anode contact and airbridge finger [126].***

The indirect wafer bonding method described above that utilizes an intermediate adhesive layer to combine different materials to form THz devices and circuits on a suitable integrated substrate has proven robust, but other techniques for heterogeneous integration are also employed and continue to be developed and refined. These methods include direct epitaxial growth [123] as well as epitaxial transfer using direct anodic or plasma-assisted bonding [122].

Most recently, silicon has received considerable attention as an alternative and attractive substrate for integration and packaging of THz components. In comparison to quartz, silicon offers a number of distinct advantages, including superior mechanical strength, higher thermal conductivity, and amenability to postprocessing that permits complex integrated substrate geometries and formation of unsupported beamleads that can be used for electrical connection as well as chip alignment and mounting. Furthermore, high-resistivity silicon (with $\rho > 10$ kΩ·cm) has sufficiently low loss for realizing THz circuits and is readily available in SOI form, thus permitting integration of submillimeter-wave devices on ultrathin (~3 μm) silicon membranes.

The first demonstration of a millimeter-wave component heterogeneously integrated to a silicon substrate is shown in Fig. 20 [125]. This device was formed using low-temperature plasma-assisted wafer bonding to join the InGaAs/InAlAs/AlAs epitaxy to high-resistivity silicon. Subsequently, individual chips were diced and standard semiconductor processing used to form the heterostructure barrier varactor (HBV) diode, a device with symmetric capacitance-voltage characteristic that is used to implement odd-order frequency multipliers.

Building upon this initial demonstration, indirect bonding methods utilizing spin-on-dielectrics have been applied to realize submillimeter-wave Schottky diodes that are heterogeneously integrated to high-resistivity silicon integrated substrates and have been characterized on-wafer to 750 GHz [126]. The devices shown in Fig. 21 illustrate the geometry of these diodes, which have a "quasi-vertical" structure in which the ohmic contact lies directly below the device mesa and anode contact. The formation of such quasi-vertical devices, in fact, is made possible by the epitaxial transfer and bonding process, as the initial fabrication step is deposition and annealing of the ohmic metallization on the epitaxial stack-up of GaAs (n+/n)-AlGaAs-semi-insulating GaAs. Afterwards, the GaAs wafer is attached to the host substrate with the ohmic contact surface bonded to the silicon using a thin layer of spin-on dielectric adhesive. Once bonded to the silicon substrate, the semi-insulating GaAs and AlGaAs etch stop layers are removed, the final device mesas defined, and anode contacts with surrounding circuitry formed using well-established lithography and etching steps [126]. Potential advantages of the quasi-vertical diodes made possible through heterogeneous integration include lower parasitic reactance (as the anode contact is lifted off the substrate, analogous to a whiskered diode) and improved thermal management and grounding (as the bonded ohmic contact serves as an integrated heat sink).

B. Integration of Submillimeter-Wave Multipliers on Micromachined Silicon

Initial applications and demonstrations of heterogeneous integration for chip-scale packaging of submillimeter-wave devices have generally focused on implementing high-order frequency multipliers (quadruplers and quintuplers). Submillimeter-wave sources based on frequency multiplication (or harmonic generation) usually consist of a cascaded chain of components. These cascaded circuits typically require intermediate matching or isolation networks to eliminate undesired interactions between adjacent stages, resulting in increased loss, complexity, and a large geometric footprint. Frequency multipliers, consequently, exemplify a quintessential case where heterogeneous integration methods provide a means for improved packaging and performance of submillimeter-wave components.

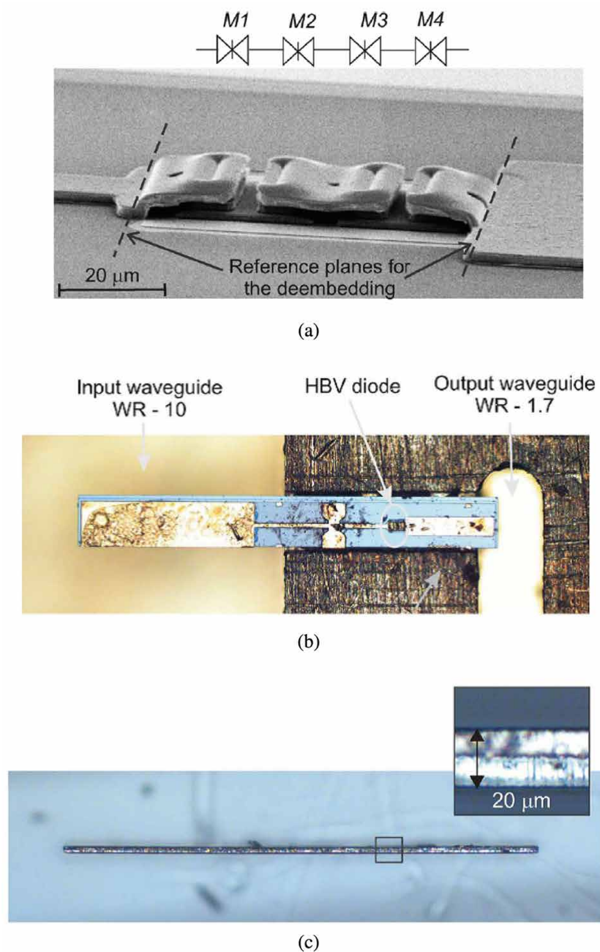


Fig. 22. ***(a) SEM image of a four-mesa HBV diode array bonded to a silicon substrate. (b) Photograph of the complete 474-GHz frequency quintupler chip mounted to a waveguide housing. (c) Sideview of the quintupler chip (dimensions are 1.5-mm length, 0.18-mm width, 0.02-mm thickness) [127].***

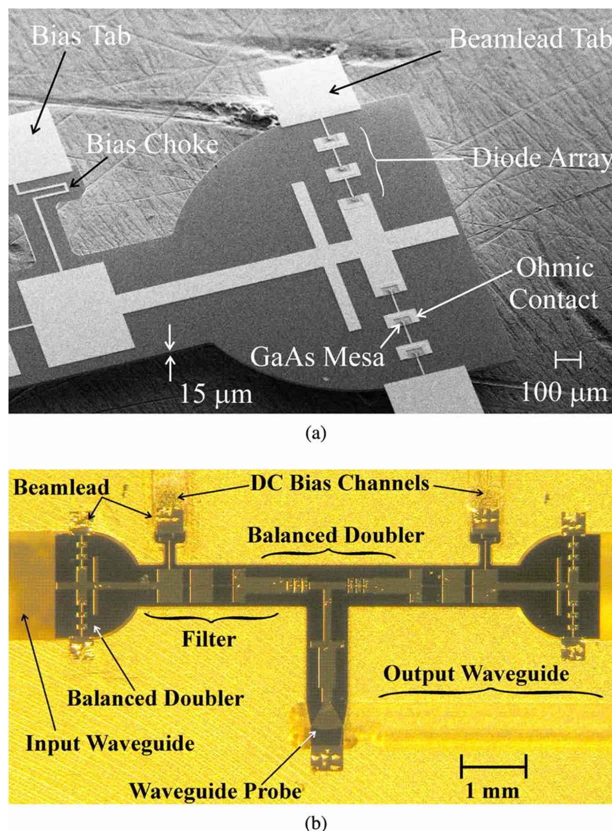


Fig. 23. ***(a) SEM image of the input balanced doubler stage of an integrated 160-GHz frequency quadrupler. (b) Photograph of the complete quadrupler chip mounted to its waveguide housing [128].***

Fig. 22, as an example, shows a submillimeter-wave frequency quintupler that was developed at Chalmers University of Technology using heterogeneous integration of InGaAs/InAlAs/AlAs epitaxy on a thin (20 μm) silicon integrated substrate [127]. This circuit produced an output of 2.8 mW at 474 GHz. The silicon serves as a support membrane for the device as well as substrate for integrated waveguide probes and matching circuits.

The first complete multistage multiplier circuit operating in the submillimeter-wave region and utilizing a micromachined silicon substrate to form an integrated package was developed at the UVA and is shown in Fig. 23 [128]. This multiplier consists of three sets of balanced frequency doublers—a pair at the two input stages that feed a third at the output stage—all integrated onto a single 15-μm-thick silicon integrated substrate chip to form a frequency quadrupler. The silicon integrated substrate supports passive circuitry associated with the quadrupler (intermediate filters and matching networks) in addition to probe waveguide structures. With an input at 40 GHz, the quadrupler shown in Fig. 23 produced an output power of 70 mW at 160 GHz with efficiency of 30%.

Fabrication of the integrated multiplier circuits shown in Figs. 22 and 23 is based on the same fundamental processing steps. The epitaxy needed to form the device initially is transferred to a SOI wafer (using plasma-assisted bonding for the quintupler and a spin-on dielectric for the quadrupler). This is followed by fabrication of the devices and circuits with well-documented and standard processing methods. After the topside circuitry is completed, the SOI carrier is postprocessed to form the final chip geometry. As with the micromachined probes described earlier, this backside process involves mounting the bonded wafers to a temporary carrier and removal of the "handle" silicon and buried oxide, leaving the circuit bonded to a thin silicon substrate membrane. A final extents etch defines the chip geometry and allows individual circuits to be released from the temporary carrier.

It should be noted that a number of the important advantages of silicon as a host substrate are evident in Fig. 23; micromachining of the substrate permits formation of chips

with complex geometries that can be tailored to the dimensions and shape of its housing. Moreover, the circuit shown in Fig. 23 incorporates free-standing gold beamleads that are used to apply bias to the diodes in addition to functioning as alignment and support tabs. This permits complete circuits to be realized as integrated drop-in chips that are readily replaced if needed and are capable of yielding consistent and reproducible performance over multiple rebuilds. Furthermore, the complex geometry and chip size, 7.5 mm in length and 15 μm thick, illustrate the enormous potential of micromachined silicon as a packaging and integration medium for submillimeter-wave and THz circuits.

VI. CONCLUSION

The continued development of THz electronics will require efficient utilization of a variety of material systems such as GaAs for Schottky diodes, InP for THz frequency transistors, and AlN and NbTiN for SIS junctions, among others. In addition, THz metrology systems must enable accurate and robust measurements of the resulting devices, circuits, and systems. This paper has demonstrated that ultrathin silicon membranes, based on a micromachined SOI fabrication process, are able to provide the high-quality and robust substrate required to integrate these technologies together as well as to develop much needed on-wafer probing capabilities. Over the past decade, this process and its variants have been used to develop SIS mixers up to 500 GHz, HEB mixers up to 4.5 THz, high-performance directional couplers up to 500 GHz, on-wafer probes up to 1.1 THz, and 160-GHz quadruplers as well as 474-GHz quintuplers. The ability to heterogeneously integrate MBE quality compound semiconductors onto silicon membranes will continue to enable the higher efficiencies and frequencies for THz systems. In addition, it is straightforward to directly integrate antenna elements on the silicon membrane to facilitate short-range high data-rate communications. Ultimately, for size-critical applications, it may be possible to heterogeneously integrate CMOS with compound semiconductors and antennas to realize complete T-SoCs. ■

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ABOUT THE AUTHORS

N. Scott Barker (Senior Member, IEEE) received the B.S.E.E. degree from the University of Virginia, Charlottesville, VA, USA, in 1994 and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 1996 and 1999, respectively.

In 1999, he joined the Naval Research Laboratory as a Staff Scientist in the Microwave Technology Branch. He is currently a Professor of Electrical and Computer Engineering at the University of Virginia. His research interests include applying MEMS and micromachining techniques to the development of millimeter-wave and terahertz circuits and components. He has over 90 publications and several patents in this field. In 2011, he cofounded the company Dominion MicroProbes, Inc., to develop and market THz frequency technology coinvented by his group at the University of Virginia, including 500–750-GHz and 750–1100-GHz on-wafer probes.

Prof. Barker has served on the IEEE Microwave Theory and Techniques technical committee on RF-MEMS (MTT-21) since 2000 and was the Committee Chair from 2008 to 2011. He has also served on the IMS Technical Program Review Committee since 2001. He served on the Steering Committee of IMS2011 in Baltimore, MD, USA; was the TPC Co-Chair for IMS2014 in Tampa, FL, USA; and is Co-General Chair for IMS2024 in Washington, DC, USA. He served as an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES from 2010 to 2013 and is currently the Editor-in-Chief of the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS. He received the 2012 IEEE MTT-S Outstanding Young Engineer Award, the Charles L. Brown Department of Electrical and Computer Engineering Outstanding Teaching Award in 2015, the New Faculty Teaching Award in 2006, and the Faculty Innovation Award in 2004. He is a recipient of the 2003 NSF CAREER Award and the 2000 IEEE Microwave Prize.

Mathew F. Bauwens received the B.S. and Ph.D. degrees in electrical engineering from the University of Virginia, Charlottesville, VA, USA, in 2007 and 2014, respectively.

In 2013, he joined Dominion MicroProbes, Inc., Charlottesville, VA, USA, as a Senior Engineer. His current research interests include on-wafer probing and submillimeter-wave metrology.

Arthur Lichtenberger received the B.A. degree from Amherst College, Amherts, MA, USA, in 1980 and the M.S. and Ph.D. degrees from the University of Virginia, Charlottesville, VA, USA, in 1985 and 1987, respectively.

He is a Research Professor in Electrical and Computer Engineering at the University of Virginia, and the Director of the UVA Microfabrication Laboratories. He has built an internationally recognized research program in superconducting materials, devices, circuits, and packaging for ultrasensitive single pixel and array THz detectors, having collaborated with astronomical groups for the past 25 years to develop state-of-the-art millimeter and submillimeter wavelength mixers for use on radio telescopes throughout the world. His group?s research includes the investigation of materials and microfabrication technologies for new terahertz devices, circuits, and metrology. To date, he has been PI or Co-PI on over 25 million dollars of funding and an author on over 150 papers. He is a founding member, and the president and COO of Dominion MicroProbes Inc., Charlottesville, VA, USA

Robert M. Weikle, II (Senior Member, IEEE) was born in Tacoma, WA, USA, in 1963. He received the B.S. degree in electrical engineering and physics from Rice University, Houston, TX, USA, in 1986 and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 1987 and 1992, respectively.

In 1993, he joined the faculty of the University of Virginia, Charlottesville, VA, USA, where he is currently a Professor in the Department of Electrical and Computer Engineering. His research group focuses on submillimeter electronics, terahertz devices, high-frequency instrumentation and metrology, and quasi-optical techniques for millimeter-wave power combining and imaging.