INVITED PAPER

Graphene Electronics: Materials, Devices, and Circuits

This paper demonstrates the use of graphene transistors in a four-port RF mixer. This mixer is capable of operating at frequencies up to 10 GHz.

By Yanqing Wu, Damon B. Farmer, Fengnian Xia, and Phaedon Avouris

ABSTRACT | Graphene is a 2-D atomic layer of carbon atoms with unique electronic transport properties such as a high Fermi velocity, an outstanding carrier mobility, and a high carrier saturation velocity, which make graphene an excellent candidate for advanced applications in future electronics. In particular, the potential of graphene in high-speed analog electronics is currently being extensively explored. In this paper, we discuss briefly the basic electronic structure and transport properties of graphene, its large scale synthesis, the role of metal–graphene contact, field-effect transistor (FET) device fabrication (including the issues of gate insulators), and then focus on the electrical characteristics and promise of high-frequency graphene transistors with record-high cutoff frequencies, maximum oscillation frequencies, and voltage gain. Finally, we briefly discuss the first graphene integrated circuits (ICs) in the form of mixers and voltage amplifiers.

KEYWORDS | Current gain; field-effect transistor (FET); graphene analog integrated circuits (ICs); graphene nanoelectronics; power gain; voltage gain

I. INTRODUCTION

Graphene is a 2-D atomic layer of carbon atoms, the building block of the 3-D structure graphite [see Fig. 1(a)]. While graphite has been a well-known and utilized material since antiquity, a single graphene layer was not isolated and studied until relatively recently. Graphene was generated by several different chemical techniques in the 1960s and 1970s, but it was not until 2004 when K. S. Novoselov, A. K. Geim, and coworkers at the University of Manchester (Manchester, U.K.) introduced a simple technique involving the mechanical exfoliation of graphite to isolate single graphene layers [1]. The availability of graphene flakes made the study of its properties possible and led to the enormous interest and intense activity in graphene research currently ongoing [2]–[5].

Graphene is a material with unique electronic transport properties such as a high Fermi velocity, outstanding carrier mobility, and a high carrier saturation velocity. These properties are complemented by excellent thermal conductivity, high mechanical strength, thinness, and flexibility. These characteristics make graphene an excellent candidate for advanced applications in future electronics.

In particular, the potential of graphene in high-speed analog electronics is currently being extensively explored [6]–[15]. In this paper, we discuss briefly the basic electronic structure and transport properties of graphene, its large-scale synthesis, the role of metal–graphene contact, field-effect transistor (FET) device fabrication (including the issues of gate insulators), and then focus on the electrical characteristics and promise of high-frequency graphene transistors and circuits.

II. ELECTRONIC STRUCTURE AND TRANSPORT IN GRAPHENE

The valence electrons of carbon atoms in graphene are sp^2 hybridized with the remaining p_z carbon orbitals forming an extended π-electron system that is responsible for the low energy transport and optical properties of graphene. The carbon atoms are arranged in the form of a hexagonal

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Y. Wu was with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598 USA. He is now with the Huazhong University of Science and Technology, Wuhan, Hubei 430074, China (e-mail: yqwu@mail.hust.edu.cn).

D. B. Farmer, **F. Xia**, and **P. Avouris** are with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: avouris@us.ibm.com).

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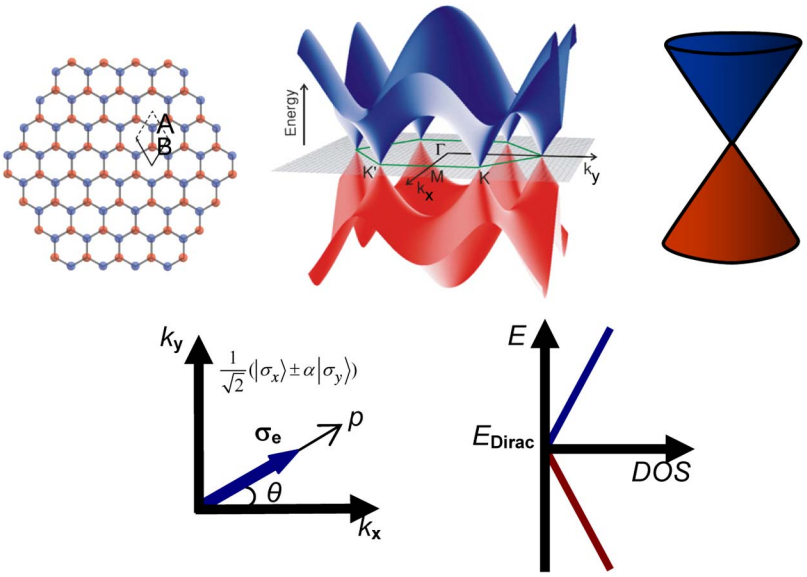

Fig. 1. *Left to right: Graphene lattice, electronic bandstructure, linear dispersion at low energies, pseudospin components, and density of states (DOS) dependence on energy.*

honeycomb lattice with two atoms A and B per unit cell [see Fig. 1(a)]. The electronic bandstructure of graphene was calculated very early on [16], [17], and is shown in Fig. 1(b). The bonding π-states form the valence band and the antibonding π^* states the conduction band. These two bands touch at six points, the so-called Dirac or neutrality points. Symmetry allows these six points to be reduced to a pair K and K', which are independent of one another. If we limit ourselves to low energies, which are the most relevant in electron transport, the bands have a linear dispersion $E = v_F hk$, where v_F is the Fermi velocity. Here, the bandstructure can be viewed as two cones touching at the Dirac point (E_{Dirac}). This behavior is the direct result of the fact that the π and π^* states are orthogonal, and as such, can cross smoothly with no repulsion or bandgap opening. Because of the lack of a bandgap, graphene is usually described as a zero-gap semiconductor, or better yet, as a semimetal. Furthermore, since the bandstructure is symmetric about the Dirac point, electrons and holes in pure, freestanding graphene should have the same properties. The density of states (DOS) is not constant with energy, as in conventional two-dimensional electron gas (2DEG), but rather increases linearly with energy away from E_{Dirac}.

Taking into account the presence of the two graphene sublattices A and B, the Hamiltonian that describes the low energy bandstructure in the vicinity of the $K(K')$ points can be described by a 2-D Dirac relativistic Hamiltonian for massless$*$ fermions $H = hv_F\sigma k$.[1] In this Hamiltonian, k is the wavevector measured relative to the $K(K')$ point and the σ's are Pauli spinor matrices [18]. This Hamiltonian is well known in particle physics where it is used to describe massless neutrinos. In the case of graphene, however, the spinor σ does not describe the particle's spin. It is rather a two-component vector called pseudospin that gives the relative amplitude of the electronic wavefunction on the two sublattices A and B, and always points along the electron momentum k (opposite for holes). If the electron density is all on A, the pseudospin is "up," while if on B, σ is "down." In general, the pseudospin wavefunction is a linear combination of the "up" and "down" states. Physically, the pseudospin describes the character (bonding or antibonding) of the underlying molecular orbital.

Considering now the implications of this bandstructure on the scattering of carriers in graphene, we distinguish two types of scatterers. First, we consider long-range scatterers with $V(q)$, where $q \ll K$, e.g., charged impurites, where the potential is approximately constant on the scale of the lattice constant and, therefore, does not couple to the pseudospin portion of the wavefunction. In this case, the resulting matrix element between initial (k) and final (k') states is given by $\|\langle k'|V(r)|k\rangle|^2 = |V(k - k')|^2 \cos^2((1/2)\theta_{k,k'})$, where $\theta_{k,k'}$ is the angle between them and the cos term represents the overlap of the initial and final spinor states. It is then clear that backscattering in graphene, i.e., the reversal of pseudospin, is forbidden, $\cos^2(\pi) = 0$, because the molecular orbitals of the initial and final states are orthogonal [18]. This absence of backscattering for long-ranged Coulombic and acoustic phonon scattering plays an important role in the excellent electrical transport properties of graphene. On the other hand, short-range disorder with $q \sim K$, e.g., lattice defects

[1]Note that the massless nature of the graphene electrons results from the relativistic relation of the energy, and the fact that the dispersion is linear, which implies that the rest mass m of the electrons is zero.

such as vacancies or foreign atoms, can mix the molecular orbitals and lead to backscattering.

Depending on the strength of the scattering, transport in graphene can be diffusive, ballistic, or intermediate between the two. Record high mobilities (μ) have been achieved in graphene. Early on, μ of the order of 200 000 $cm^2V^{-1}s^1$ was obtained in suspended and annealed samples [19], [20], and even higher μ of the order of 10^6 $cm^2V^{-1}s^{-1}$ has been reported more recently at low temperatures and low carrier densities [21], [22]. These values reflect the properties of nearly isolated graphene. Given that graphene is all surface, it can interact rather strongly with its environment (substrates, ambient atmosphere, etc.) and its properties can, therefore, be significantly affected. There are a number of different types of interactions that affect carrier mobility. An important one in realistic device structures involves charged impurities, either on the graphene itself, or in the underlying/overlaying insulators. The mobility resulting from Coulomb scattering μ_C does not depend on the carrier concentration n, and is not temperature dependent for $k_BT \ll E_F$ As expected, increased screening reduces the strength of Coulombic scattering. In current devices based on synthetic graphene samples, μ_C is typically of the order of 1000–10 000 $cm^2V^{-1}s^{-1}$. The strength of short-range scattering depends on the quality of the graphene sample, where $\mu_S \propto 1/n$, and μ_S is temperature independent at $k_BT \ll E_F$ [23]. Interestingly, increased screening enhances the importance of short-range interactions.

Acoustic phonon scattering is rather weak in graphene with $\mu_{Ph} \propto 1/nT$ [24], thus allowing mobilities $>$ 100 000 $cm^2V^{-1}s^{-1}$. Furthermore, the optical phonon energy of graphene is much higher than that in conventional semiconductors $\sim$200 meV, and thus optical phonon scattering is not important at low energies. Another phonon scattering mechanism that needs to be considered in supported graphene, however, involves the surface phonon modes of polar insulator substrates/overlayers. These surface phonon polaritons (SPPs) generate an electric field that couples with and scatters the carriers in the graphene channel. This SPP mechanism has an activated temperature dependence, determined by the phonon frequencies of the insulator [25], and can dominate the mobility of very pure samples. Other scattering mechanisms that involve structural features of the graphene will be addressed in Section VII.

Intrinsic graphene exhibits unique electrical characteristics, however, environmental interactions and high carrier densities present in working devices can significantly impact these characteristics due to the scattering mechanisms outlined above. The aim of current graphene research is to improve the graphene material quality and control the interactions so as to optimize device performance.

Given that graphene does not have a bandgap, electrostatic confinement and inhibition of transport through graphene is rather weak. A graphene field-effect transistor (GFET) cannot be turned off completely, even though DOS $= 0$ at the Dirac point (E_{Dirac}). A residual conductivity, the so-called minimum conductivity, remains [26]. This conductivity was originally thought to have a universal value of $G_{min} = 4e^2/\pi h$, but we now know that it depends on the concentration of defects and the structure (width/length ratio) of the device [23], [27]–[29]. The fact that the current in the graphene channel cannot be completely turned off by a gate limits the GFET's ON/OFF ratio. At ambient conditions, this ratio is typically less than 10, the exact number depending on the quality of graphene and the effectiveness of the gating. Therefore, in its pristine form, a graphene layer cannot be used as the channel in digital FETs. However, given its excellent transport properties, it is a promising candidate for high-frequency [radio-frequency (RF)] electronics, the main subject of this paper.

III. GRAPHENE SYNTHESIS

While the facile isolation of graphene by graphite exfoliation [1] gave the impetus for the development of the graphene field, and much of the basic science on graphene was performed on such exfoliated graphene flakes, technology requires the controlled, large-scale synthesis of graphene. For most applications in electronics technology, one needs to have large-scale graphene on an insulating substrate, with the wafer form being ideal. Currently, two basic types of large-scale synthesis of graphene are utilized. One is based on the thermal decomposition of SiC [30], [31]–[34]. By heating SiC wafers, typically in the presence of an argon background, to temperatures around 1500 °C, Si desorbs and the remaining carbon rebonds to form graphene on top of the insulating SiC substrate. Both the growth rate and the characteristics of the resulting graphene depend on the exposed SiC face, silicon or carbon. Growth is much faster on the C face, typically leading to multilayer graphene, which becomes p-doped after exposure to the environment (water and oxygen). Si-face growth is slower and, therefore, more controllable, and the graphene is intrinsically n-doped. This n-doping arises from charge transfer from the Si-rich underlayer, the so-called buffer layer. This effect can be eliminated by hydrogen treatments at high temperatures, which saturate the Si dangling bonds [35]–[37].

Another widely used synthesis approach involves the growth of graphene on metals. There are two main mechanisms by which this growth can proceed. One involves catalytic metals such as (Ni, Ru, Fe, Ir), which can dissociate carbon precursors (e.g., CH_4, C_2H_2) and dissolve significant amounts of carbon at high temperatures [38]–[41]. Upon cooling, the carbon segregates to the metal surface as graphene. The other approach is a catalytic chemical vapor deposition (CVD) process where the precursor is decomposed at elevated temperatures ($>$ 1000 °C) on a metal which has very limited solubility for carbon. In most cases the metal used is copper [42], [43]. This technique is essentially self-limiting, yielding monolayer graphene. Its key advantage

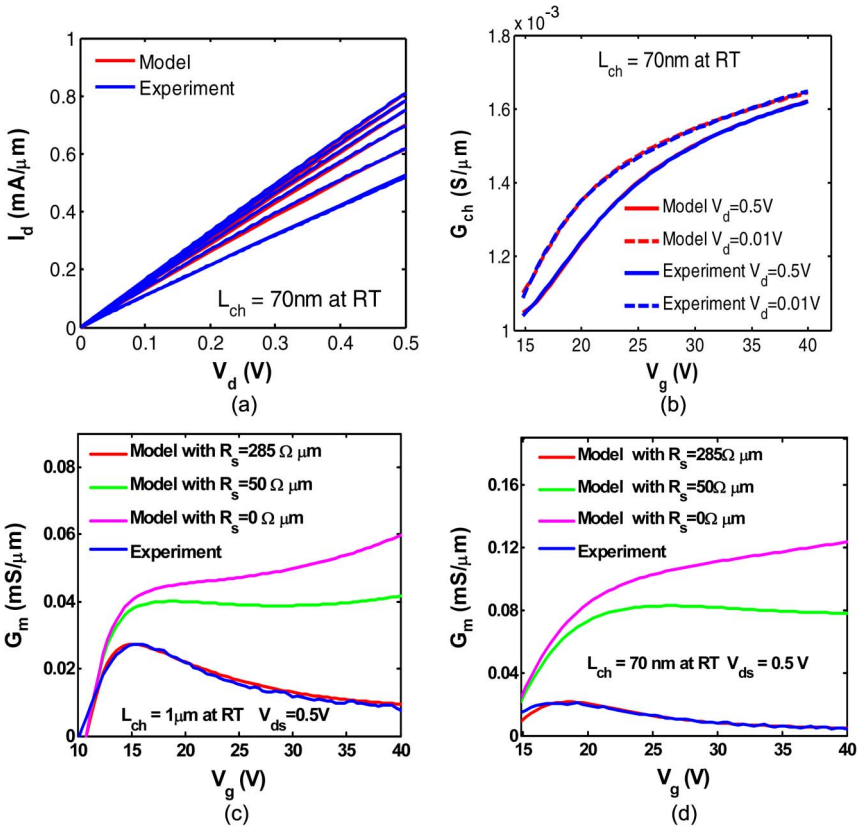

Fig. 2. *(a) Experimental output characteristics and simulations for a 70-nm device at room temperature. Back-gate voltage V_g is swept 25 V from the Dirac point with a step of 5 V. (b) Comparison of the measurements and the simulations of the transfer characteristics of the 70-nm device at room temperature. (c) and (d) Modeling of G_m by varying R_s for 1-μm and 70-nm devices, respectively. More than four times improvement of G_m can be achieved for the 70-nm device. Figures reproduced from [11].*

is that the resulting monolayer can be transferred to any substrate after the dissolution of the Cu, thereby expanding the possible applications of graphene.

IV. CONTACT RESISTANCE AND ITS IMPACT ON CHANNEL LENGTH SCALING

Early studies of transport in graphene used Hall-bar structures in order to exclude many extrinsic influences. Intrinsic graphene electronic properties such as ultrahigh mobilities have been obtained by reducing external perturbations such as contacts with metal and dielectric materials. However, a complete understanding of the entire graphene device with all of the necessary external components is essential for the development of a graphene technology. We will, therefore, dedicate a large portion of our discussion here to these external influences. Furthermore, as in Si complementary metal–oxide–semiconductor (CMOS) devices, it is very important to study how graphene devices behave when the channel lengths are scaled down. In particular, since there is currently no viable way of reducing the contact resistance while scaling down the channel length, it is especially important to study short-channel graphene devices where the contact resistance and contact-induced doping may dominate the transport.

To analyze the performance of short-channel graphene devices, we adopted with the appropriate modifications the "virtual source" model [44]–[45], which was originally used for short-channel Si metal–oxide–semiconductor field-effect transistors (MOSFETs).

The analytical approximation for the charge density near the virtual source was expressed as $Q_{ixo} = \sqrt{Q_p(n_0)^2 + (C_g(V_{GS}^* - V_{T0} - \delta V_{DS}))^2}$, where Q_p is the charge from the residual doping n_0, C_g is the gate dielectric capacitance, V_{T0} is the gate voltage at the Dirac point, and δ is the rate of the Dirac point voltage change with applied drain biases (typically between 0.5 and 1). Thus, the drain current can be expressed as $I_D/W = Q_{i,x0}v_{x0}F_{\text{sat}}$, where v_{xo} is the virtual source velocity, and F_{sat} is an empirical saturating function. The details of the modeling can be found in [11].

This model can account satisfactorily for the behavior of graphene devices with different channel lengths, as

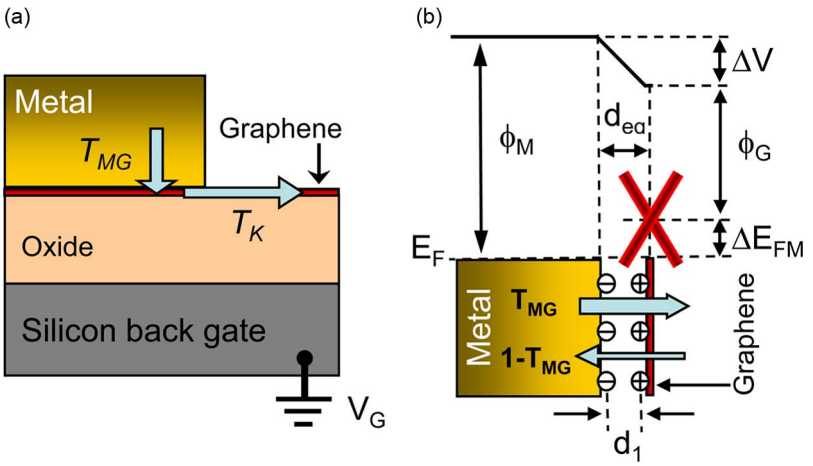

Fig. 3. *(a) Schematic diagram of charge carrier injection from metal electrodes to graphene and into the graphene channel with transmission coefficient T_{MG} and T_K, respectively. (b) Work function differences and Fermi energy misalignment between the metal and the graphene creates a dipole barrier at the interface (d_{eq}). Carriers are transmitted through the resulting barrier with probabilities T_{MG}. Figures reproduced from [46].*

shown in Fig. 2(a) and (b). In order to further understand the impact of contact resistance for the short-channel graphene devices, we use the parameters from the previous fitting, and model the device performance using different contact resistances for two channel lengths. As can be seen from Fig. 2(c) and (d), the longer channel 1-μm device shows only a slight improvement of the peak transconductance (g_m) of less than twice if the contact resistance is reduced to 50 $\Omega\mu$m. However, the improvement of g_m for the short-channel 70-nm device is more than four times with the same contact resistance reduction. It is obvious from this modeling that the overall device performance depends critically on the contact resistance value, and a major effort should be focused on improving it in short-channel devices.

V. PHYSICS OF METAL–GRAPHENE CONTACT

While the above analytic model is useful in demonstrating the importance of contact resistance in short-channel devices, it does not provide a fundamental understanding of its origin. As a 2-D material, graphene is very sensitive to its environment. Indeed, with no effective body thickness, all electronic transport through graphene occurs at its surface.

As a result, materials that come into contact with the graphene surface, such as metal electrodes and gate dielectrics, can have a dramatic impact on the transport behavior. Appropriate material selection is, therefore, of the utmost importance in graphene devices. The injection of charge carriers into graphene from the contact electrodes is necessary to establish a current in the device. For enhanced device operation, it is desirable for this injection to be as efficient as possible. Charge carriers that are to be injected into a graphene channel in a FET are confronted by two barriers. The carriers must first travel from the electrode to the underlying graphene in contact with the electrode. Any work function difference between the graphene and the electrode will result in charge transfer, which creates an electrostatic barrier in the form of a dipole layer at the graphene/electrode interface [Fig. 3(a)]. This barrier can be minimized by using an electrode material that: 1) has a work function that matches the Fermi energy of the contacted graphene; and 2) favorably wets the graphene surface to make smooth contact. Some of the best results in terms of low contact resistance that have been attained to date have used palladium electrodes. Here we define the carrier transmission coefficient from the metal to underlying graphene as T_{MG}. Once injected into the contacted graphene, the charge carriers must next travel out from under the electrode into the channel region. The interface between these two regions constitutes another electrostatic barrier due to charge transfer doping inhomogeneity, and an effective p–n junction may be formed here [Fig. 3(b)]. The nature of transmission with a coefficient of T_K through this barrier depends on the barrier shape, where charge carriers are transmitted more efficiently through sharp barriers (due to Klein tunneling) than more gradual barriers [46].

Critical to the understanding the transmission of carriers through the contacts and the effect of the gate in graphene FETs is the understanding of the tunneling through graphene p–n junctions. Tunneling through such junctions is basically an interband (valence to conduction) process, and unlike typical Zener interband tunneling in semiconductors, graphene has zero bandgap. The relativistic description of graphene allows a description of this

tunneling analogous to that of Klein tunneling of relativistic particles [47], [48]. The exact tunneling behavior depends on whether the barrier potential is sharp ($w \ll \lambda_F$) or smooth, ($w \gg \lambda_F$) on the scale of the Fermi wavelength, and the angle of incidence of the particle to the potential barrier [49], [50]. For normal incidence on a sharp (e.g., square) barrier, the transmission coefficient $T(\theta)$ is unity, i.e., the transmission is perfect. This is a direct result of pseudospin conservation and the absence of backscattering. For oblique incidence, on the other hand, $T(\theta \neq 0) < 1$. In this case, tunneling is restricted by classically forbidden regions, and the transmission has a $\cos^2(\theta)$ angular dependence. For a smooth barrier at oblique incidence, the interband tunneling is given by $T(\theta) \approx \exp[-\pi \hbar v_F k_F^2 \sin^2(\theta)/F]$, where F is the gradient of the potential barrier at the Fermi energy.

Regardless of the characteristics of the electrostatic barriers in the device, carrier transmission is ultimately dependent on the number of conduction modes (states) that are available to carry current. In graphene, the minimum number of conduction modes is found at the Dirac point, where the resistance is theoretically infinite but always possesses a finite value in actuality, due to potential fluctuations along the graphene surface (electron/hole puddles) [26].

As a result, the contact resistance is highest when the Fermi energy of the electrode coincides with the Dirac point energy of graphene. This can be seen in Fig. 4(a), where the contact resistance is plotted relative to the gate voltage of a graphene FET. The resistance is indeed highest when this voltage is equal to the Dirac voltage. Contact resistance in graphene is unique in that it decreases with decreasing temperature, as seen in Fig. 4(b) for different global gate voltages (electrostatic doping levels). While still in need of further study, it is suggested that this effect is due to the relationship between the characteristic coupling length (λ_m) of the charge carrier with the electrode and the mean free path (λ_{mfp}) of the charge carrier. When $\lambda_{\mathrm{mfp}} \gg \lambda_m$, transmission from the metal to the graphene is facile, resulting in a relatively low contact resistance. This inequality is strongest at low temperature, when carrier scattering with phonons is minimized and the mean free path can subsequently increase.

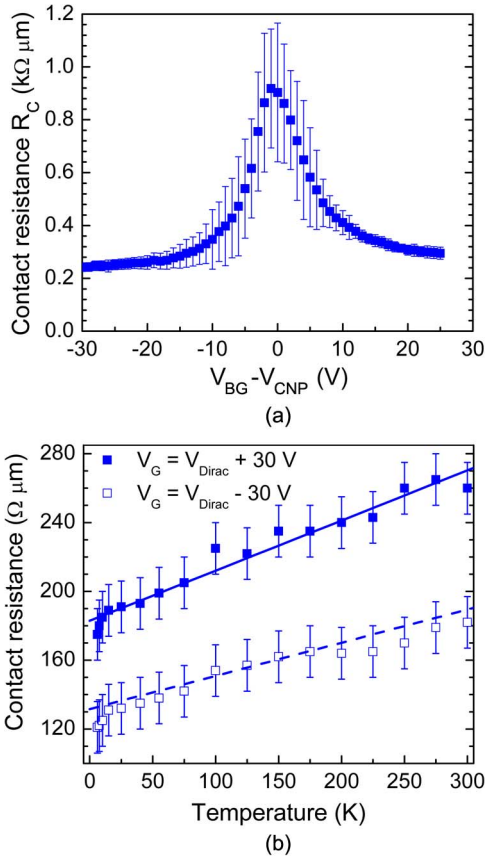

Fig. 4. *(a) Contact resistance of a palladium–graphene contact determined using the transfer length method (TLM) for a set of FET arrays at room temperature. (b) Measured palladium–graphene contact resistance as a function of temperature at gate biases of $V_{\mathrm{Dirac}} - 30$ V and $V_{\mathrm{Dirac}} + 30$ V, showing a systematic improvement of contact resistance when temperature decreases. Figures reproduced from [46].*

VI. GRAPHENE HETEROJUNCTIONS INDUCED BY METAL CONTACTS

The metal–graphene contact not only impacts the value of contact resistance, but also plays an important role in the whole process of transport, especially in short-channel devices. For a typical graphene FET device, transport can be described [51] as consisting of five distinct regions, as shown schematically in Fig. 5(a). As outlined above, when injected from the source region, the carriers first need to travel through the metal–graphene interface where a junction is formed (region I), the detailed profile of the junction being determined by the metal work function, the way the metal was deposited, the graphene mobility, and its original doping. The transmission efficiency here is denoted as T_{MG}. Carriers exiting from the metal–graphene junction in region V encounter a similar situation as in region I. Doped by the charge transfer from the metal contact (in this case, Pd), the graphene underneath the electrode forms a p–n or p–p' junction with the graphene in the channel at regions II and IV. This contact junction width is largely determined by electrostatic nonlinear screening in graphene rather than by the oxide thickness alone [52], [53], and does not exceed a few nanometers. Carriers can then experience various scattering events during transport through region III, where the main graphene channel lies. The channel scattering rate is determined by the ratio of the channel length L_{ch} and the mean free path λ_{mfp}. If L_{ch} can be made short enough so that the channel transport is ballistic, then the junctions formed at the source side (region II) and drain side (region IV) can be viewed as a

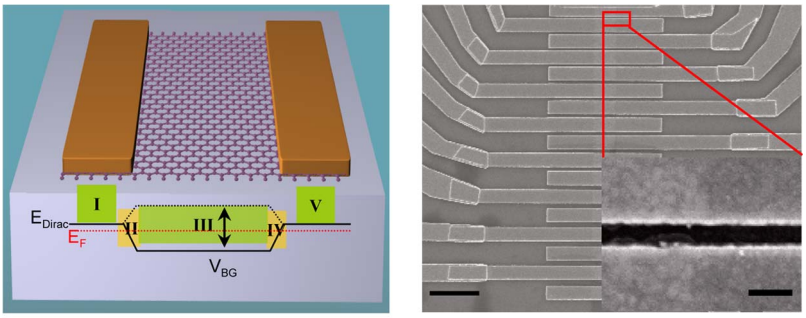

Fig. 5. *(a) Schematic view of a bottom-gated graphene transistor and the potential profile divided into five regions. (b) Scanning electron microscope (SEM) image of an array of bottomed-gated graphene device with different channel lengths (scale bar: 2 μm). Inset: SEM image of a 50-nm channel length device (scale bar: 100 nm). Figures reproduced from [51].*

ballistic p–n–p or p–p'–p junction, controlled by the gate voltage.

To obtain more insights into the role played by the contacts in the performance and scaling behavior of graphene transistors, we studied a series of such devices with different gate lengths. The gate length varied from 500 nm down to 50 nm, as shown in the SEM images in Fig. 5(b).

As may be expected from the symmetric bandstructure of graphene, Hall-bar structures exhibit symmetric electric currents for the electron and hole branches, when the mobilities are similar in both branches. However, asymmetric electric currents for electrons and holes are always observed in a two-terminal configuration. As will be discussed further, contact-induced doping is the main reason for this effect, which becomes more obvious in shorter channel devices. To quantify the effect of contact doping, the odd part of the total device resistance $R_{\text{odd}} = (R_n - R_p)/R_p$ is used to characterize the diffusive transport in graphene devices [54]. Typical ambipolar transport results for graphene transistors with three different channel lengths are shown in Fig. 6(a) and (b) at room temperature and 4.3 K, respectively. It is clear that the resistance asymmetry induced by the contact metal is increasing as the channel length decreases, and it is maximized at the shortest channel where transport is expected to be ballistic, as shown in Fig. 8(a).

Moreover, the resistance of the shortest channel length device (50 nm) shows characteristic oscillations analogous to the Fabry–Perot oscillations in optical cavities confirming that the transport is at this point phase coherent [see Fig. 7(a) and (b)]. From the period of the oscillations, we can extract the cavity length, which we find to be very close to the physical channel length. This shows that nonlinear screening in graphene is effective and the resulting junction barrier width is short. Previously, such quantum oscillations were demonstrated in graphene heterostructures using complex fabrication techniques such as ultranarrow top-gate structures, and the effective resonance cavity is largely determined by the top-gate dielectric [55]–[57]. Furthermore, good agreement between the observed resistance asymmetry [Fig. 8(a)] and theoretical modeling can only be achieved by allowing the Fermi level to vary for the graphene underneath the metal, implying an, at least partially, unpinned Fermi level under palladium. The ability to modulate the Fermi level for graphene under metal by the back gate provides extra freedom of tuning the barrier shape (width and angle) of the resulting heterojunctions.

It can also be seen from Fig. 8(b) that the ON/OFF ratio of the graphene FETs deteriorates more rapidly for the smaller channel devices. The larger ON/OFF ratio for p-FET is attributed to the high work function palladium metal used for contacts, which shows the importance of choosing the appropriate metal for the particular polarity of the transistor. The ON/OFF ratio decreases for smaller channel length devices and can be mainly attributed to the increasingly more

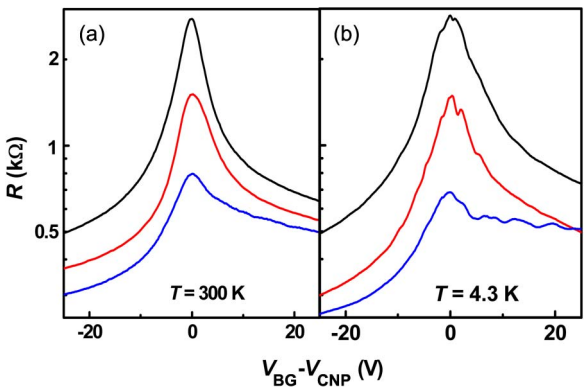

Fig. 6. *(a) Total resistance versus back-gate voltage sweep relative to the charge neutrality point for three different channel lengths: 500 nm (black line), 170 nm (red line), and 50 nm (blue line) at room temperature and at 4.3 K (b). Figures reproduced from [51].*

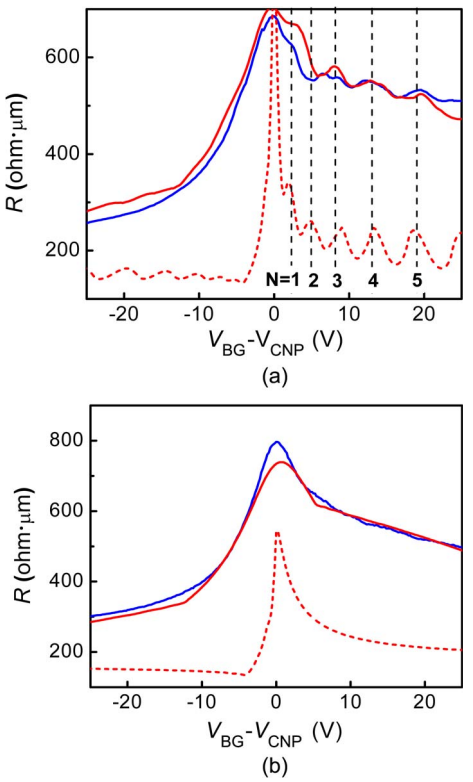

Fig. 7. *Experimental and theoretical analysis for ballistic short-channel graphene devices. (a) Resistance versus the relative back-gate voltage for a 50-nm device at 4.3 K. Experimental data (blue curve) and ballistic modeling using: (1) a channel length $L_{ch} = 52$ nm, a Fermi level in graphene under the metal pinned at $V_O = 100$ meV, and transparent metal to graphene junctions (red dashed line); and (2) using a nonideal graphene metal barrier with $T_{MG} = 0.36$, the Fermi level under the metal described by an electrostatic model with a metal to graphene distance $d_1 = 1.3$ Å, and electron–hole puddles with npd $= 1.1 \times 10^{12}$ cm^{-2}, and $V_{pdM} = 150$ meV (red solid line). (b) Same as (a) at 300 K: experiment (blue), model 1 (red-dashed), model 2 (solid red). Figures reproduced from [51].*

important role of the contact resistance and the transport mechanism, which switches from diffusive to ballistic. In the diffusive transport limit, the current is linearly dependent on the carrier density in the graphene channel, while in the ballistic regime, the current has a weaker carrier density dependence of square root of carrier density. It is thus important to understand the origins and limits of the metal–graphene contact in order to further improve it, and it is especially important for the deeply scaled graphene devices where the transport is dominated by the contacts.

VII. GRAPHENE TRANSPORT WITH PARASITIC EFFECTS

As the channel length becomes shorter, the effects of the parasitic resistance associated with the length of the channel between the source/drain edge and the gate edge [access length, Fig. 9(a)] become more prominent. It is crucial to minimize this access length and the associated resistance as much as possible for an effective gate length scaling. This is conventionally done by self-aligned gating, where the source/drain and gate electrodes are automatically positioned so that no overlap or significant gap exists between them. This is routinely done in Si CMOS technology through ion implantation. However, both implantation and plasma etching techniques would inevitably damage the fragile, single-layer graphene. Alternative self-alignment techniques for graphene technology are therefore needed. Self-aligned gated structures have been realized in graphene transistors by shadow masking with nanowire gates or metal T-gates [10], [58]. They have also been formed by exploiting the inherent nucleation inhibition of atomic layer deposition (ALD) material on graphene to form insulating spacers on the sidewalls of the gate stack while leaving the source/drain regions electrically accessible [59]. The resulting structure allows for self-aligned source/drain formation. As an example, the output characteristics of a self-aligned graphene device with a channel length of 1 μm is shown in Fig. 9(a). The

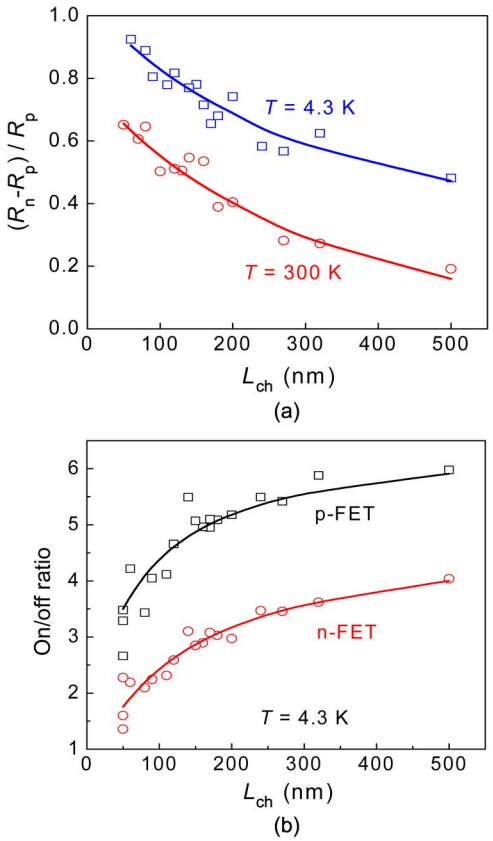

Fig. 8. *(a) Resistance asymmetry versus channel length at room temperature (red circles) and at 4.3 K (blue squares). (b) Current ON/OFF ratio versus channel length at 4.3 K for n-FET (red) and p-FET (black). The lines are to guide the eye. Figures reproduced from [51].*

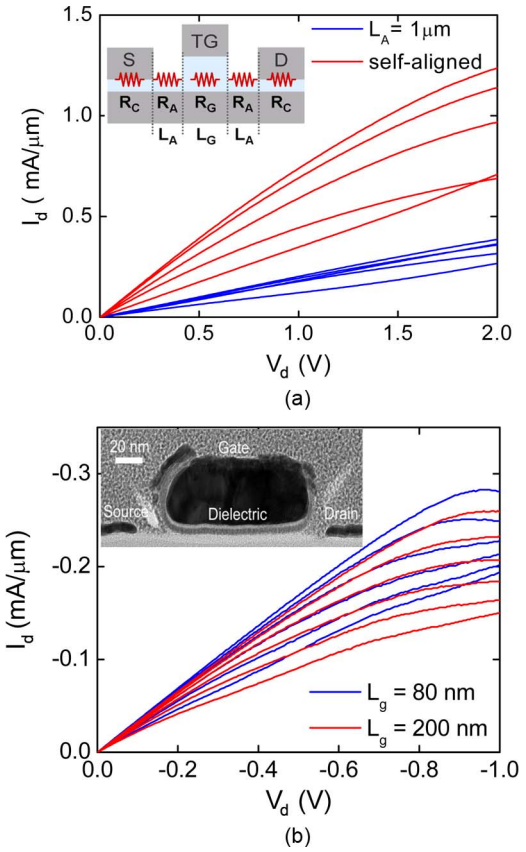

Fig. 9. ***(a) Comparison of output characteristics of a self-aligned and non-self-aligned graphene transistor with $L_A = 1$ μm. Both transistors have identical gate lengths of 1 μm. Inset: schematic diagram of the basic dimensions and corresponding resistances in a graphene transistor with source (S), drain (D), top gate (TG), contact resistance (R_C), gate length and resistance (L_G and R_G), and access length and resistance (L_A and R_A). Figures reproduced from [59]. (b) Representative output characteristics of two graphene transistors that were fabricated using a self-alignment process with $L_G = 200$ nm (red) and $L_G = 80$ nm (blue). The output current is observed to saturate in both cases. Inset: corresponding cross-sectional transmission electron microscopy (TEM) image of a graphene transistor with $L_G = 80$ nm and $L_A = 15$ nm. Here, the dielectric sidewall spacers can be seen on either side of the gate electrode.***

output current of this structure is about three times higher than that with an access length of 1 μm [59].

Recently, we devised a way to achieve self-aligned devices with sub-100-nm gate lengths using conventional CMOS processing techniques. The graphene surface is coated with lithography resist and the gate is patterned into this resist layer. After appropriate seeding of the exposed graphene surface to facilitate dielectric nucleation, a gate dielectric is deposited by ALD. This film coats the graphene and the resist pattern uniformly (top surface and sidewalls of the resist). A gate metal is then deposited on top of the dielectric layer and liftoff is performed. The end result is a gate stack structure consisting of insulating sidewall spacers formed during the ALD process. These spacers offer electrical insulation from the self-aligned source/drain electrodes, which are subsequently deposited by electron-beam evaporation. Self-aligned graphene transistors with gate lengths as short as 80 nm have been demonstrated by this process [Fig. 9(b)].

After carriers are injected from the contact electrodes, traversing the potential barriers through available modes as described above, they enter the graphene channel, where additional extrinsic impediments to current flow exist. The origin of these scattering centers is associated with the materials used to encapsulate the channel, i.e., the supporting substrate below the channel and the gate dielectric above the channel. Carrier mobility in graphene has been found to be the highest, on the order of 100 000 cm^2/Vs or higher at carrier densities around 10^{12} cm^{-2}, when it is suspended and current annealed to desorb adsorbates. However, such a configuration is not practical for technological applications. Graphene must, therefore, lay on a supporting substrate, where the resulting contact inevitably introduces scattering effects such as long-range Coulomb scattering by charge impurities on or near the substrate surface and remote interfacial phonon scattering with phonon modes associated with the substrate material.

The extent to which these effects degrade the carrier mobility in graphene depends on the quality and properties of the substrate material in question. For instance, Fig. 10(a) compares the carrier mobility in graphene devices on two different substrates, one on SiO_2 and the other on a polyhydroxystyrene-based polymer (NFC). It is clear from this comparison that the nature of scattering on these two surfaces is different. Coulomb scattering dominates the transport behavior when graphene is on the SiO_2, as seen by the temperature invariance of the mobility. This is in stark contrast to graphene that is on the polymer, which comparatively reduces Coulomb scattering, allowing for higher mobilities to be attained. Here, a pronounced temperature dependence is exhibited, suggesting phonons as the dominant scatterer [60]. In the case of epitaxial graphene, charge traps can exist in the SiC substrate, which can reduce the mobility by trapping and scattering. This is shown in Fig. 10(b), where the mobility is observed to decrease with increasing temperature. A more thorough study of this effect reveals that the corresponding carrier density exhibits an activated Arrhenius-type behavior with a characteristic activation energy of 70 meV. This indicates the presence of charge traps on or near the SiC surface [61]. Recently, a novel substrate of hexagonal boron nitride (hBN) has been adopted as the supporting substrate for graphene FETs with minimized substrate scattering and improved RF performance [62].

The carrier mobility can also be influenced by the morphology of the supporting substrate. For example, epitaxial graphene typically has a step-like morphology, a

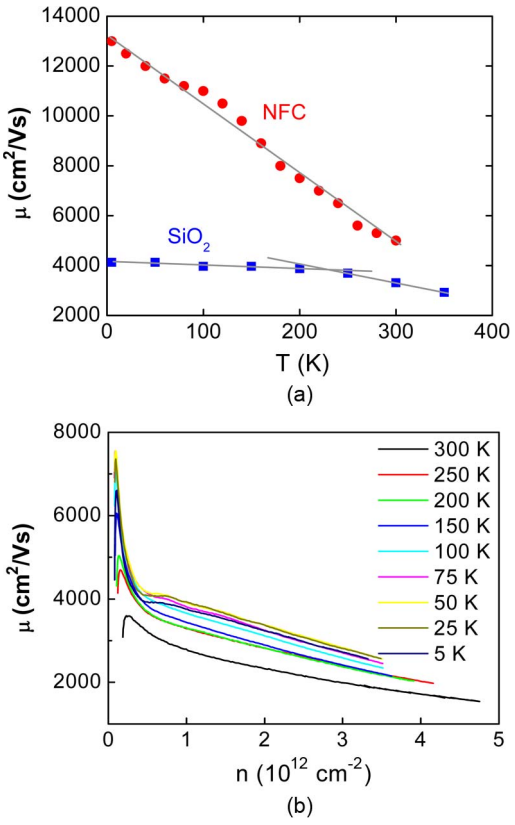

Fig. 10. *(a) Comparison of the temperature dependence of the carrier mobility in graphene transistors that are fabricated on two different types of substrate surface: NFC polymer and SiO_2. Figures reproduced from [60]. (b) Temperature dependence of the carrier mobility in an epitaxial graphene transistor at different carrier densities. Figures reproduced from [61].*

byproduct of the SiC miscut angle and the graphene growth process. Though the graphene is continuous over these step edges, these edges represent regions of higher resistance [63]. This is partly due to elastic deformation of the graphene, but it is mostly a result of p–n junctions that are formed by inhomogeneous doping by the SiC substrate as the graphene pulls away from the step edge. As with p–n junctions created by the contact electrodes, charge carriers must transverse these potential barriers, and their mobility subsequently decreases. When fabricating devices on epitaxial graphene, the relative orientation between the device channel and the step location must, therefore, be taken into account in order to achieve optimal device performance. For example, a substantial increase in the cutoff frequency is obtained by aligning channels with the surface steps, so that the current flow does not cross any surface steps [64]. Similar behavior has also been observed in devices based on CVD graphene [65], [66]. One choice of substrate for CVD graphene RF–FETs is diamond-like carbon (DLC). DLC is chosen as a substrate because of its high thermal conductivity, chemical inertness, and high phonon energy, all which are desirable to maintain high transistor performance.

Since graphene transistors are gated devices, the other side of the graphene surface, the side not in contact with the substrate, must be coated with gate dielectric material. Coating graphene with thin dielectric layers is a nontrivial process. This is due to the fact that graphene is a fully bonded structure, and as such is very inert to conventional dielectric deposition processes. Moreover, since graphene is very sensitive to its material environment, any attempt to make the surface more amiable to coating processes will most likely have a deleterious effect on its electronic properties (particularly the carrier mobility). Research in this area is ongoing, but several processes have already been established that allow for the uniform deposition of thin dielectric films with workable amounts of mobility degradation. Detailed discussion of these processes is beyond the scope of this paper and can be found elsewhere [67]. However, a few representative examples of RF device characteristics with different gate dielectric materials are discussed in Section VIII. Because of the as-prepared graphene, film is typically doped, depending on the growth mechanism and the subsequent process steps. Using dielectrics to compensate these doping effects should result is improved device performance. For example, an Al_2O_3 stack which brings in n-doping can be chosen for typically p-doped CVD graphene, while a plasma-enhanced CVD grown Si_3N_4 dielectric which is p-doped [68] can be used for the typically n-doped Si-face epitaxial graphene. The Dirac point can be shifted to close to zero with such appropriate dielectric choices. Furthermore, continued scaling of the thickness allows for more favorable transconductance and output conductance properties to be attained and, hence, better device performance to be achieved.

VIII. HIGH-FREQUENCY GRAPHENE TRANSISTORS

Transistors suitable for high-frequency measurements have been fabricated on large-area graphene grown both epitaxially and by CVD [13], [37]. Typical RF transistors have a coplanar G–S–G structure with a channel width of 20 μm. As can be seen from the SEM and TEM images in Fig. 11(a) and (b), good alignment can be realized by e-beam lithography, even for transistors with gate lengths of 40 nm. This alignment eliminates most of the overlap capacitance, which can impact the high-frequency performance of graphene devices, especially for those small channel ones. On-chip open and short structures with exact design of the devices were used to de-embed the parasitic effects such as pad capacitance and interconnection resistance. A commonly used de-embedding procedure using "open" and "short" structures is adopted to obtain the intrinsic RF performance. The de-embedding mainly follows this equation: $Y_{\text{transistor}} = [(Y_{\text{DUT}} - Y_{\text{open}})^{-1} - (Y_{\text{short}} - Y_{\text{open}})^{-1}]^{-1}$. The RF results of the devices in Fig. 11 are shown in Fig. 12, as will be discussed in the same section.

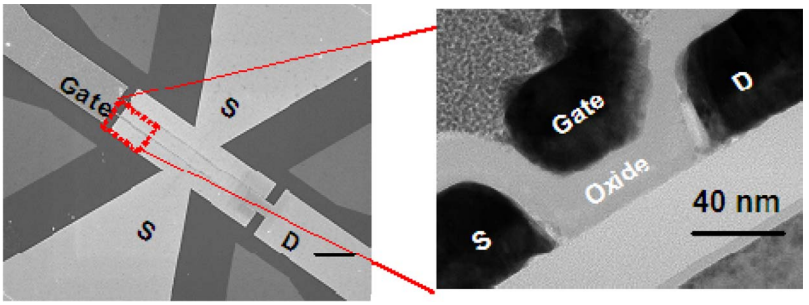

Fig. 11. *(a) SEM image of a typical top-gated dual-channel graphene RF device (scale bar: 3 μm). (b) Cross-sectional TEM image of a graphene transistor with a gate length of 40 nm. (scale bar: 40 nm). Figures reproduced from [13].*

The RF devices are based on CVD graphene and transferred to a DLC substrate. For the purpose of doping compensation, we adopt a gate oxide stack consisting of a layer of oxidized Al and subsequent Al_2O_3 grown by ALD [69]. As was discussed in Section VII, the choice of gate oxide is a vital component of the resulting device performance. This oxide stack leads to a high electron doping of graphene, which shifts the Dirac point to negative V_g.

From the measured S-parameters of the device, the current gain (h_{21}) expressed as $h_{21} = -2S_{21}/((1 - S_{11})(1 + S_{22}) + S_{12}S_{21})$, has been obtained and is plotted against the measurement frequency in Fig. 13(a) and (b). It is seen that the current gain of these devices exhibits the well-behaved $1/f$ (-20 dB/dec) dependence on the frequency for all gate lengths. The temperature dependence of the cutoff frequency has also been measured and is shown in Fig. 12(a). Almost no degradation of this frequency is observed. Therefore, unlike in the conventional MOSFETs, graphene transistors have the advantage of maintaining their performance even in very low temperatures, without suffering from a carrier freeze-out effect. This property makes them promising candidates for operation in extreme environments such as outer space. The dependence of f_T on the device transconductance is shown in Fig. 12(b). As expected from the relation $f_T = g_m/2\pi C_{ox}$, all three data sets fall nicely onto one linear curve, verifying the reliability of the RF and dc measurements.

Despite the fact that good RF performance can be achieved using the above oxide stack, it is even better to use an oxide stack that introduces minimal external doping. This is because the peak transconductance usually occurs near the Dirac point, where the carrier density is not too high and transport is not contact limited. Moreover, as we have discussed elsewhere [70], the ambipolar characteristics and small Dirac voltage shift are essential for good saturation. High transconductance and

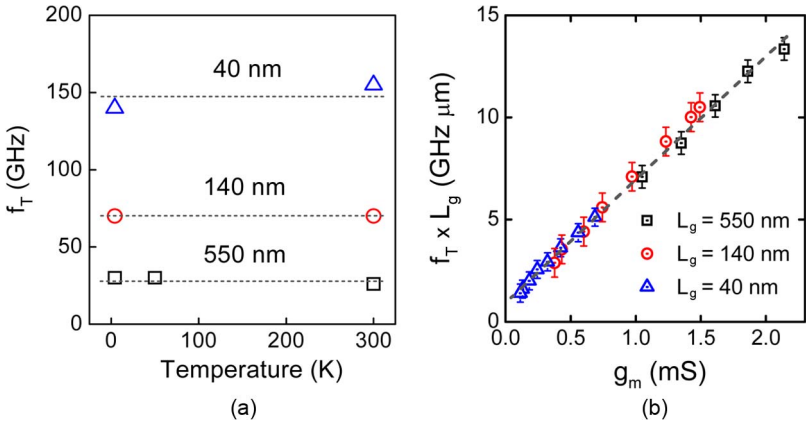

Fig. 12. *(a) Summary plot of the temperature dependence of f_T for three different devices, where little temperature dependence is found. (b) $f_T L_g$ versus direct current (dc) transconductance g_m for the three gate lengths. The data from these three different sets of devices fall onto the same line, the slope of which corresponds to the unit area gate capacitance. V_{ds} is 1.6 V and V_{gs} is -8 V for all three devices. The gate width is 30 μm for all devices. The f_T's presented here are all de-embedded and the as-measured f_T for the 40-, 140-, and 550-nm devices are 5, 9, and 10 GHz, respectively, at room temperature and similar at 4.3 K. This demonstrates the uniformity of the graphene devices, the consistency of the measurements, and the accuracy of the de-embedding approach. Figures reproduced from [13].*

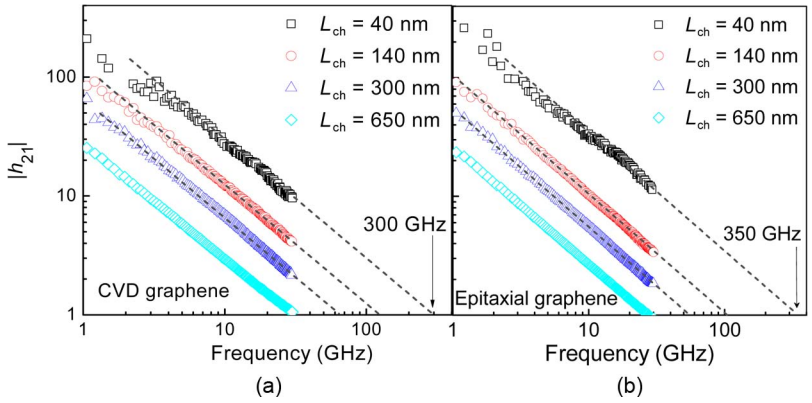

Fig. 13. ***(a) Small-signal current gain $|h_{21}|$ versus frequency for devices with channel lengths of 40, 140, 300, and 650 nm for RF devices based on CVD graphene and (b) on epitaxial graphene. Peak cutoff frequencies above 300 GHz are achieved for both types of graphene devices. For CVD graphene RF FETs, V_{ds} is from 0.5 to 0.8 V for channel lengths smaller than 300 nm and 1.6 V for channel lengths greater than 300 nm. V_{gs} is around −1.2 V, which coincides with the peak g_m. For epitaxial graphene RF FETs, V_{ds} is from 1 to 2 V for channel lengths smaller than 300 nm and around 4 V for channel lengths greater than 300 nm. V_{gs} is around −0.5 V, which coincides with the peak g_m. The gate width is 20 μm for all devices. The f_T's presented here are all de-embedded and the as-measured f_T's for CVD graphene for the 40-, 140-, 300-, and 650-nm devices are 9.3, 16, 15.9, and 14.8 GHz, respectively. The as-measured f_T's for epitaxial graphene for the 40-, 140-, 300-, and 650-nm devices are 10.5, 19, 18.5, and 15 GHz, respectively. Figures reproduced from [71].***

low output conductance in dc measurements translate into high current gain and high voltage gain in RF measurements. Therefore, the RF performance of graphene transistors can be optimized by choosing the gate dielectric best suited for the type of graphene material being used. These optimizations yield greatly improved RF performance for transistors based on both types of graphene. As shown in Fig. 13, cutoff frequencies of 300 GHz for CVD and 350 GHz for epitaxial graphene can be achieved using these dielectric stacks [71].

The cutoff frequency is the key figure of merit to evaluate the intrinsic speed of devices and is relevant in both analog and digital applications. Another important figure of merit for analog applications is the maximum oscillation frequency $f_{\max}$, which is typically determined as the frequency at which the maximum available gain (MAG) or the unilateral gain (U) become unity [72]–[74]. $f_{\max}$ is the highest operating frequency one can possibly achieve before a transistor loses the ability to amplify power. Fig. 14(a) and (b) shows unilateral power gain for these

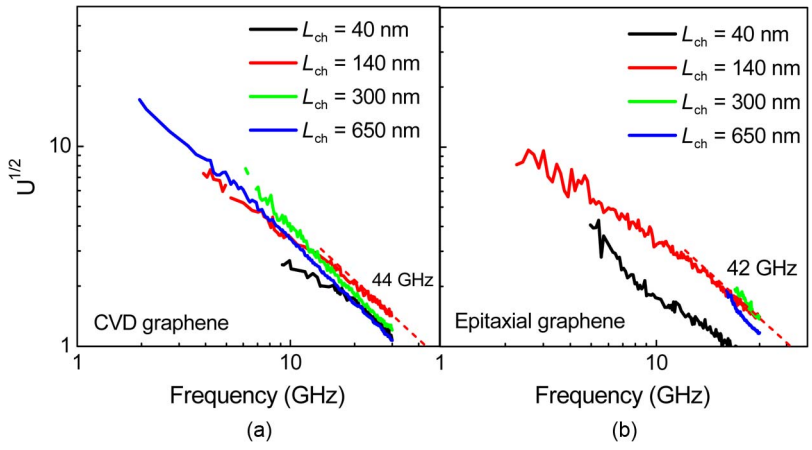

Fig. 14. ***(a) Mason's unilateral gain versus frequency, with a peak f_{max} of 44 GHz obtained from the 140-nm device using CVD graphene and (b) a peak f_{max} of 42 GHz obtained from the 140-nm device using epitaxial graphene. The bias conditions and device geometries are the same as those in Fig. 13. The f_{max}'s presented here are all de-embedded and the as-measured f_{max}'s for CVD graphene for the 40-, 140-, 300-, and 650-nm devices are 4, 14, 14, and 21 GHz, respectively. The as-measured f_{max}'s for epitaxial graphene for the 40-, 140-, 300-, and 650-nm devices are 4.3, 14, 23, and 20 GHz, respectively Figures reproduced from [71].***

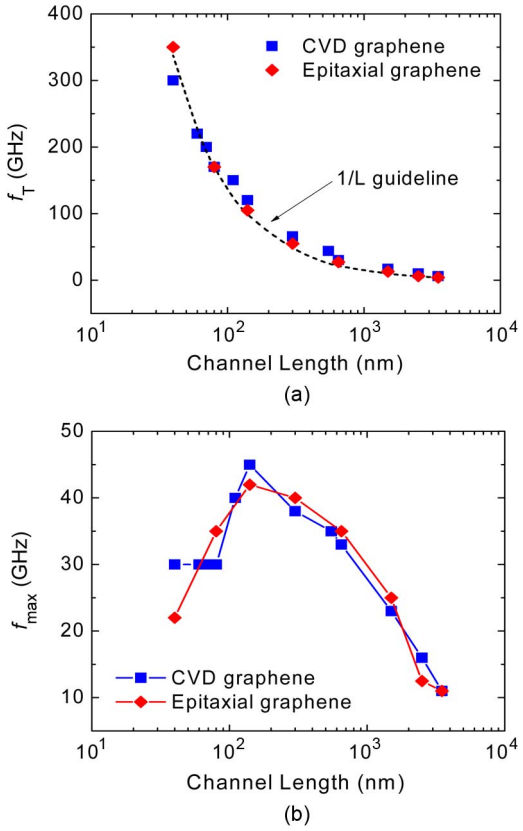

Fig. 15. *(a) Scaling behavior of de-embedded f_T versus channel length, showing the clear $1/L$ dependence. (b) f_{max} versus channel length with the peak f_{max} obtained at a channel length of 140 nm. Figures reproduced from [71].*

four devices, with a maximum f_{max} of 44 GHz obtained from the 140-nm device for CVD graphene and 42 GHz for epitaxial graphene, which is a factor of two improvement over the previous record of 20 GHz [12]. Unlike f_T, which can be directly related to the intrinsic graphene device properties, f_{max} is a more complex function: $f_{max} = f_T/(2\sqrt{g_{DS}(R_{Gate} + R_i + R_S) + 2\pi f_T C_{GD} R_{Gate}})$, where g_{DS} is the differential source/drain conductance, R_s is the source resistance, R_i is the channel-sided charging resistance of the gate/source capacitance, C_{GD} is the gate-to-drain capacitance, and R_{Gate} is the gate resistance. It can be seen from this that f_{max} not only depends on intrinsic device properties such as the transconductance and output conductance, but also relies on the extrinsic parasitic passive elements that can be further optimized. A well-behaved $1/L$ dependence of f_T is obtained for the RF transistors based on both CVD and epitaxial graphene, as can be seen from Fig. 15(a). The channel-length dependence of f_{max} is shown in Fig. 15(b). As discussed above, f_{max} has no monotonic dependence on the channel length since it is a more complex function that relies on external components. In comparison, f_T of the state-of-the-art graphene FETs has approached or reached in some cases the best of the other mature technologies such as Si or III–V high electron mobility transistors (HEMTs). However, much more work needs to be done to improve f_{max}, which heavily relies on the current saturation and gate geometry optimization.

While in typical performance evaluation for high-frequency transistors, f_T and f_{max} are the two most popular figures of merit, these two parameters present device performance limits under special conditions only. As a result, they are insufficient in providing a comprehensive evaluation of realistic circuits based on graphene devices. Specifically, f_T refers to short-circuit current gain with zero load impedance, which is a condition that does not exist in real circuits. f_{max} characterizes the power gain obtained using the best impedance matching networks, which is also not possible in many realistic cases. Therefore, to better evaluate the performance and potential of graphene RF devices, open-circuit voltage gain (A_V) is used as the more applicable figure of merit. In

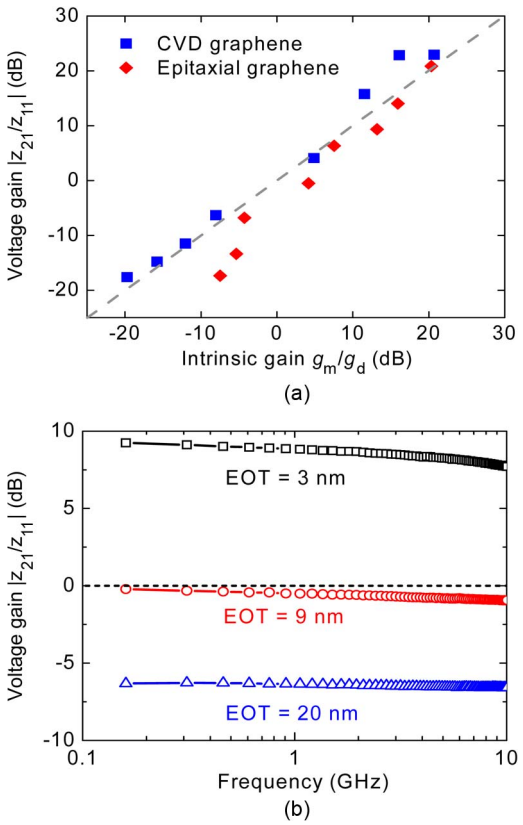

Fig. 16. *(a) Voltage gain $|z_{21}/z_{11}|$ versus intrinsic gain g_m/g_d, showing a linear dependence. This demonstrates the uniformity of the graphene devices, consistency of the measurement, and accuracy of the de-embedding approach. (b) Voltage gain of $|z_{21}/z_{11}|$ versus frequency for 300-nm-long graphene RF devices with three different EOT values. An improvement of voltage gain of more than 15 dB can be achieved by scaling the EOT from 20 to 3 nm. Figures reproduced from [71].*

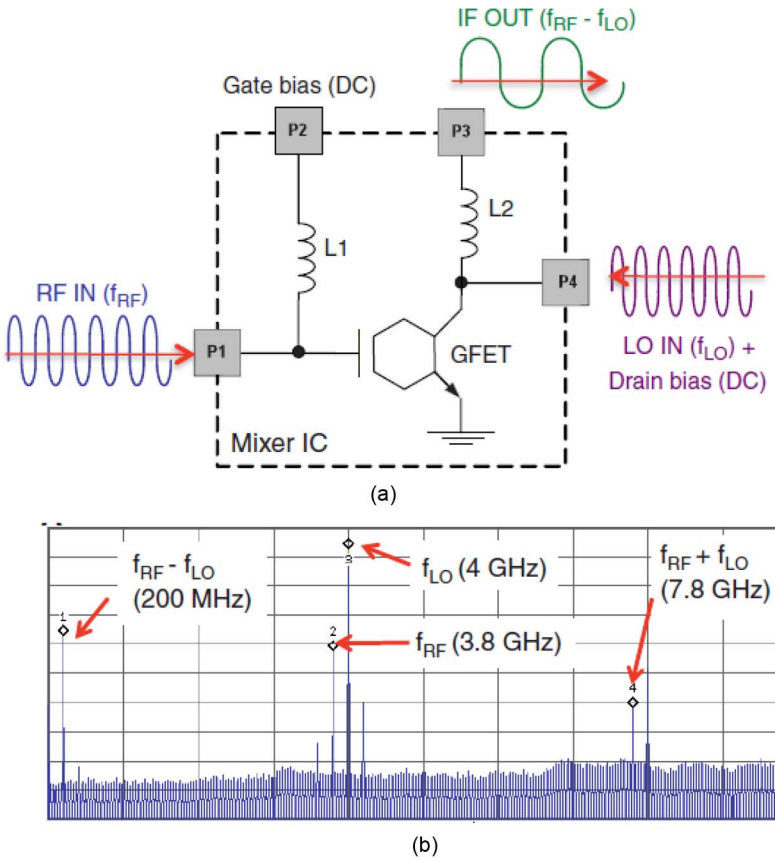

Fig. 17. *(a) Circuit diagram of a four-port graphene RF frequency mixer. The scope of the graphene IC is confined by the dashed box. The hexagonal symbol represents a graphene FET. The graphene FET here is a long-channel device. (b) A snapshot of the output spectrum, between 0 and 10 GHz, of the mixer taken from a spectrum analyzer with $f_{RF} = 3.8$ GHz and $f_{LO} = 4$ GHz. Each x and y division corresponds to 1 GHz and 10 dBm, respectively. The graphene FET is biased at a drain bias of 2 V and a gate voltage of −2 V. The input RF power is adjusted to 0 dBm so that the output spectrum power measured is the actual loss (gain) with respect to the RF input. Frequency mixing is visible with two peaks observed at frequencies of 200 MHz and 7.8 GHz with a signal power of −27 and −52 dBm, respectively. Figures reproduced from [90].*

the case of zero-bandgap graphene-based devices and circuits, this parameter is even more important because of the typically weak current saturation. The intrinsic gain, or self-gain, is the ratio of transconductance (g_m) and the output conductance (g_d), and can be directly translated into a voltage gain. From *S*-parameter measurements, the voltage gain can be expressed as the ratio of z_{21}/z_{11}. This ratio is frequency dependent and should approach the dc limit of the intrinsic gain of g_m/g_d at low frequencies. As shown in Fig. 16(a), the comparison of alternating current (ac) voltage gain z_{21}/z_{11} and dc intrinsic gain g_m/g_d exhibits the anticipated linear relationship with a slope of 1, confirming the validity of the voltage gain measurement.

Devices based on both types (epitaxial and CVD) of graphene materials show similar voltage gains. Values of voltage gain above 20 dB were achieved and are currently the highest attained for graphene devices [71]. Due to the weak current saturation behavior in scaled down devices, larger voltage gains are typically achieved in long-channel devices. Also, by reducing the dielectric thickness, the increased gate capacitance can lead to larger g_m. The combined effects of better saturation and g_m result in improved voltage gain. As shown in Fig. 16(b), an improvement in voltage gain of more than 15 dB is obtained by just scaling the equivalent oxide thickness (EOT), which demonstrates the potential and future directions of scaling in graphene high-frequency devices. Also, with better current saturation behavior using Bernal stacked bilayer graphene [75], recent demonstration on large-area bilayer graphene growth [76]–[79] shows the possibility of achieving even better voltage gain for graphene circuits.

IX. GRAPHENE INTEGRATED CIRCUITS

As discussed above, graphene transistors with intrinsic cutoff frequencies beyond 300 GHz have been demonstrated on large-area graphene materials. However, as for any other semiconductor technologies, it is essential to demonstrate the feasibility of monolithic integration of the

active transistors with other passive components. Heterogeneous integration of individual graphene transistors with external passive elements has been demonstrated recently by various research groups [80]–[89]. However, the resulting performance of the circuit is usually dominated by parasitics, which severely degrade the high intrinsic performance of the graphene transistors. Due to the many difficulties originating from the unique material properties of the graphene itself, wafer–scale integration of graphene transistors with other passive elements remains a challenge [90], [91].

An example of monolithic integration of a graphene integrated circuit (IC) is provided by a frequency mixer fabricated on a single SiC substrate using a wafer–scale processing [90]. This frequency mixer is based on the current modulation induced by the gate and the drain, and can be used in both ambipolar and unipolar operating regimes. As shown in Fig. 17(a), a high-frequency RF signal (f_{RF}) is applied to the gate and a local oscillator RF signal (f_{LO}) is applied to the drain of the graphene transistor. The drain current is then modulated by both signals. This resulting current contains the mixed frequencies of the two input frequencies, i.e., the sum $(f_{\mathrm{RF}} + f_{\mathrm{LO}})$ and the difference $(f_{\mathrm{RF}} - f_{\mathrm{LO}})$. The latter is usually referred to as the intermediate frequency (f_{IF}), and is typically the output signal component of interest. The integrated inductors are important in this mixer, as inductor $L1$ resonates out the pad and gate parasitic capacitances from the input terminal, and inductor $L2$ acts as a low-pass filter and is used as an input match to the LO signal.

This mixer takes advantage of the output characteristics of a graphene FET, which exhibits only weak current saturation. As a result, the nearly linear dependence of the drain current on the gate and drain biases can be expressed as $I_d \propto A \cdot (V_g - V_{\mathrm{CNP}}) \cdot V_d$, where A is a constant. The output power $P_{\mathrm{out}} \propto I_d^2 \propto g_m \cdot g_d \cdot (V_g - V_{\mathrm{CNP}}) \cdot V_d$ then has a frequency dependence on both the gate input f_{RF} and the local oscillator f_{LO}, and is proportional to the product of the transconductance and output conductance. The fact that the graphene transistor has relatively large output conductance helps to improve the performance of the frequency mixer, with superior linearity compared to other mixers operating in the saturation region. As shown in Fig. 17(b), the output frequency spectrum of the graphene mixer with input signals $f_{\mathrm{RF}} = 3.8$ GHz and $f_{\mathrm{LO}} = 4$ GHz clearly exhibits the mixing operation with a $f_{\mathrm{IF}} = 200$ MHz and $f_{\mathrm{RF}} + f_{\mathrm{LO}} = 7.8$ GHz. The output power of f_{IF} is proportional to that of f_{RF} up to 12 dBm and the f_{LO} power up to 20 dBm, demonstrating the high linearity indicated above. We also note that the conversion loss of -27 dB is very stable with less than 1 dB of fluctuation across a wide temperatures rage from 300 to 400 K.

A most important use of RF transistors and circuits is in amplifiers, which, of course, must have a voltage gain larger than 0 dB. As discussed above, the difficulty in achieving current saturation poses limitations on the magnitude of the gain. Nevertheless, progress is being made and the layout of a common source epitaxial graphene-based voltage amplifier is shown in Fig. 18(a). Here, a high-frequency signal applied to the gate electrode acts as an input, while a high impedance probe applied to the drain electrode acts as an output used to monitor the output voltage by a spectrum analyzer. The dc drain bias of the transistor is applied through a resistive load. With this structure, a positive voltage gain for the circuit can be achieved provided that the condition $g_m/(g_d + 1/R_{\mathrm{load}}) > 1$ is satisfied. As shown in Fig. 18(b), this integrated voltage amplifier has a gain of over 3 dB at an operating frequency of 5 MHz [71]. Note here that integration with other passive elements will degrade the graphene performance, and it requires much more effort to optimize the integration process. The main reasons that current graphene-based circuit is mainly operated at megahertz or low gigahertz frequencies are the nonoptimized parasitic components and integration processes. Furthermore, with high-quality novel substrates and gate dielectrics that are being explored, such as DLC or BN, graphene holds great potential for future high-frequency electronics. ■

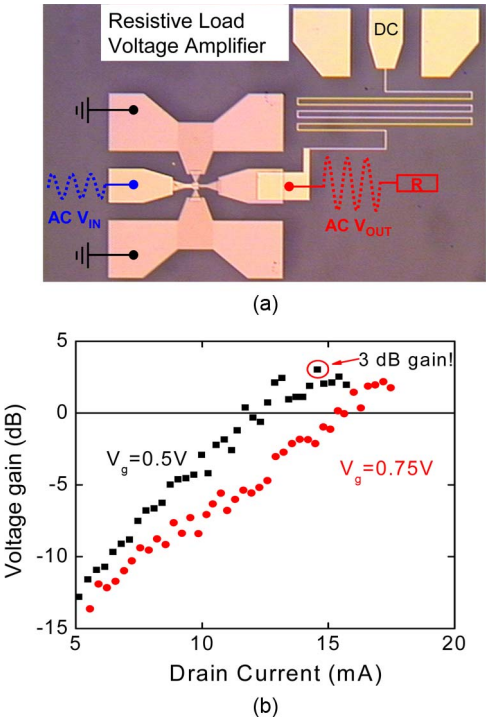

Fig. 18. *(a) An optical image of an integrated graphene amplifier with resistive load on wafer–scale epitaxial graphene. (b) The measured voltage gain versus drain current at 5 MHz for a 1.5-μm device with a maximum gain of 3 dB. The gate width is 20 μm and estimated V_{ds} for the device is around 6 V. f_T and f_{max} for the FET before the resistor fabrication are 3.5 and 4 GHz, respectively, both before and after de-embedding. Figures reproduced from [71].*

Acknowledgment

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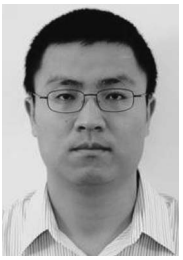
ABOUT THE AUTHORS



Yanqing Wu received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2005 and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, USA, in 2009.

He then joined the IBM Thomas J. Watson Center, Yorktown Heights, NY, USA, as a Postdoctoral Researcher and later became a Research Staff Member. He is currently a Professor at the Huazhong University of Science and Technology, Wuhan, Hubei, China. His research interests include graphene nanoelectronics; high-frequency devices and circuits; high-performance III–V metal–oxide–semiconductor field-effect transistors (MOSFETs), fin field-effect transistors (FinFETs), and high electron mobility transistors (HEMTs) for logic applications; and low-temperature transport on novel low-dimensional materials.

Damon B. Farmer received the B.S. degree in physics from Vanderbilt University, Nashville, TN, USA, in 2001, where he worked on silicon-carbide-based transistors for power electronic applications. He also received the Ph.D. degree in applied physics from Harvard University, Cambridge, MA, USA, in 2007, with a dissertation on the applications of atomic layer deposition in nanoelectronic systems.

He joined the research staff at the IBM Thomas J. Watson Center, Yorktown Heights, NY, USA, in 2010, after a postdoctoral fellowship at the same institution. He is currently performing research in the areas of graphene electronics and atomic layer deposition.

Fengnian Xia received the B.E. degree in electronic engineering (with the highest honors) from Tsinghua University, Beijing China, in 1998 and the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2005. His Ph.D. dissertation was about integrated receivers using regrowth-free methods for long-wavelength optical communications.

He then joined the IBM Thomas J. Watson Center, Yorktown Heights, NY, USA, as a Postdoctoral Researcher and currently is a Research Staff Member. He focuses on nanoelectronics and nanophotonics for futuristic switches and optical communications, using both conventional and newly emerged materials such as graphene and other 2-D systems, carbon nanotubes, silicon, and germanium. He is also actively involved in carrier transport in reduced dimensional systems. He authored and coauthored more than 50 peer-reviewed papers in leading scientific journals and delivered numerous invited and contributed talks in international conferences and universities.

Dr. Xia received an IBM corporate award, three IBM research division level awards, and many invention achievement awards. In 2011, he was selected by *MIT Technology Review* magazine as a top young innovator under the age of 35.

Phaedon Avouris received the B.Sc. degree in chemistry from the Aristotle University of Thessaloniki, Thessaloniki, Greece and the Ph.D. degree in physical chemistry from the Michigan State University, East Lansing, MI, USA, in 1974.

He is currently an IBM Fellow and Manager of Nanometer Scale Science & Technology at the IBM Thomas J. Watson Center, Yorktown Heights, NY, USA. He did postdoctoral work at the University of California Los Angeles (UCLA), Los Angeles, CA, USA and was a Research Fellow at AT&T Bell Laboratories before joining the staff of IBM's Research Division at the Watson Research Center as a research staff member in 1978. He has published about 500 scientific papers.

Dr. Avouris was elected Fellow of the American Academy of Arts and Sciences, the American Physical Society (APS), the Institute of Physics of the UK, the National Academy of Greece, the IBM Academy of Technology, the Materials Research Society, the American Association for the Advancement of Science, New York Academy of Sciences, and the American Vacuum Society (AVS). He has received many awards including the APS Irving Langmuir Prize for Chemical Physics, the IEEE Nanotechnology Pioneer Award, the MRS David Turnbull Lectureship, the AVS Medard W. Welch Award for Surface Science, the Julius Springer Award for Applied Physics, the Richard E. Smalley Research Award of the Electrochemical Society, and the Richard Feynman Nanotechnology Prize. He has also received many IBM Corporate and Outstanding Technical Achievement awards.