Physics-Based LED Modeling and Nonlinear Distortion Mitigating With Real-Time Implementation

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***Abstract*—In this paper, a nonlinear model for Light Emitting Diodes (LEDs) inspired by semiconductor physics, and a corresponding post-compensator are implemented in a Field Programmable Gate Array (FPGA) for real-time Visible Light Communications (VLC). Our experiments demonstrate that the LED model effectively characterizes the dynamic LED nonlinearity, including the memory effects. The output signal of this nonlinear LED model shows a good resemblance with the measured LED output. In addition, a dedicated nonlinear equalizer, say, a post-compensator, inspired by this LED physical model can mitigate the nonlinear distortion substantially. Thereby it facilitates high data rate over the bandwidth-limited LED. It shows that the nonlinear compensator is attractive for practical real-time digital signal processing systems due to its high performance and low complexity.**

***Index Terms*—LED, nonlinearity, post-compensator, real-time implementation.**

I. Introduction

AS THE LEDs by now dominate the illumination market, Visible Light Communication (VLC) that modulates LED light outputs with data, has become an active area in the communications society. Due to the potential high transmission rate, broad and license-free spectrum, and enhanced security, VLC becomes a promising technique in 6G [1], [2].

However, to accelerate the commercial applications of VLC, one of the critical problems that need to be settled is how to obtain a high-speed data transmission with mass–market LEDs. The bandwidth of these LEDs tends to be only several MHz [3], which strongly limits the data transmission rate of VLC systems. Besides, the nonlinear distortion of LEDs causes a performance degradation, particularly for the commonly used (linear) equalization, high-order modulation, multi-carrier modulation such as Orthogonal Frequency Division Multiplexing (OFDM) for increasingly scarce spectrum resource [4], etc.

To reduce the nonlinearity of LEDs, many methods have been developed in recent years. These can be classified into two categories, namely, optimizing the LED itself and compensating the input/output signal of the LED. The first method is mainly related to the research in the field of material science. By optimizing the material, structure and packaging technology of LEDs, it can avoid the decline of efficiency when large current is injected [5], and finally alleviate the nonlinearities of the LED.

In this work, we mainly discuss the second approach, namely utilizing signal processing for the input/output signal of the LED to compensate or mitigate the nonlinearities. To this end, it is essential to realistically model the dynamic nonlinear LED response. Then, an inverse structure can be inspired from this model to compensate nonlinearities. The generic method for modeling LED is Volterra model [6]. Nonlineariti compensation methods on the basis of Volterra model were reported [7]. Due to its generality, it is widely used to characterize different nonlinear systems. However, it is hardly implemented in practice due to its complexity. Though Wiener model [8] and Hammerstein model are two simplified cases of Volterra model, they fail to describe the dynamic memory effect of the LED [9]. Memory polynomial model [8], [10] is another special case of Volterra model, offering a compromise between performance and complexity. In recent years, there has been a surge in research on artificial intelligent and machine learning, which are also used to compensate the nonlinear distortion of the LED [11], [12].

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In this work, we argue that it is feasible to characterize the LED based on its internal physics processes rather than treating it as a black box using complex generic methods. As the nonlinear characteristics of the LED vary over time and differ for different LEDs, a practical high-speed real-time nonlinearity compensation technology requires both a suitable model structure and an effective parameter updating algorithm. A simple yet accurate LED model built from the physics of the LEDs will facilitate the parameter estimation process and reduce the overall complexity. In this work, we consider such LED model and study an inverse structure, which we use as post-compensator, to deal with the nonlinear distortion caused by the LED. As a next step in bringing such solutions, as also identified in [13], to maturity, in this paper we show that these concepts can be implemented in real–time signal processing. Both the nonlinear LED model and post-compensator are implemented in Field Programmable Gate Array (FPGA) for real-time applications. Experiments show high performance and low complexity of the nonlinear LED model and post-compensator. The remainder of this paper is organized as follows. In Section II, we describe the nonlinear LED model and post-compensator based on semiconductor theory in detail, in particular with FPGA implementation. In Section III, simulation and experimental results are presented and discussed in aspects of the accuracy of the LED model, effectiveness of the post-compensator, and the implementation complexity. Section IV draws conclusions from this paper.

II. Nonlinear LED Model and Post-Compensator Based on Semiconductor Theory

From injecting current $I(t)$ to output optical power $p_{opt}(t)$, several complex physical processes are involved. As an intermedium, the carrier concentration $n_c(t)$ is introduced to establish the connection between $I(t)$ and $p_{opt}(t)$. The carrier generation rate within the Quantum Well (QW) can be described as:

$$\frac{dn_c(t)}{dt} = R_{in}(t) - R(t) = \frac{I(t)}{qt_wA_w} - R_r(t) - R_{nr}(t), \quad (1)$$

where $R_{in}(t)$ is external carrier injection rate. $R(t)$ is carrier recombination rate, which equals to the sum of radiactive recombination rate $R_r(t)$ and non-radiactive recombination rate $R_{nr}(t)$. q, t_w and A_w are elementary charge, thickness and area of the active layer, respectively.

According to the classical ABC model [14], there are three dominant physical processes in nitride LEDs, including Shockley-Read-Hall (SRH) recombination, radiative recombination, and Auger recombination. For low level current injection situations (despite carrier leakage effect), the time-domain transient (dynamic) memory behavior of LED is governed by the full LED rate equation, expressed as

$$\frac{dn_c(t)}{dt} = \frac{I(t)}{qt_wA_w} - A_{nr}n_c(t) - B_rn_c^2(t) - C_{nr}n_c^3(t), \quad (2)$$

where A_{nr}, B_r, C_{nr} are the SRH, radiative, and Auger recombination coefficients, respectively. To make (2) suitable for digital signal processing at sampling interval T_s, a discrete-time approximation using Euler's method is constructed, namely [13]

$$\begin{aligned} n_c(t+T_s) &\approx n_c(t) + T_s\frac{dn_c(t)}{dt} \\ &\approx \frac{T_sI(t)}{qt_wA_w} + [1-(B_rp_0 + A_{nr})T_s])n_c(t) \\ &\quad - B_rT_sn_c^2(t) - C_{nr}T_sn_c^3(t). \end{aligned} \quad (3)$$

where p_0 represents the doping concentration. Here, an approximation is adopted to the radiative recombination rate $R_r(t)$ of p-doped LEDs, i.e. $R_r(t) \approx B_rp_0n_c(t) + B_rn_c^2(t)$. Since the carrier accumulation effect is included in the dynamic rate equation, the dynamic memory effect of the LED can be well described by (1)–(3). Based on the fact that the optical output power $p_{opt}(t)$ of the LED grew in proportion to $R_r(t)$, then we have

$$p_{opt}(t) = \bar{E}_pA_wt_w(B_rp_0n_c(t) + B_rn_c^2(t)), \quad (4)$$

where $\bar{E}_p$ is the average photon energy. Thus, an nonlinear LED model can be built based on (3) and (4), as shown in Fig. 1, where the coefficients $a_0 \ldots a_5$ reflect the physical LED parameters. More specifically $a_0 = T_s/(qt_wA_w)$, $a_1 = 1-(B_rp_0 + A_{nr})T_s$, $a_2 = -B_rT_s$, $a_3 = -C_{nr}T_s$, $a_4 = \bar{E}_pA_wt_wB_rp_0$ and $a_5 = \bar{E}_pA_wt_wB_r$. Note that, nonlinear LED model in Fig. 1 is built with Xilinx blocksets for real-time FPGA implementation. Although the physical model cannot consider all the physics in the LED, it can capture most of the LED characteristics, i.e., static memoryless and transient memory nonlinearity. In particular, the parameter discrepancy can be caused by different LEDs and other physical processes in practice which are not considered, e.g., the carrier leakage from active region to the barriers. However, the physical model is robust enough to cover the effect of those physical processes since it can adaptively adjust $a_0 \ldots a_5$.

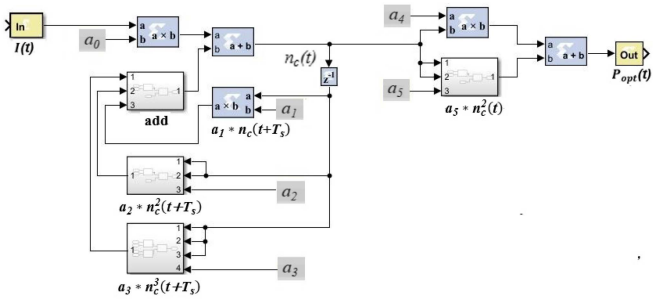

Fig. 1. Diagram of the physics-based nonlinear LED model, bulit with Xilinx FPGA blockset.

Considering that the nonlinearity of LEDs will change over time, and other LEDs that follow these physical processes may have different coefficients, Nelder-Mead Simplex Search (NMSS) algorithm is applied to estimate these coefficients based on the measured input and output signal of the LEDs. To be specific, in order to ensure that the LED nonlinear model can simulate the real LED, NMSS algorithm is used to train the LED model, and then estimate coefficients $a_0 \ldots a_5$ of the LED

model. Mean square error (MSE) is used as a metric to measure the difference between the LED model output and the real LED output. Under the premise of balancing the computational cost and performance, the iterative training process can be terminated when the MSE is relatively small. NMSS does not calculate the derivative of the cost function, but according to the cost function value to adjust the search direction. Matlab provides a function of the NMSS algorithm called $fminsearch$, which facilitates the nonlinear parameter estimation. Therefore, we only need use (3) and (4), and the real LED input/output signal to establish the objective function of LED model. Then, the coefficient of the LED model can be estimated.

Before implementing the nonlinear LED model with FPGA, several optimizations are conducted to the original nonlinear LED model (see Fig. 1). Firstly, coefficients $a_0 \ldots a_5$ are normalized by a_0, such that the dynamic ranges of coefficients are reduced, to allow fixed-point operations. Secondly, with a relatively small input current, the parameter a_3 can be negligibly small, so we omit the cubic term of (3). As a result, there are only 4 coefficients in the LED model. Thirdly, we rewrite the original nonlinear LED model with Horner's method. The original LED structure (3)–(4) can now be rewritten as

$$n_c(t+T_s) = I(t) + n_c(t)[a_1 + a_2 n_c(t)], \tag{5}$$

$$p_{opt}(t) = n_c(t)[a_4 + a_5 n_c(t)]. \tag{6}$$

In this way, half of multipliers can be saved in every iteration when using NMSS algorithm to estimate the coefficients of the nonlinear LED model. A high performance and low complexity LED model requires a simple model structure and an efficient parameter updating algorithm. The Volterra model is widely used in the modeling of various nonlinear systems [4], and it has the characteristics of universality and generality. In terms of model complexity, the second-order Volterra model with a memory length of 10 needs to estimate up to 65 coefficients, and the second-order Volterra model with a memory length of only 3 still needs to estimate 14 coefficients. In addition, there are the Wiener model [6] and the Hammerstein model, both of which can be seen as special forms of the Volterra model and have similar model structures. They have a simpler structure than Volterra models, but they can only describe the static nonlinear characteristics of the LED [7], [11]. However, we built a simple yet accurate LED model based on its physical properties. Our LED model can not only describe the dynamic memory nonlinearity of LED, but also has only four coefficients in the model. The reduction of the number of coefficients accelerates the parameter estimation process and leads to the overall complexity reduction. The reduced complexity helps the nonlinear model to run in the FPGA with a clock frequency of about 160 MHz. The final estimated coefficients of the nonlinear LED model for the used blue LED are shown in Table I.

Inspired by the nonlinear LED model, a reverse structure as a post-compensator is applied to compensate the nonlinear distortion of LED, which can be written as

$$\tilde{n}_c(t) = \sqrt{d_0 I(t) + d_1} + d_2, \tag{7}$$

TABLE I
NORMALIZED ESTIMATED COEFFICIENTS FOR THE NONLIENAR LED MODEL

Parameter	Value	Value (normalized)
a_1	0.9888	0.9888
a_2	$-6.4841 * 10^{-21}$	-0.0002636286
a_4	$4.3971 * 10^{-19}$	0.0178776
a_5	$3.516 * 10^{-37}$	0.0005812119

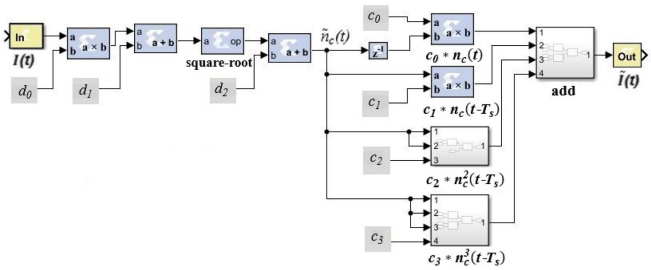

Fig. 2. Diagram of the post-compensator, bulit with Xilinx FPGA blockset.

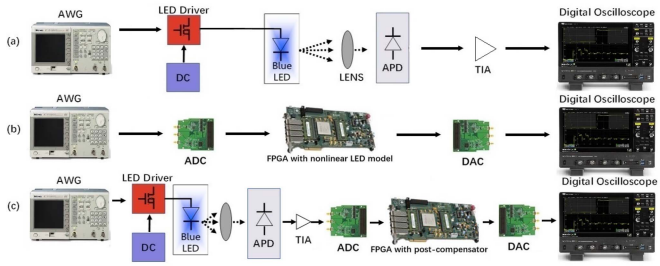

Fig. 3. Verification processes. (a) Real LED output signal measurement. (b) Nonlinear LED model output signal measurement. (c) Post-compensator output signal measurement.

$$\tilde{I}(t+T_s) = c_0\tilde{n}_c(t+T_s) + c_1\tilde{n}_c(t) + c_2\tilde{n}_c^2(t) + c_3\tilde{n}_c^3(t), \tag{8}$$

where $d_0 = 1/\tilde{a}_5$, $d_1 = \tilde{a}_4^2/4\tilde{a}_5^2$, $d_2 = -\tilde{a}_4/2\tilde{a}_5$, $c_0 = 1/\tilde{a}_0$, $c_1 = -\tilde{a}_1/\tilde{a}_0$, $c_2 = -\tilde{a}_2/\tilde{a}_0$, $c_3 = -\tilde{a}_3/\tilde{a}_0$. $\tilde{a}_0 \ldots \tilde{a}_5$ are the estimated value of $a_0 \ldots a_5$. The implementation diagram of the post-compensator is provided in Fig. 2. To compensate the feedback structure of the nonlinear LED model, the post-compensator has a feed-forward structure, which facilitates parallel high-speed data processing.

III. PERFORMANCE VERIFICATION AND DISCUSSION

The performance of the nonlinear LED model and the corresponding post-compensator are verified by experiments following the verification processes in Fig. 3, including the real LED measurement, nonlinear LED model measurement and post-compensator measurement. The signal is generated from the Arbitrary Waveform Generator (AWG, Tektronix AFG3251), as the input of the LED driver. Then the signal is fed into the LED (HCCLS2021CHI02) and transmitted through a wireless channel. The signal is received by an avalanche photodiode (APD) module (Thorlabs PDA10A2). The data requiring offline representation is recorded and stored by the oscilloscope (Lecroy WAVEMASTER813Zi). In this work, an Xilinx FPGA

evaluation board featured with a Kintex-7 XC7K325TFFG676-2 device is utilized for real-time implementation. The used Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) carrying FPGA Mezzanine Card (FMC) connectors are AD9613 and AD9706 respectively. The sampling rates of ADC and DAC are 250MSPS and 175MSPS respectively, with resolution are 12-bit. The photoelectric characteristics of the LED device used in our experiment can be found in [13]. From these characteristics, when the forward current is 100 mA at room temperature, the standard value of forward voltage is 3.26 V with optical power of 134.2 mW at 456.2 nm. This LED device adopts EMC3030 patch and PCB board packaging process.

A. Nonlinear LED Model Verification and Discussion

The VLC setup is shown in Fig. 3(a) and the setup for verification of the LED model is depicted in Fig. 3(b). To capture the intrinsic on-off transition characteristics of the LED, we firstly measure the output signal of a blue LED in the real VLC system using a square wave input signal with a frequency of 1 MHz. An APD is used to capture the LED output signal, and this signal is finally sampled and displayed by an oscilloscope. Next, the nonlinear LED model is loaded into the FPGA and the output signal of the nonlinear LED model is also measured (see Fig. 3(b)). The performance of the nonlinear LED model can be readily analysed by comparing the signal data stored in oscilloscopes.

To implement the nonlinear LED model with FPGA, the netlist project of this model needs to firstly be built with hardware description language (HDL). Then, the configuration HDL codes for ADC and DAC are included with the LED model. After generating the bit stream, this LED model can be run in the FPGA, to simulate the nonlinear behavior of the LED in real-time. The ADC and DAC modules are used to sample the analog signal from the AWG and to convert the digital signal from the FPGA into an analog signal, respectively. Then, the output signal from the DAC can be observed on the oscilloscope.

Fig. 4(a) shows the experimental setup of the nonlinear LED model implemented in the FPGA. The output signal of the real LED and the nonlinear model is further compared in Fig. 4(b). We see that the nonlinear LED model accurately mimics the on-off transitions characteristics of the real LED, which differ from the exponential rise and fall curves that a linear system would exhibit. The mean square error (MSE) between the two curves is 1.8×10^{-3}, which confirms a decent match. The differences between the rise and fall time of the LED output, i.e., 72 ns and 139 ns respectively, further confirm the significant nonlinearity.

B. Post-Compensator Verification and Discussion

In order to verify the performance of the post-compensator, we first apply it to the PAM-4 system with white Gaussian noise for Symbol Error Rate (SER) simulation. A matched filter is used to filter out the noise outside the signal band and maximize the Signal to Noise Ratio (SNR). As can be seen in Fig. 5, the SER increases with the symbol rate due to the bandwidth-limited channel which introduces distortion to the signal. With the application of the proposed post-compensator,

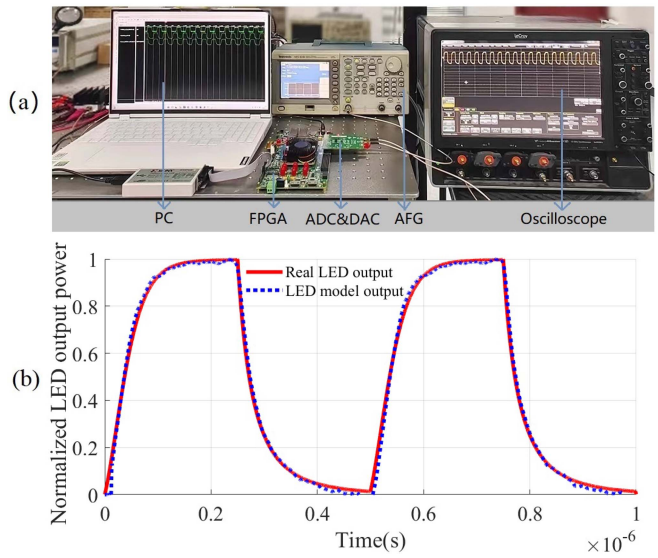

Fig. 4. (a) Experimental setup. (b) Comparison between the output signal of the real LED (red solid line) and the LED model as generated by the FPGA (blue dotted line).

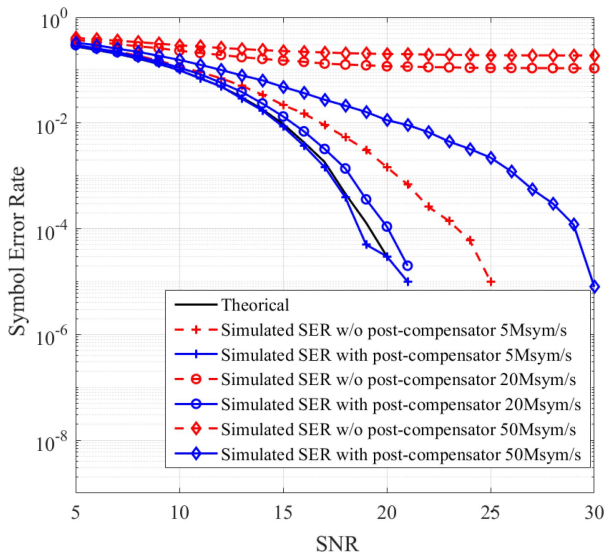

Fig. 5. SER of the PAM-4 system with and without post-compensator.

the SER for the input symbol rate 5 Msym/s and 20 Msym/s is close to the theoretical SER of PAM4 system. This illustrates the excellent performance of the post-compensator. While, when the input symbol rate is increased to 50 Msym/s, the SER of the system with the post-compensator is far from the theoretical one. This is mainly due to the fact that the signal bandwidth of 50 Msym/s significantly exceeds the 3 dB bandwidth of the used LED model (around 15 MHz), and in this case the channel-introduced distortion cannot be sufficient mitigated by the post-compensator. In spite of this, when the input symbol rate is high, the performance of the system with the post-compensator is still much better than that of the system without the post-compensator.

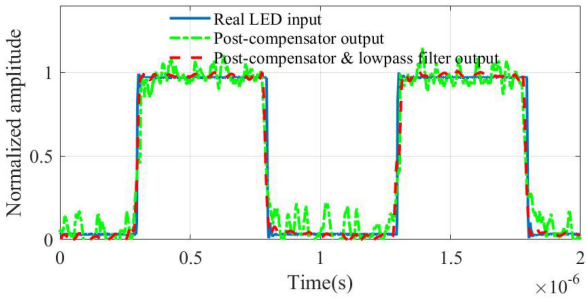

Fig. 6. 1 MHz square wave input signal of the real LED (blue), the FPGA output signal of the post-compensator (green) and the signal through both post-compensator and low-pass filter (red).

To further verify the post-compensator, it is implemented with FPGA. Fig. 3(c) shows the setup for the implementation of the post-compensator with FPGA. This implementation process is similar to the implementation process of the nonlinear LED model, as described before. However, the input of the post-compensator is the distorted signal from the real LED, which is stored in the Read Only Memory (ROM) of the FPGA. Then it is fed into the post-compensator. After being processed by the post-compensator, the signal is transferred to the DAC and is then shown on the oscilloscope. The running rate of the post-compensator is set to 160 MSPS, since the maximum conversion rate of the used DAC is limited. In fact, with a faster DAC, our post-compensator is able to run at a rate beyond 220 MSPS. To be specific, the highest symbol rate depends on the speed of both FPGA and DAC/ADC, and is limited by the lower one of their supported rates. According to the static timing analysis for the proposed circuit with the used FPGA (Kintex-7 XC7K325TFFG676-2), and under the assumption that the worst setup slack is 0, the highest operating frequency of the post-compensator is 220 MHz according to the static timing analysis for the design after the layout and wiring. In this case, the symbol rate of signal is mainly limited by the selected DAC (AD9706) which has a sampling rate of 175MSPS. In addition, the highest achievable data rate also depends on the modulation order and noise, beside the symbol rate. However, the used FPGA development board is not optimized with ADC and DAC, the supported highest symbol rate of the board is lower than the sampling rate of DAC.

The accuracy of this post-compensator can be verified by comparing the input signal of the blue LED and the output signal of post-compensator. As shown in Fig. 6, the post-compensator accurately recovered the original signal from the distorted one. Quantitatively, the MSE between the input signal of the real VLC system and the output signal of the post-compensator is 8.8×10^{-3}, which also verifies the effectiveness of the post-compensator. It is worth mentioning that when a filter is applied to suppress the noise, the selection of the cut-off frequency of the low-pass filter is particularly important. Because the square wave signal is a superposition of different frequency components based on the Fourier expansion, if the cut-off frequency of the low-pass filter is too low, the effective component of the square wave signal will be filtered out, causing distortion in the square-wave signal. In contrast, if the cut-off frequency is too high, the noise cannot be effectively filtered out.

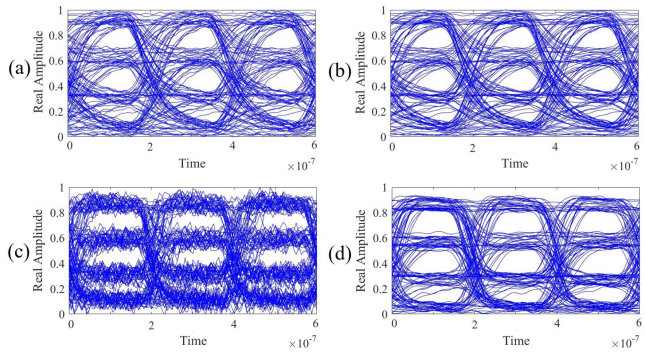

Fig. 7. (a) Eye diagram of the real LED output when 5 Msym/s PAM-4 signal is input. (b) Signal in (a) processed by lowpass filter. (c) Signal in (a) processed by post-compensator in FPGA. (d) Signal in (a) processed by both post-compensator and low-pass filter.

TABLE II
RESOURCE UTILIZATION OF THE NONLINEAR LED MODEL

Resource	LUT	LUTRAM	FF	BRAM	DSP
Used	3450	639	4596	8.5	4
Available	203800	64000	407600	445	840
Utilization	1.69%	1%	1.13%	1.91%	0.48%

TABLE III
RESOURCE UTILIZATION OF THE POST-COMPENSATOR

Resource	LUT	LUTRAM	FF	BRAM	DSP
Used	4592	881	6275	18	18
Available	203800	64000	407600	445	840
Utilization	2.25%	1.38%	1.54%	4.04%	2.14%

Fig. 7 further shows the eye diagrams within a PAM-4 system. To clearly present the effect such as right-skew caused by the LED nonlinearity and the effect of signal processing, the eye diagram with symbol rate of 5 Msym/s is presented for comparison. As shown in Fig. 7(a), due to the LED nonlinearities, there is a right-skew in the eyes and low-level eyes are almost closed. This indicates the measured 5 Msym/s PAM-4 signal suffered from a serious distortion. Fig. 7(b) shows the eyediagram of the measured 5 Msym/s PAM-4 signal processed by a low-pass filter. As can be seen, it fails to recover the distorted signal. In Fig. 7(c), with the processing of the post-compensator, the right-skew of the eyes disappears, but there is still much high-frequency noise in the signal. To further improve the signal quality, a low-pass filter is applied following the post-compensator. As shown in Fig. 7(d), the eye openings are enlarged and become clearer, which means the distorted signal has been compensated and a higher quality signal is obtained.

C. Resource Utilization and Timing Analysis in FPGA

The resource utilization of the nonlinear LED model and the post-compensator are listed in Tables II and III respectively. Mainly due to the square-root operation, the post-compensator needs more resources compared with the nonlinear LED model, including the Lookup Table (LUT), Flip-Flop (FF), DSP, etc.

TABLE IV
DESIGN TIMING OF THE NONLINEAR LED MODEL

Type	Worst slack	Total violation	Failing endpoints	Total endpoints
$Setup$	$29.973ns$	$0.000ns$	0	928
$Hold$	$0.058ns$	$0.000ns$	0	928
$PulseWidth$	$15.732ns$	$0.000ns$	0	483

TABLE V
DESIGN TIMING OF THE POST-COMPENSATOR

Type	Worst slack	Total violation	Failing endpoints	Total endpoints
$Setup$	$1.277ns$	$0.000ns$	0	13623
$Hold$	$0.047ns$	$0.000ns$	0	13623
$PulseWidth$	$2.357ns$	$0.000ns$	0	7252

The total utilization for the LED model and post-compensator are 0.48% and 2.14% respectively, which indicates the low-complexity of the proposed methods and facilitates the real-time implementation. The design timing of them are also listed in Tables IV and V respectively. Among them, the setup slack is the difference between the required data arrival time and the actual data arrival time, and the worst setup slack is the minimum among all the setup slacks. It can be positive or negative. The negative value refers to the setup time sequence violation, and the positive value refers to the correct setup time sequence. Similarly, the hold slack is the difference between the actual data departure time and the required data departure time, and the worst hold slack is the smallest of all the hold slacks. A positive value refers to the hold time sequence of all paths is correct. When all paths meet timing requirements, the worst pulse width slack is positive without any timing issue. All values of the worst slacks in Tables IV and V are positive, indicating that our designs meet the timing requirements of FPGA.

IV. CONCLUSION

For the first time, we implemented the novel physics-based nonlinear LED model and post-compensator in FPGA for real-time applications. This work exhibits great potential of bringing such physics-based structures into real-time digital signal processing. On the basis of fully understanding the internal physical mechanism of the LED, the LED model we established not only can simulate the dynamic memory nonlinearity of LED, but also has only four coefficients in the model. Compared with the Volterra model, the coefficients to be estimated is greatly reduced. In addition, we used the NMSS algorithm to estimate the parameters of the LED model, and it only took 1000 iterations to achieve convergence. Finally, we construct a high performance and low complexity post-compensator according to the inverse process of LED modeling. Due to the low complexity, the post-compensator can be run at a clock frequency of 220 MHz in the used FPGA to compensate the distorted signal. In FPGA, the utilization of all resources of the LED model and the post-compensator model is less than 2.5%, which indicates the low complexity of the proposed model and facilitates the real-time implementation.

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