All Silicon Microdisplay Fabricated Utilizing 0.18 μm CMOS-IC With Monolithic Integration

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***Abstract*—A low voltage all silicon microdisplay is presented based on MOS-like gate-control all-Silicon light-emitting diode (LED) in standard 0.18 μm complementary metal oxide semiconductor (CMOS) technology. The MOS-like LED is designed under a PN alternate structure with polysilicon gate control electrode for high luminous intensity and low operating voltage. The microdisplay device is fabricated based on the LED as pixel units. The size of the proposed microdisplay device is 6.2 mm $\times$ 5.0 mm with a about 368 mW/mm2 luminous intensity at the stable operating voltage of 1.8 V.**

***Index Terms*—All-Silicon CMOS LED microdisplay gate-control.**

I. Introduction

THE silicon light-emitting device (LED) has developed into a broad concept which includes research in many fields. Its applications in microdisplay have attracted extensive attention. [1]–[3] The most promising technology for microdisplay is Micro-LED (pixel size less than 100 μm) and mini-LED (pixel size from 100 μm to 500 μm) which all based on the principle of LED with different materials such as GaN and other Nitride. [4]–[6] Although these microdisplay light-emitting diodes have achieved relatively high luminous efficiency, their complicated process and poor thermal stability remain the main obstacles for realizing monolithic integration with the most widely used micro-electronics technology, namely, standard silicon(Si) complementary metal oxide semiconductor (CMOS) technology. [7] In order to solve these problems, this study uses MOS-like gate-control all-silicon LEDs as the pixel units to fabricate a microdisplay devices, which are compatible with the standard CMOS process.

Due to its widespread application, sufficient resources and semiconductor characteristics, Si is still an important material in the semiconductor and integrated circuit field. The development of the semiconductor industry in recent decades has been based on various applications of silicon materials. However, the Si's indirect band-gap property severely restricted the application of silicon materials in the field of luminescence. Many attempts have been made such as Si /SiO_2 superlattices [8], Si quantum dots [9] and Si nanocrystals [10]. The most practical attempt among these attempts is the luminescence phenomenon of the silicon PN junction under reverse-biased avalanche mode, and the silicon-based light-emitting device has appeared based on this mechanism. [11] Silicon-based LEDs have been fabricated by Xu *et al.* utilizing standard CMOS technology. [12] Furthermore, the light intensity can be controlled by the gate voltage in the all-silicon MOS-like LEDs.

From recent research, there are also many results on silicon-based microdisplay. Snyman *et al.* fabricated a 100 nW 5GHz Silicon Avalanche based LED with good performance. [13] Germer *et al.* designed silicon-based LED display arrays based on silicon p-n junction in standard 0.35-μm CMOS technology with improved emission power. [14] Muhowski *et al.* fabricated mid-infrared superlattice LEDs on silicon and predicted its light-emitting phenomenon in principle. [15] Jiang *et al.* fabricated a multiphase switched-capacitor converter for fully integrated active-matrix light-emitting diode (AMLED) which is useful for the interconnections of microdisplay system. [16] In contrast to these works, this paper applies a gated technology to realize light emission at the junction of each pixel unit.

Utilizing the electroluminescence (EL) phenomenon of the silicon PN junction under reverse-biased avalanche mode, we designed a low voltage MOS-like gate-control all-silicon LED and fabricated a microdisplay devices based on 100 $\times$ 100 pixel array of the LEDs using standard SMIC 0.18 μm CMOS technology. This microdisplay device can be powered by a common voltage power supply, such as a normal power supply for CMOS integrated circuits. Compared with our previous studies, this device has achieved better performance, such as lower operating voltage, higher frequency, which is comparable to those of other similar LEDs. [17] The emission spectrum of our microdisplay device ranges from visible light range to near infrared range

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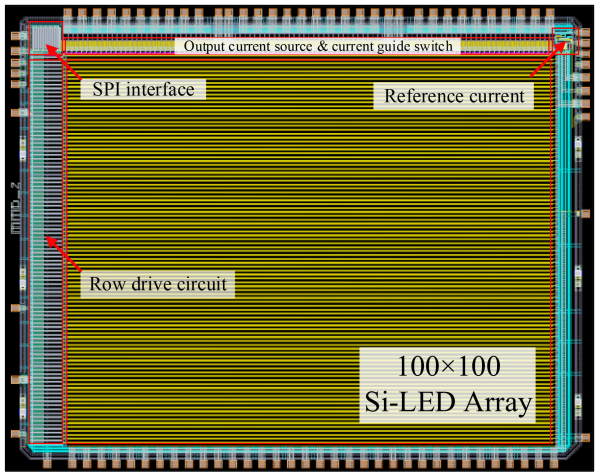
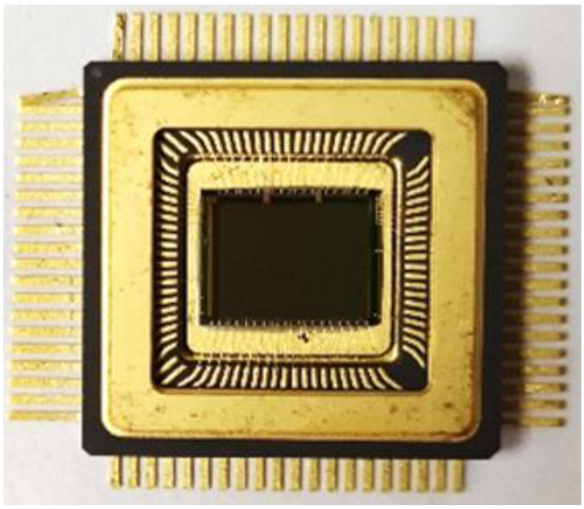


(a)



(b)

Fig. 1. (a) Layout (b) Sample of the 100x100 pixel array microdisplay device.

(450 nm-1000 nm). Furthermore, this device can be controlled by applying different gate voltages to obtain several operating voltages and optical-power efficiencies, which makes multiple working modes possible. We named this control method as 'gate-control'. This low voltage all-silicon device can be used in nightvision viewer, Projection display and Helmet mounted display. [18], [19]

II. Device Structure and Methods

The design and fabrication of 100x100 pixel array of the MOS-like gate-control all-silicon LED is based on traditional standard CMOS technology. The device takes the full advantages of the mature CMOS process. The layout of the 100x100 pixel array microdisplay device is shown in Fig. 1(a). The sample is shown in Fig. 1(b).

The device is fabricated using a 0.18 μm SMIC CMOS technology without any modification. The entire light-emitting device is fabricated in the same N-type well, and contains two identical PMOS light-emitting units placed side by side. The gate length L of the PMOS cell is 3 μm, the gate width W (Y axis) is 25 μm, and the area of the source and drain active regions is appropriately increased. The source and drain active regions are covered with metal and the anode is located upward, between the metal electrode and the side wall leave a 2 μm light-emitting window. The N+ doping is performed at 0.5 μm on the left and right sides of the PMOS cell as a N-well contact, and the upper part is covered with metal and the cathode is located downward. The gates of the two PMOS light-emitting units are separately led out as the third control electrodes, which we named it 'gate-control electrode'. Total area of the device is about 25 μm $\times$ 25 μm. And a P+ ion implantation is carried out on the substrate with a 1.5 μm distance from the N-well to form a guard ring to avoid the formation of a latch-up effect with other surrounding devices, and also to avoid the breakdown between the P-type substrate and the N-well. The PN junction formed between them is preferentially broken down. In addition, in order to further improve the external quantum efficiency of silicon LEDs, SAB (Salicide Block) is used to cover the light-emitting windows on both sides of the side wall during layout design to prevent the formation of opaque metal silicide on the surface of the light-emitting area.

The positive and negative electrodes are led out on both sides of the silicon LED, and each silicon LED device is made in a separate N-type well, which is convenient for independently controlled. A row drive transistor is placed next to each silicon LED to control the flow of current from the column line into the light-emitting unit. In order to effectively reduce the gate resistance and the area of the source/drain junction, the row drive transistor adopts an "interdigital" structure design, and the number of finger transistors is increased as much as possible. The column line and the negative power line use a multi-layer metal overlapping wiring design to reduce the partial pressure on the metal wire as much as possible.

The mechanism of this microdisplay device is stated as follows. According to the theory of carrier recombination, the luminescence phenomenon of PN junction is mainly caused by the release of excess energy in the form of photons when the carriers inside the material transition from a high energy level to a low energy level. However, since silicon is an indirect band gap semiconductor material, the band transitions of carriers are mostly non-radiative recombination involving phonons, because most different particle transition quantum states have different vectors in K-space. As a result, the light output power and external quantum efficiency of light-emitting devices based on silicon materials are very low.

We improve the external quantum efficiency through the principle of gate control and avalanche breakdown. (1)–(4) shows the theoretical model of photon emission from MOSFETs and (5) shows the electron avalanche multiplication coefficient M_x:[20]

$$W_v dv = \frac{Ddv N_c I_d}{m^* q^2 \lambda} \int_0^L \frac{E_1\left(\frac{hv}{qE_x\lambda}\right)}{E_x} dx \tag{1}$$

The energy radiated per unit frequency per unit time is Wv. Energy radiated per unit time in the frequency interval from v_1

to v_2 is

$$E_{v_1,v_2} = \int_{v_1}^{v_2} W_v dv \tag{2}$$

For a MOSFET, the impact-ionization substrate current can be expressed as

$$I_{sub} = \frac{I_d A_i E_m^2}{B_i \left[\frac{dE_x}{dx}\right]_{x=L}} e^{-B_i/E_m} \tag{3}$$

$$E_{v_1,v_2} \approx \left(\frac{DN_c\lambda}{m^* h^2}\right)\left(\frac{I_{sub}B_i}{A_i} e^{B_i/E_m}\right)\left(\frac{h}{qE_m\lambda}\right) \left[\ln(\frac{v_1}{v_2}) + \left(\frac{h}{qE_m\lambda}\right)(v_2 - v_1)\right] \tag{4}$$

$$M\ (x) = \frac{1}{1 - \int_0^{W_d} \alpha_n \exp\left[\int_0^x \alpha_n - \alpha_p dx'\right] dx} \tag{5}$$

where W_d is the width of depletion region for an p-n junction or Schottky junction and α_n and α_p are the ionization rates of electrons and holes. In order to occur avalanche breakdown, it is necessary to make the denominator of the formula infinite, that is, the number of electron-hole pairs in the depletion region is infinite.

This can be achieved by applying a large reverse bias voltage, but it is difficult for the device to work stably in the breakdown state, and the luminous efficiency also needs to be improved. We use another method, 'gate-control', to improve avalanche efficiency, reduce breakdown voltage and increase luminous efficiency. This method can form a 'current channel' in the depletion region, thereby greatly reducing the limiting conditions of avalanche breakdown. The detailed principle explanation will be provided through simulation results below. Fig. 2(a) and 2(b) show the difference between 'gate-control' and 'no-gate-control'.

In the actual production process, when the P^+ ion implantation is performed on the PMOS source/drain region, the impurity concentration at the silicon surface is slightly higher than the impurity concentration in the silicon body, so the width of the depletion region of the horizontal diode is actually smaller than that of the vertical diode. At the same time, the reverse breakdown voltage is also reduced. Therefore, when the reverse bias voltage of the P^+ source/drain region and the N well is high enough, breakdown will occur at the lateral diode at the silicon surface first, thereby restricting the light-emitting point to the silicon The surface is conducive to light output. At the same time, there are a large number of traps at the Si/SiO2 interface, and the interface traps also actually promote the light emission of the silicon PN junction.

When the gate voltage is applied, the 'gate control' function starts to play its role. The gate oxide layer slightly overlaps the P+ source/drain regions, so a capacitor structure is actually formed between the polysilicon gate and the source/drain edge covered by the oxide layer. When a higher positive voltage is applied to the polysilicon gate, a vertical downward electric field will be generated on the surface of the silicon, thereby attracting electrons to gather on the surface of the silicon. When the voltage of the gate is high enough, an N^{++} electron accumulation layer and an N^+ inversion layer is formed on the surface of the

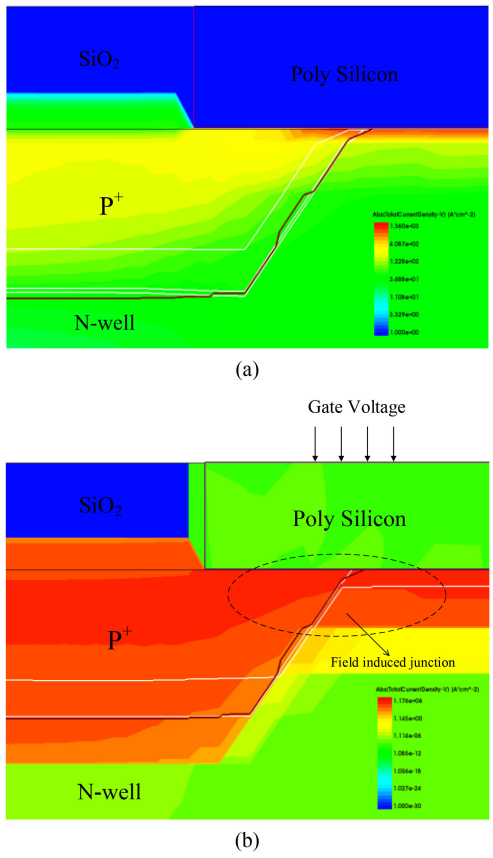


Fig. 2. Current density distribution with (a) No-gate-control (b) Gate-control at breakdown state.

N-type well at the edge of the gate oxide and the surface of the P^+ type source/drain region respectively. The existence of this thin electron layer made the P^+N junction at the boundary of the source/drain region covered by the insulating gate become a $P^+N^+N^{++}$ 'field-induced junction'. Compared with the normal diffusion junction, the width of the depletion region of the field-induced junction is narrower and the breakdown voltage is lower, resulting in a greater current density through the field-induced junction at the same reverse bias voltage, and higher current density also means that the probability of radiative recombination of carriers is greater. This method of restricting the conduction current to the surface of silicon through the gate voltage, thereby improving the luminous efficiency of PN junction avalanche breakdown is called 'gate-control' method.

III. Experiments and Analysis

The all-silicon LED emits visible light when a reverse bias voltage is applied. The typical I-V_{gate} characteristic diagram of the fabricated all-silicon LED under operating condition is shown in Fig. 3. This diagram shows the difference of the total current under different 'gate control' conditions. It can be clearly seen that 'gate control' greatly reduces the breakdown voltage (at the same current), so that the all-silicon LED can work at a relatively low voltage, which not only improves the stability but also the total current. In addition, this method results in an increase in the luminous intensity.

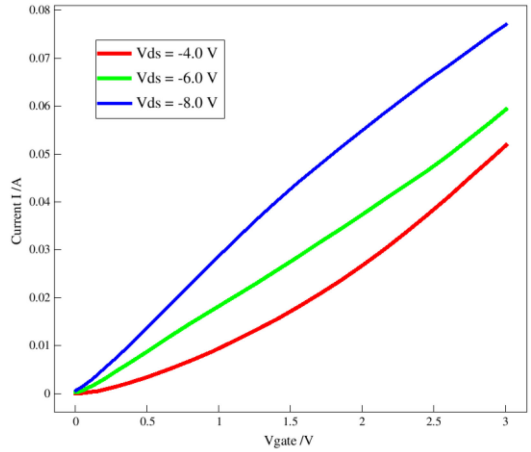


Fig. 3. I-V_{gate} diagram of All-Silicon LED.

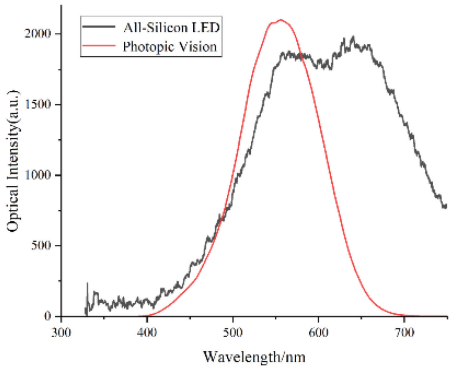


Fig. 4. Emission spectrum of All-silicon LED (V_{gate} = 2.0V) and the Photopic Vision.

The emission spectrum of All-silicon LED is also measured as shown in Fig. 4. The spectrum is a continuous spectrum, covering the visible light region from 420 to 780 nm, where peaks appear at wavelengths of 580 nm and 650 nm. Therefore, the device mainly emits orange-yellow light. Refer to the emission mechanism model proposed by Akil *et al.*, the phenomenon of optical transmitters with different wavelengths can be explained [21]. For wavelengths greater than 620 nm (photon energy is less than 2.0ev), it is mainly an electronic indirect interband transition assisted by phonons; for photons with a wavelength range of 539 nm to 620 nm (photon energy between 2ev and 2.3ev), it is due to the action of intraband bremsstrahlung; high-energy photons with a wavelength shorter than 539 nm (photon energy more than 2.3ev) emit lights because the electrons are accelerated by the strong electric field in the space charge region to form high-energy hot electrons, and they recombine with the holes at the same wave vector to produce a direct transition between bands. By comparing the emission spectrum of the device with the photopic vision, it can be found that there is a large overlap in the 500-600 nm wavelength range, which are the most sensitive range the human eyes can react. The Fig. 5 reveals the actual light emitted by the all-silicon LEDs. The luminous power is about 59.8nW, detected by the spectral measurement equipment with an operating voltage of 3.8V. [22]

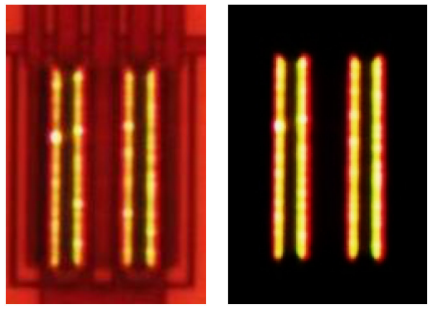


Fig. 5. Light-emitting graph of All-Silicon LED (Left: brightfield/Right: darkfield).

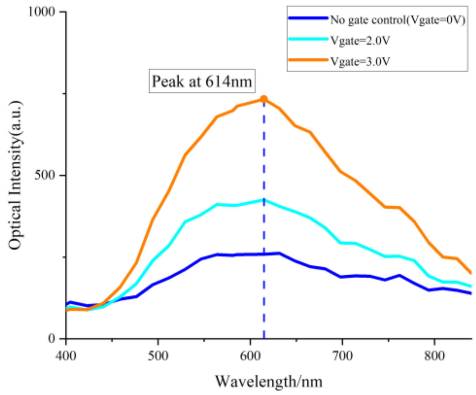


Fig. 6. Emission spectrum with different Vgate.

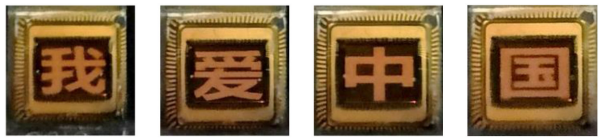


Fig. 7. Actual display of the all-silicon LEDs.

The spectrum difference between 'gate control' and without 'gate control' is shown in Fig. 6. We re-measured the spectrum to show the effect of 'gate control' on the luminous intensity. Among them, the two sets of data with 'gate control' operate at voltage of 2.0V, and the set of data without 'gate control' operate at voltage of 6.0V, because it is difficult to observe the emission spectrum of the all-silicon LED at a lower voltage under this condition.

By integrating the designed all-silicon LED as a light-emitting unit into a 100×100 pixel array, we finally realized the microdisplay device. The display result shown in Fig. 7. was taken by a LEICA camera with exposure time of 4s. The meaning of the Chinese characters in the picture is 'I love China'. It shows the actual display effect of the all-silicon LED microdisplay device. The actual luminous intensity of the device can be estimated by the following formula:

$$LUX = \frac{E_p \frac{L_1}{L_2}}{S} \tag{6}$$

where Ep is the output light power of the reference light source, L_1 and L_2 are the light emission intensity of the pixel unit and

the reference light source respectively, and S is the light-emitting area of the pixel unit. The actual luminous intensity of the calculation device is about 368mW/mm^2.The size of the fabricated microdisplay device is 6.2mm$\times$5.0mm and the minimum pixel center distance is 42 μm, which belongs to the category of microdisplay.

For other characteristics of the fabricated microdisplay device, we have also done some targeted tests. In terms of temperature tolerance, when the voltage is stable, the device can operate stably in the normal temperature range (10-30°), and the working current will have a slight change; the external quantum efficiency is about 10^{-6}, which is comparable to those of other work on similar semi-conductor LEDs [23]; when the heat sink is added, the device can work stably for more than 1 hour, and the device's ultimate service life has not been tested. In order to improve the lifetime and stability of this device, it is possible to further reduce the operating voltage or add a heat sink. The specific effect awaits more experiments and tests.

IV. Conclusion

This article uses 0.18 standard CMOS technology to successfully design and fabricate a low operating voltage MOS-like gate-control all-Silicon light emitting device, and fabricate a microdisplay devices based on 100$\times$ 100 pixel array of this LED using the same CMOS technology. The remarkable feature is that there is no need to make any changes to the CMOS process, and the proposed 'gate control' method can improve avalanche efficiency, reduce operating voltage and increase luminous efficiency, which make it possible to share the power supply with other CMOS circuits. We are thus looking forward to make this device play an irreplaceable role in the field of microdisplay.

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