Improved Noise Performance of CMOS Poly Gate Single-Photon Avalanche Diodes

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***Abstract*—The noise performance of three types of n^+/p-well single-photon avalanche diodes (SPADs) fabricated in a standard 180 nm CMOS technology is studied. The SPADs had different poly gate configurations: no poly gate (SPAD_NG), a dummy floating poly gate (SPAD_DG), and a field poly gate connected to the n^+ cathode (SPAD_FG). The measurement results of dark count rate and afterpulsing showed that the SPAD_DG had better noise performance compared to the SPAD_NG. This is because the dummy poly gate pushed the shallow trench isolation away from the active region of the SPAD, thus reducing the dark noise generated from the Si-SiO_2 interface. The measurement results also revealed that the noise performance can be further improved by connecting the poly gate to the n^+ cathode. The voltage on the poly gate in SPAD_FG reduced the electric field in the n-well guard ring (GR) region, thus reducing the carriers from the GR region that can enter the active region of SPADs and initiate dark counts.**

***Index Terms*—Single photon avalanche diode (SPAD), guard ring, poly gate, dark count rate (DCR), afterpulsing (AP).**

I. Introduction

WITH the advances in silicon fabrication technologies, single photon avalanche diodes (SPADs) fabricated in complementary metal-oxide-semiconductor (CMOS) processes are being more commonly used in applications such as biomedical imaging (diffuse optical imaging [1], Raman spectroscopy [2], positron emission tomography [3], fluorescence lifetime imaging microscopy [4], etc.), light detection and ranging [5] and optical wireless communications [6]. That is because CMOS SPADs have lower fabrication cost and can be easily integrated with other CMOS circuits to form complete and compact systems compared to SPADs in custom technologies. For Geiger-mode operation, the SPAD is biased in excess of the breakdown voltage, so guard rings (GRs) are generally used to prevent premature edge breakdown (PEB). However, GRs can increase the total area of an SPAD, thus reducing its fill factor. More importantly, the GR structure can significantly affect the SPAD's noise performance.

There are several options for GRs of SPADs in CMOS processes to prevent PEB. One solution uses shallow trench isolation (STI) to confine the edges of the depletion region [7]. However, such SPADs suffer from high dark noise due to the high density of defects at the Si-SiO_2 interface during the formation of STI. To mitigate this issue, diffusion GR structures are preferred. For example, n-well diffusion GRs were used for n^+/p-well junctions [8], [9] and p-well diffusion GRs were used for p^+/n-well junctions [10], [11]. The lower doping in the diffusion GRs widens the depletion regions at the edges of SPADs to locally decrease the electric field, thus preventing PEB. Another alternative are virtual GRs: the retrograde doping profile that is created from the deep n-well (DNW) to the surface during the formation of the DNW [12]; or lower doping concentration due to the diffusion between DNWs [13]. The results in [12], [13] showed that the virtual GRs can effectively prevent PEB.

Another interesting approach for GRs uses the polysilicon layer, typically used for the poly gates of MOSFETs. It is known that there is a higher defect density at the Si-SiO_2 interface during the formation of STI, which contributes to the source of the dark noise [7]. In CMOS planar technologies, STIs are originally used to isolate the NMOS and PMOS transistors to prevent latch-up and punchthrough effects. As a general rule in CMOS processes, all p^+ and n^+ active areas are surrounded by STIs except when they are abutted with poly layers. That is to say, STI will not be formed underneath the ploy gate layer in standard CMOS processes. Therefore, the floating poly gates are used as a stop mask in the SPAD design to prevent the formation of the STI near the depletion region of the SPAD in early days [14], [15]. That is, the poly gate helps to push the STI away from the depletion region of the SPAD so as to reduce the dark noise. The function of the floating poly gate has been investigated in both p^+/n-well and n^+/p -well SPADs [14], [15]. Recently, it was found that the noise performance can be further improved by applying negative voltages on the poly gates of p^+/n-well SPADs [16], [17]. A perimeter-gated p^+/n-well SPAD in a 0.5 μm CMOS process designed with a lateral diffusion n-well guard ring and a perimeter gate over the edge of active region was reported in [16]. By applying a negative voltage on the perimeter gate, the electric field at the edge of the SPAD was reduced, thus preventing PEB. The DCR was also reduced in this perimeter-gated SPAD (PGSPAD) due to the voltage on the gate. Based on the PGSPAD, a SPAD pixel that includes active quench and reset circuit [18], an analog

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silicon photomultiplier (SiPM) [19], a digital SiPM [20] and a model for the SiPM [21] were further developed. However, the operation of this perimeter-gated structure requires an extra pin to bias the gate. In addition to a common p^+/n-well SPAD with a n-well diffusion GR, the researchers in [17] presented another two types of SPADs in a 180 nm BCD (Bipolar-CMOS-DMOS) process: one p^+/n-well SPAD with a dummy floating gate, and a p^+/n-well SPAD with a field poly gate connected to its p+ anode. The measurement results showed that noise performance of SPAD was improved by adding the dummy poly gate, and was improved further by connecting the poly gate to the anode. The current research on the function of poly gate in SPAD are all based on p^+/n-well SPAD. However, whether the poly gate can be used in n^+/p-well SPADs to improve the noise performance has not been reported.

To investigate this issue, we designed and measured three types of n^+/p-well SPADs with different configurations of the poly gate layer using a standard 180 nm CMOS process. To the authors' knowledge, this is the first work to report the design and dark noise improvements of n^+/p-well field poly gate SPADs. Compared to the poly gate SPADs in the expensive BCD process [17], SPADs designed in this work use a low-cost standard 180 nm CMOS process, thus decreasing the fabrication cost. In future, these CMOS SPADs can be easily integrated with CMOS peripheral circuits for further signal processing. After comparing the measured DCR and afterpulsing (AP) of these three SPADs at different excess voltages and at different temperatures, we found that the dummy poly gate reduces the DCR up to 48.7% and AP up to 40% when compared to the SPAD without poly gate. The DCR and AP can be further reduced in the field gate structure.

II. SPAD Design

A. SPAD Structure

Fig. 1 shows the cross-sectional views of three types of SPADs studied in this work. Fig. 1(a) shows the design of a traditional n^+/p-well SPAD with only a n-well diffusion GR. The n^+ layer is designed to extend by 0.5 µm into the n-well diffusion GR, pushing the shallow trench isolation (STI) away from the active region to reduce the dark noise. This SPAD with no poly gate layer is named SPAD_NG. The SPAD shown in Fig. 1(b) has the same structure except a dummy poly gate that is placed on top of the n-well diffusion region. Because the poly gate is floating during the operation of the SPAD, it is named SPAD_DG (i.e., dummy gate). Compared to SPAD_DG, the third type of SPAD shown in Fig. 1(c) has the same structure but the poly gate is connected to the n^+ cathode. In this structure, the poly gate in the SPAD functions like a field gate in a MOSFET which can change the electric field under of the poly gate, thus leading to its given name: SPAD_FG. It is worth noting that no STI is formed underneath the poly gate layer in SPAD_DG and SPAD_FG. Therefore, the distances between the STI and the depletion region increase to ∼1.4 µm in SPAD_DG and SPAD_FG. All SPADs have a circular shape with a diameter of 12.4 µm and were fabricated in a standard 180 nm CMOS process.

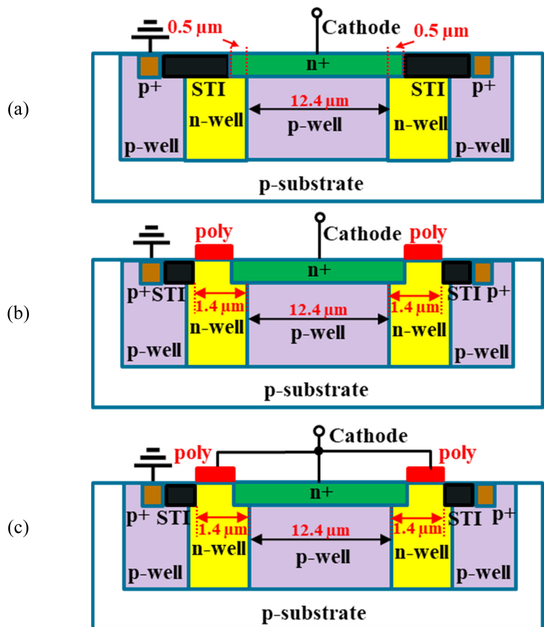

Fig. 1. Cross-sectional views of (a) of SPAD_NG (n^+/p-well SPAD without poly gate), (b) SPAD_DG (n^+/p-well SPAD with dummy poly gate) and (c) SPAD_FG (n^+/p-well SPAD with field poly gate).

B. TCAD Simulation

Technology computer-aided design (TCAD) simulations were performed using Sentaurus Device to show differences in the electric field distributions of three types of SPADs. The doping concentration parameters used in the simulation are based on Ref. [22], and are 5×10^{19} cm^{-3} for the n^+ and p^+ layers, 1.3×10^{17} cm^{-3} for the n-well, 2×10^{17} cm^{-3} for the p-well and 1.3×10^{15} cm^{-3} for the p-substrate. For the simulation, silicon dioxide (SiO_2) is used to form the STI. The simulation results are shown in Fig. 2 when the SPAD is biased at the measured breakdown voltage of 12.3 V. Since all three SPADs have the same core junction structure, a n^+/p-well junction with a n-well diffusion guard ring, the simulation results showed that the electric field distributions for the three types of SPADs are nearly identical in the central depletion region. However, the electric fields near the edges are different due to their different configurations of the poly gate (see detailed analysis in Section III). As shown in Fig. 2, the lower electric fields at the edge of the depletion regions demonstrates the effectiveness of the n-well guard ring for all three SPADs in preventing PEB.

III. Experimental Results and Discussion

Before the detailed measurements, the DCR of 5 SPAD samples each (SPAD_NG and SPAD-DG/SPAD-FG) were measured at room temperature with a 0.5 V excess voltage first. The SPAD structures with a median value of DCR were chosen to perform detailed measurements to compare their noise performance at different excess voltages (0.3 V to 0.7 V with a step size of 0.1 V) and different temperatures (−30 °C to 30 °C with a step size of 15 °C). As stated in Section II (SPAD structure), SPAD_DG and SPAD_FG have the same structure except for

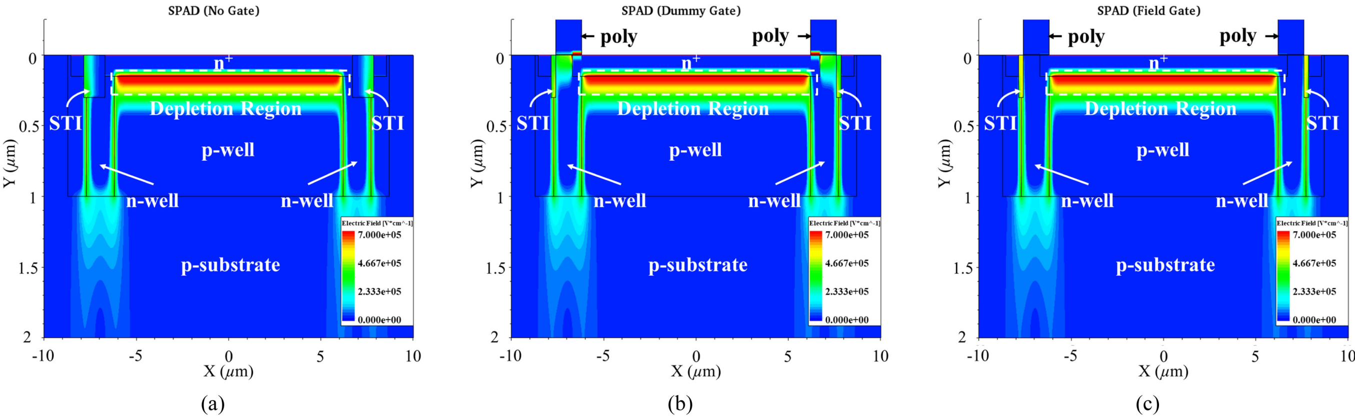

Fig. 2. TCAD electric field simulations with a 12.3 V bias for (a) SPAD_NG (n+/p-well SPAD without poly gate), (b) SPAD_DG (n+/p-well SPAD with dummy poly gate) and (c) SPAD_FG (n+/p-well SPAD with field poly gate).

their poly gate connection. To eliminate the effect of process variations when comparing the performance of SPAD_DG with SPAD_FG, the same SPAD is used for all measurements. The poly gate is floating when used as SPAD_DG, but is connected to the n^+ cathode externally on the printed circuit board level when used as SPAD_FG.

A. Breakdown Voltage

The breakdown voltage (V_{BR}) of a SPAD is defined as the reverse bias voltage that leads the electric field across the junction to reach a critical level to cause self-sustaining avalanches. It can be measured through the reverse current-voltage (I-V) characteristic. In this work, V_{BR} is the voltage at the onset of the rapid rise in the current, which corresponds to the point of the maximum derivative of the I-V characteristic.

The $V_{BR}s$ of the three types of SPADs were first measured to ensure proper Geiger-mode operation. A Semiconductor Device Analyzer (Agilent B1500A) was used to measure their I-V characteristics to get V_{BR}. To the determine temperature dependence of the SPAD's performance, the measurements were performed from −30 °C to 30 °C in steps of 15 °C. Since the V_{BR} for SPAD_DG and SPAD_FG were measured on the same n^+/p-well junction, they showed almost the same $V_{BR}s$. SPAD_NG shows slightly higher breakdown voltages than the other two SPADs. Samples of the I-V characteristics for these three SPADs at 15 °C are shown in Fig. 3(a). At 15 °C, V_{BR} is 12.18 V for SPAD_NG while V_{BR} is 12.14 V for SPAD_DG and SPAD_FG. The temperature dependences of the V_{BR} are shown in Fig. 3(b).The temperature coefficients of the breakdown voltages were obtained from the slopes of linear fits of breakdown voltages as a function of temperature [23], [24], which are 12.3 mV/°C for SPAD_DG, 11.6 mV/°C for SPAD_DG and SPAD_FG.

B. Dark Count Rate (DCR) and Afterpulsing (AP)

The measurement setup for DCR and AP is shown in Fig. 4(a). The SPAD is passively quenched through an on-chip 50 kΩ resistor connected to the cathode. Another terminal of the quench resistor is connected to a DC voltage source (Agilent E3646A).

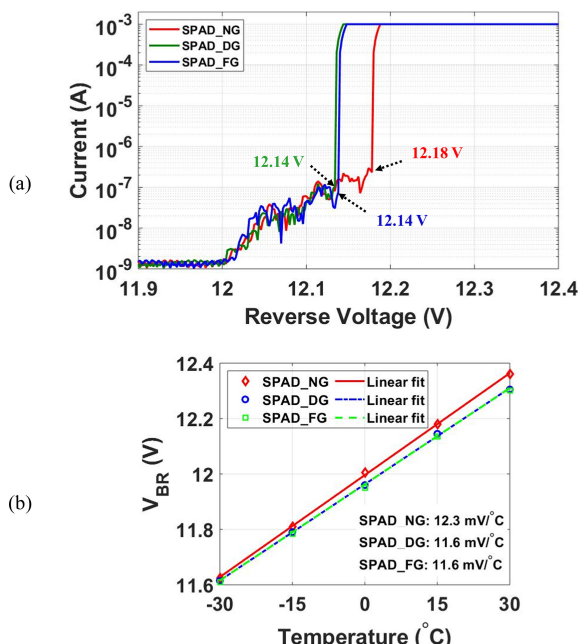

Fig. 3. (a) Samples of I-V characteristics for three SPAD at 15 °C. Note that the x-axis is 0.5 V width to clearly show the breakdown voltages. (b) Breakdown voltages as a function of temperature for three SPADs.

The anode of the SPAD is grounded. Then, the output signal from the cathode is sent to a high-speed oscilloscope (LeCroy WaveRunner 625Zi) to measure the inter-arrival time (IAT) between the avalanching pulses. Fig. 4(b) presents an illustration of the IAT measurement. Note that the avalanche pulses in Fig. 4(b) are negative pulses. In the illustration, t_n represents the time difference n^{th} pulse and $(n+1)^{th}$ pulse. For example, t_1 stands for the time between the 1st pulse and the 2nd pulse. After obtaining the histogram of IAT, the DCR and AP can be derived through the exponential fits. The first-order exponential fit represents the primary dark count and the area deviating from the first-order exponential fit represents the AP, as shown in Fig. 4(c). The details of the IAT method for the AP measurement can be found in [25]. Fig. 5 shows an example of the experimental

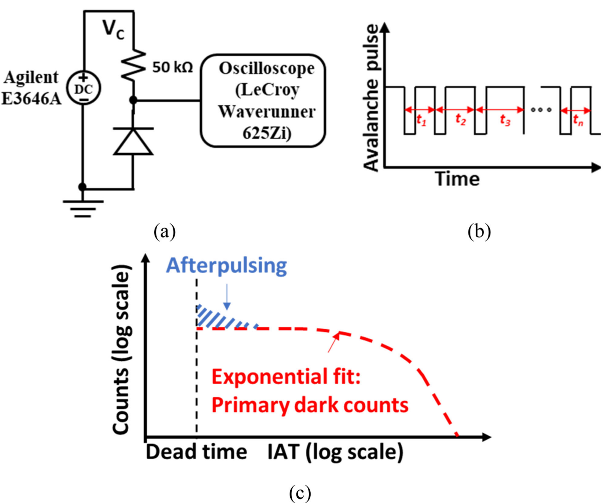

Fig. 4. (a) Measurement setup of dark count rate (DCR) and afterpulsing (AP) for the passively quenched SPAD. (b) Illustration of inter-arrival time (IAT) of the SPAD output pulses. Avalanche pulse is a negative pulse in the illustration. (c) Illustration of the histogram of IAT to show the component of DCR and AP.

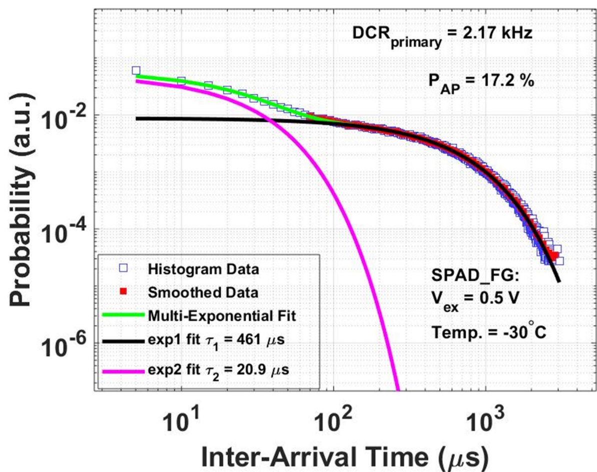

Fig. 5. The histogram of the IAT from the real measurement data to show the DCR and AP of the SPAD_FG with 0.5 V excess voltage at −30 °C.

data that was measured on SPAD_FG with 0.5 V excess voltage. The measurement was performed at a low −30 °C in order to show an obvious AP. As shown in Fig. 5, a multi-exponential fit is applied on the histogram of IAT. The primary term of the exponential fit gives the DCR of 2.17 kHz and the AP has a large value of 17.2% due to the low operating temperature.

The DCR and AP measurements were done at different excess voltages (0.3 V to 0.7 V with a step size of 0.1 V) and different temperatures (−30 °C to 30 °C with a step size of 15 °C). Note that the breakdown voltage temperature coefficient was considered to ensure consistent excess voltages at different temperatures. The measurement results of DCR as a function of excess voltage (V_{ex}) at three different temperatures (15 °C, 0 °C and −15 °C) for the three SPADs are shown in Fig. 6. Using the DCR of SPAD_NG as the baseline, Fig. 6(a) shows the DCR comparison of SPAD_DG with SPAD_NG while Fig. 6(b) shows the DCR comparison of SPAD_FG with SPAD_NG. They

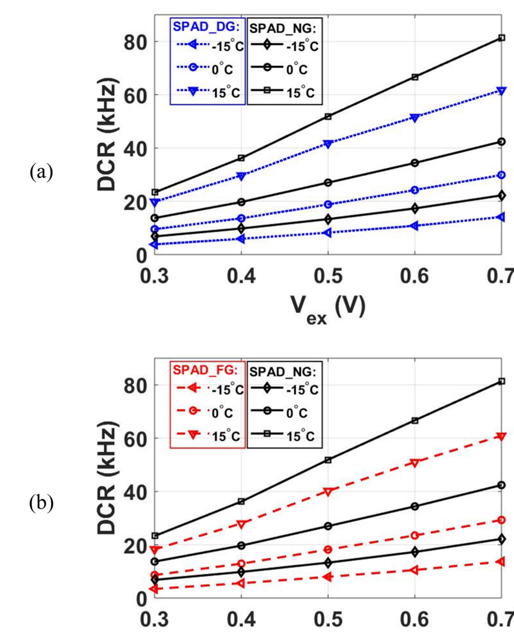

Fig. 6. Comparison of the DCR of SPAD_NG with (a) SPAD_DG and (b) SPAD_FG at different excess voltages and at different temperatures.

TABLE I
DCR Comparsion Between SPAD_NG and SPAD_DG: [DCR(SPAD_NG)-DCR(SPAD_DG)]/DCR(SPAD_NG) × 100 (%)

Temp. (°C)	Excess Voltage (V)				
	0.3	0.4	0.5	0.6	0.7
-30	48.7	47.8	44.5	44.4	40.7
-15	43.8	39.4	38.2	37.6	36.5
0	30.5	31.0	30.4	29.7	29.5
15	15.0	18.0	19.5	22.6	24.1
30	3.4	7.7	13.8	14.5	16.6

all show similar trends: DCR increases with excess voltages and operating temperatures. However, it is seen that SPAD_DG and SPAD_FG can significantly reduce the dark noise when compared to SPAD_NG.

Table I shows the DCR comparison between SPAD_NG and SPAD_DG at different excess voltages and temperatures. The values in Table I are calculated using $[\mathrm{DCR(SPAD_NG)} - \mathrm{DCR(SPAD_DG)}]/\mathrm{DCR(SPAD_NG)}$. The calculation results show that DCR of SPAD_DG is reduced by almost two times at −30 °C when compared to SPAD_NG. As shown in Fig. 1(a), the n^+ layer in SPAD_NG is extended by 0.5 µm into the n-well guard ring. Therefore, the distance between the Si-SiO_2 interface and the edge of the depletion region in SPAD_NG is 0.5 µm. However, the dummy poly gate layer on top of the n-well guard ring in SPAD_DG stops the formation of the STI underneath the poly gate, thus moving the STI away from the n^+ layer. As shown in Fig. 1(b), the distance between the Si-SiO_2 interface and the edge of the depletion region in SPAD_DG increases to ∼1.4 µm. As a

TABLE II
DCR COMPARSION BETWEEN SPAD_NG AND SPAD_FG: [DCR(SPAD_NG)-DCR(SPAD_FG)]/DCR(SPAD_NG) × 100 (%)

Temp. (°C)	Excess Voltage (V)				
	0.3	0.4	0.5	0.6	0.7
-30	52.8	50.7	46.9	45.3	41.5
-15	49.7	43.1	40.3	39.3	38.3
0	37.1	34.5	32.6	31.7	30.9
15	21.5	22.7	22.5	23.5	25.1
30	11.6	12.4	16.1	16.2	18.3

result, carriers generated from the high density of defects at the Si-SiO_2 interface in SPAD_DG are less likely entering the depletion region to trigger an avalanche. Therefore, the DCR of SPAD_DG is reduced compared to SPAD_NG. The comparison between SPAD_NG and SPAD_DG agrees with the research findings in [26] that the DCR reduces as the gap between the STI and the depletion region increases. Note that as the temperature increases, the DCR improvement of SPAD_DG compared to SPAD_NG is reduced. For example, the DCR reductions at -30 °C are more than 40% while DCR reductions at 30 °C show much smaller values ($< 20\%$). This result implies that at higher temperatures, the noise contribution from the planar depletion region to the total dark noise is larger than carriers diffusing from the guard rings.

Table II shows the DCR comparison between SPAD_NG and SPAD_FG at different excess voltages and at different temperatures. The values in this table are calculated using $[\mathrm{DCR(SPAD_NG)} - \mathrm{(SPAD_FG)}]/\mathrm{DCR(SPAD_NG)}$. Compared to Table I, the values in Table II are better (∼2 -10%), which indicates that SPAD_FG shows further reduction in DCR. As described in Section II of SPAD structure, SPAD_DG and SPAD_FG have the same structure except the poly gate connection. Similar to SPAD_DG, the poly gate in SPAD_FG also causes the STI to be pushed away from the active region of the SPAD. As shown in Fig. 1(c), the distance between the Si-SiO_2 interface and the edge of the depletion region in SPAD_FG is also ∼1.4 µm. In addition, the poly gate connected to the cathode of SPAD_FG reduces the electric field distribution near the n-well guard ring. Fig. 7 shows TCAD simulations focussed on the edges between the n-well guard ring and depletion region for SPAD_DG and SPAD_FG when the SPAD is biased at the measured breakdown voltage of 12.3 V. The simulation results show that the field poly gate in SPAD_FG helps to suppress the electric field in the region of n-well guard ring when compared to SPAD_DG since it ensures that there is no voltage difference between the poly gate and the semiconductor located underneath. The reduced electric field at the n-well guard ring of SPAD_FG improves the effectiveness of the guard ring, and lowers the probability that carriers in the guard ring region can enter the depletion region, thus reducing the DCR.

The implementation of field gate in the SPAD structure does not require extra customized masks in a standard CMOS process, or an additional pin to bias the field gate since it is connected to the cathode. Therefore, to reduce DCR, it is beneficial to

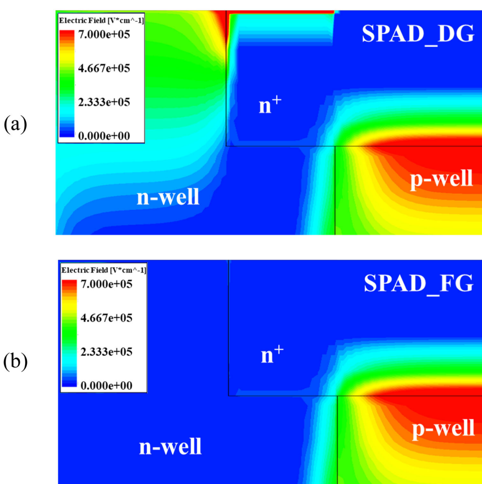

Fig. 7. TCAD electric field simulations with a 12.3 V bias for at the edge of depletion region of (a) SPAD_DG and (b) SPAD_FG.

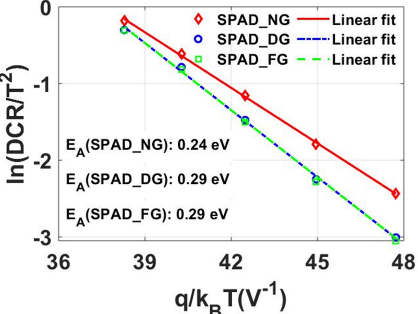

Fig. 8. Arrhenius plots of three SPADs with 0.5 V V_{ex}.

implement the SPAD_FG structure when designing n+/p-well SPADs with a poly gate.

The DCR of SPADs can be expressed as a function of temperature using the Arrhenius equation, given by [27]

$$DCR \propto T^2 \exp\left(-\frac{E_A}{k_B T}\right) \tag{1}$$

where E_A is the activation energy, k_B is Boltzmann's constant, and T is the absolute temperature in Kelvin. By taking the natural logarithm on Eq. 1, we get that $ln(DCR/T^2)$ has a linear relationship to $1/k_B T$. The slope of this linear fit gives the activation energy E_A. The Arrhenius plots of the three SPADs at 0.5 V excess voltage are shown in Fig. 8, and the E_A is 0.24 eV for SPAD_NG, and 0.29 eV for both SPAD_DG and SPAD_FG. The small values of the activation energy in all three SPADs indicate that the trap-assisted tunneling noise is likely the dominant source for the dark noise in the measured temperature range (-30 to 30 °C).

The measurement results of AP as a function of V_{ex} at three different temperatures (15 °C, 0 °C and -15 °C) for the three SPADs are shown in Fig. 9. Using the AP of SPAD_NG as the baseline, Fig. 9(a) shows the AP comparison of SPAD_DG with SPAD_NG while Fig. 9(b) shows the AP comparison of SPAD_FG with SPAD_NG. It is seen that AP increases

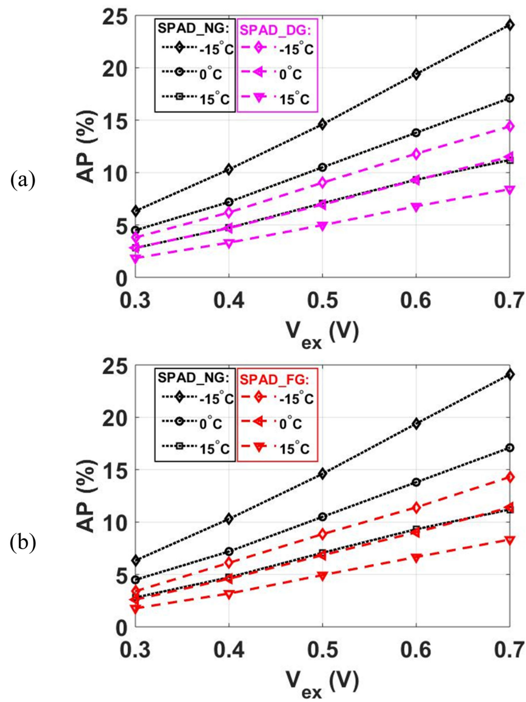

Fig. 9. Comparison of the AP of SPAD_NG with (a) SPAD_DG and (b) SPAD_FG at different excess voltages and at different temperatures.

as temperature decreases. This is because that the lifetime of trapped carriers in the trap centers increases exponentially as temperature decreases, thus resulting in a higher probability for carriers released from the trap centers to generate a secondary pulse. As for the dependence on excess voltage, the measurement results indicate that the AP has a linear relationship to the excess voltages at different temperatures for all three SPADs. This linear relationship can be interpreted using the model described in [28] as

$$P_{AP} \approx (CN_t\sigma_t W_e V_{ex})/q \tag{2}$$

where $P_{AP}$is the afterpulsing probability, C is the junction capacitance of the SPAD, N_t is the electron trap concentration, $\sigma_t$is the cross-section of the electron trap, and W_e is the effective depletion width. Note that SPAD_DG and SPAD_FG do not show the any AP at 30 °C. This means that lifetime of captured carries by the trap centers of SPAD_DG and SPAD_FG at 30 °C are small enough so there is negligible generation of secondary pulses.

The detailed comparison of AP between the three SPADs are shown in Tables III and IV, which demonstrates similar trends as DCR. Compared to SPAD_NG, SPAD_DG showed improved performance of AP as shown in Table III. For example, the AP reduction is as high as 40% at 0.3 V V_{ex} and -15 °C. Compared to Table III, the values in Table IV are better (more reduction), which indicates AP performance of SPAD_FG was further improved when compared to SPAD_DG. As stated in the section on DCR, the field gate in SPAD_FG not only pushes the STI away from the active region of SPAD, but it also reduces the electric field at the edge of the depletion region. This leads to a reduction in carriers diffusing from the guard ring region into the depletion region, thus resulting in the best AP performance among the three SPADs.

TABLE III
AP Comparsion Between SPAD_NG and SPAD_DG: [AP(SPAD_NG)-AP(SPAD_DG)]/AP(SPAD_NG) × 100 (%)

Temp. (°C)	Excess Voltage (V)				
	0.3	0.4	0.5	0.6	0.7
-30	17.7	13.2	12.3	12.8	13.9
-15	40	39.9	38.2	39.2	40.2
0	37.2	34.6	33.9	32.7	32.7
15	34.3	29.9	29.6	27.3	24.9

TABLE IV
AP Comparsion Between SPAD_NG and SPAD_FG: [AP(SPAD_NG)-AP(SPAD_FG)]/AP(SPAD_NG) × 100 (%)

Temp. (°C)	Excess Voltage (V)				
	0.3	0.4	0.5	0.6	0.6
-30	24.3	17.1	15.7	16.3	14.6
-15	46.3	40.7	39.4	41.2	40.7
0	42.1	36.2	34.9	34.6	33.3
15	36.8	32.6	30.1	28.5	25.6

C. Photon Detection Probability

The photon detection probability (PDP) is defined as the ratio of the photon count rate detected by the SPAD to the incident photon rate. The measurements of the PDP were performed on three SPADs at the same excess voltage of 0.5 V. A Xenon lamp provides a continuous light source for the PDP measurement. Optical bandpass filters are used to select the wavelength while neutral density filters are used to control the intensity of light to avoid saturation. The integrating sphere is used to generate evenly distributed incident light. A Newport 818-SL wavelength calibrated silicon photodetector (SiPD) connected to a Newport 1830-C optical power meter is used to measure the incident optical power to estimate the number of incident photons on the SPAD area per unit of time. Then, the total count rate is recorded using the LeCroy digital oscilloscope. The real photon count rate is obtained by subtracting the DCR at 0.5 V excess voltage from the total count rate. The ratio of SPAD pulses from photons to the total number of incident photons gives the PDP. The measured PDPs as a function of wavelength for three SPADs with the same excess voltage of 0.5 V are shown in Fig. 10. The measurements show that three SPADs have almost the same PDP. The peak PDPs for the three SPADs are $\sim$ 7.35% at 560 nm. These results are expected since the three SPADs have the same core junction structure - n^+/p-well junction with n-well guard ring as shown in the cross-sectional views in Fig. 1. Therefore, they have the same quantum efficiencies and the same avalanche triggering probabilities at the same excess voltages, thus leading to almost the same response of PDP.

TABLE V
COMPARISON OF OUR SPADs TO OTHER SPADs FABRICATED IN RECENT LITERATURE

Ref., Year	Tech. (nm)	Junction	Active area (μm)	Guard ring	V_{BR} (V)	DCR (cps/μm^2) @ V_{ex} (V), T (℃)	AP (%) @ V_{ex} (V), T (℃)	Peak PDP (%) @ λ (nm), V_{ex} (V),
Non-standard CMOS Process								
[10], 2014	180 nm CMOS	p^+/DNW	12 (Circular)	p-well	23.5	0.15 @ 3, 25 12.84 @ 10, 25	0.03 @ 2, 25 0.3 @ 10, 25	23 @ 480, 2 47 @ 480, 10
[11], 2015	180 nm CMOS	p^+/n-well	12 (Circular)	p-well	14.64	16 @ 4, 25	0.2 @ 4, 25	24 @ 480, 1 47 @ 480, 4
[30], 2018	180 nm HV CMOS	p^+/shallow n-well	12.08 (Square)	shallow p-well	16.8	0.19 @ 1, 25 1.49 @ 4, 25	-	55 @ 480, 4
[31], 2018	180 nm CMOS	p-well/p-epi/BN	16.38 † (Circular)	PW lateral diffusion and low doping p-epi	25.46	0.26 @ 4, 25	-	41 @ 520, 3 # 55 @ 520, 11 #
[17], 2020	180 nm BCD	p^+/n-well	10 (Circular)	p-well	11.55	6.34 @ 1, 22	-	-
				p-well and poly gate (floating)	11.85	4.82 @ 1, 22	-	-
				p-well and poly gate (connected to p^+ anode)	11.4	2.37 @1 V, 22	-	-
Standard CMOS Process								
[32], 2013	65 nm stand. CMOS	n+/p-well	8 (Octagonal)	n-well and poly gate (floating)	9.1	15.6 k @ 0.4, 20	1 @ 0.4, 25	5.55 @ 420, 0.25
[33], 2018	65 nm stand. CMOS	p+/n-well	20 (32-sided polygon)	p-well	9.9	2.8 k @ 1.5, 25	<10 @ 1.5, 25	8 @ 470, 1.5
[27], 2021	65 nm stand. CMOS	n+/p-well	10 (Square *)	STI	9.52	138 k @ 0.3, 25	<1 @ 0.3, 25	7.3 @ 440, 0.3 #
[29], 2008	180 nm stand. CMOS	p^+/n-well	10 (Octagonal)	p-well	10.2	685 @ 0.5, 20	-	2.5 @ 420, 0.5
This work	**180 nm stand. CMOS**	**n^+/p-well**	**12.4 (Circular)**	**n-well**	**12.18**	**430 @ 0.5, 15 685@ 0.5, 25**	**7.07 @ 0.5, 15 0 @ 0.5, 25**	**7.35@ 560, 0.5**
				n-well and poly gate (floating)	**12.14**	**346 @ 0.5, 15 635@ 0.5, 25**	**4.98 @ 0.5, 15 0 @ 0.5, 25**	**7.35@ 560, 0.5**
				n-well and poly gate (connected to n^+ cathode)	**12.14**	**333 @ 0.5, 15 629@ 0.5, 25**	**4.94 @ 0.5, 15 0 @ 0.5, 25**	**7.35@ 560, 0.5**

*. Square with 45° corners.
†. The active area was not reported. The value of 16.38 μm is the pixel pitch in a 512 × 512 SPAD array.
#. Values are read from or calculated based on the curves.

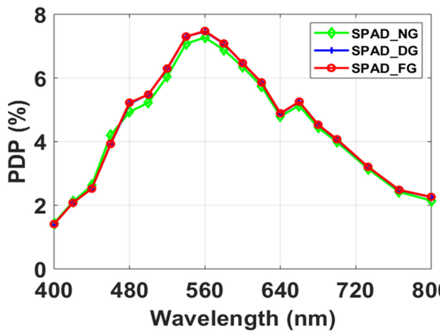

Fig. 10. Photon Detection Probability (PDP) as a function of wavelength with an excess voltage of 0.5 V.

D. *Performance Summary and Comparison*

Table V, a summary of the properties and noise performance of the three SPAD designs (last row) and a comparison to other SPADs in recent literature is given. However, note that only [29] used a similar process to ours. The n^+/p-well SPADs in this work show better noise performance than other SPADs fabricated in standard CMOS processes. However, the DCR of these three SPADs are higher than SPADs in other non-standard processes. Several reasons could be responsible for the higher dark noise. First, the three SPADs in this work are implemented in a fully standard CMOS process and no special layers such as buried-N layer in [10], [11] and [17], or deep p-well layer [30] are available to isolate the active region of SPADs from the noisy bulk. Second, even though the DNW is available in this 180 nm process, it cannot be used in this n^+/p-well SPAD design since the bottom of the n-well reaches the DNW in this process. As shown in Fig. 1, if the DNW was placed underneath the p-well to isolate the active region of the SPAD from the p-substrate, the n-well guard ring will touch the DNW, thus making the p-well anode of the SPAD inaccessible. Third, compared to breakdown voltages of the SPADs with a very low DCR (23.5 V in [10], 16.8 V in [30], 25.46 V in [31]), the three n^+/p-well SPADs in this work have a relatively low breakdown voltage (∼12.1 V). This means that the doping concentrations of the n^+ layer and p-well in this 180 nm standard CMOS process are higher, thus leading to a thinner depletion region and a higher probability for tunneling noise, which is in agreement with the low activation energy values for three SPADs shown in Fig. 8.

The comparison between the three SPADs in this work proves the effectiveness of a field gate in n^+/p-well SPADs to prevent PEB and to reduce the primary DCR and AP. Also, since these SPADs are designed in a standard 180 nm process, they can be easily integrated with other CMOS signal processing and conditioning circuits to form a complete imaging system with lower costs and very good overall performance.

IV. Conclusion

We designed and fabricated three types of n^+/p-well SPADs with different poly gate configurations: no poly gate (SPAD_NG), a dummy floating poly gate (SPAD_DG), and a field poly gate connected to the n^+ cathode (SPAD_FG) in a low-cost standard 180 nm CMOS process. Based on these three types of SPADs, the TCAD simulations were performed to show the effectiveness of the guard rings to prevent premature edge breakdown (PEB). The dark count rate (DCR) and afterpulsing (AP) of these three SPADs operating at different excess voltages and at different temperatures were measured and compared. The comparison of measurement results between SPAD_NG and SPAD_DG or SPAD_FG reveal that poly gate greatly helps to reduce the DCR and AP. This is because the presence of the poly gate over the n-well guard ring pushes the noisy Si-SiO_2 interface of the STI away from the active region of the SPAD. The best results were obtained from SPAD_FG because the voltage on the poly gate reduces the magnitude of the electric field distribution in the guard ring region, as shown from the TCAD simulation. The reduced electric field decreases the likelihood that carriers in the guard ring can enter the active region of the SPAD and initiate the dark counts, resulting in improved the noise performance. In addition, SPAD_FG in this work is implemented in a standard CMOS process, which does not require extra mask layers in the fabrication nor an additional pin for biasing the SPAD, thus reducing the effort for integration of SPADs with other CMOS signal conditioning and processing circuits. Overall, this work verifies that the n^+/p-well field gate SPAD is an effective structure for improving the noise performance of CMOS SPADs.

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