Fabrication and Characterization of Low-Threshold Single Fundamental Mode VCSELs With Dielectric DBR Mirror

Pingping Qiu, Bo Wu, Pan Fu, Ming Li, Yiyang Xie, and Qiang Kan

***Abstract*—The SiO_2/SiN_x dielectric film stacks deposited by inductively coupled plasma chemical vapor deposition (ICP-CVD) are employed on the top of the oxide-confined vertical-cavity surface-emitting lasers (VCSELs). The reflecting mirror characteristics of the dielectric films are measured with varying numbers of pairs from 4 to 12. The prepared devices have low threshold current of 0.3 mA, single-mode peak power of 1.4 mW at room temperature. The thermal resistance of the device depending on ambient temperature is estimated according to the relationship of wavelength shift and dissipated power, allowing us to extract the actual temperature in active region and the temperature dependence of the output characteristics of the VCSEL. The beam property of the device is characterized by the far field pattern (FFP). Depending on the drive current, the average divergence angles of the output beam estimated from the full-width-half-maximum (FWHM) of the FFP varies between 20.4° and 21.2°. Furthermore, polarization-controlled single mode emission is achieved by introducing a built-in grating into the VCSEL with orthogonal polarization suppression ratio (OPSR) around 19 dB.**

***Index Terms*—Semiconductor laser, vertical-cavity surface-emitting lasers, dielectric distributed Bragg reflectors, single fundamental mode, polarization stable device.**

I. Introduction

VERTICAL-CAVITY surface-emitting lasers (VCSELs) are the promising optical sources for data communication, photonic integrated circuits, and sensing due to their low power consumption, low fabrication cost, high beam quality, and wafer-level testing [1]–[3]. Compared to the edge-emitting lasers, the cavity length of the VCSELs is extremely short, thus highly reflective reflectors (>99%) are required to obtain enough optical gain. Conventional VCSELs use epitaxially-grown semiconductor distributed Bragg reflectors (DBRs) as the bottom and top reflectors. Typically, it needs 25 to 40 pairs of semiconductor DBRs due to their low refractive index contrast [4], [5]. This leads to a high series resistance and thermal heating especially in the p-type DBRs. Besides, it suffers scattering from the dopants, and free-carrier absorption, which degrades the performance of the devices. However, dielectric DBRs, composed of dielectric film stacks e.g., a-Si/SiN_x, ZnS/MgF_2, SiO_2/SiN_x, can offer much higher index contrast and less absorption [6]–[8]. A few pairs of dielectric DBRs are enough for VCSEL to achieve lasing. More importantly, dielectric DBRs can be deposited after the epitaxial growth and during device fabrication, which increases the flexibility in the device design. For example, an index guide structure is introduced into the device for transverse mode control before depositing dielectric DBRs [9], [10].

There are a lot of methods for dielectric film deposition. Such as plasmas-enhanced chemical vapor deposition (PECVD), thermal evaporation, sputtering and inductively coupled plasma chemical vapor deposition (ICP-CVD) [11]–[14]. Thomas Maier *et al*. deposited SiO_2/SiN_x as top Bragg mirrors using PECVD. But, in order to obtain dense dielectric films with low optical losses, the sample was heated to 300°C during deposition. After that, extra etching process was performed to expose the pads for contacting [7]. In magnetron sputtering, the deposition rate can be accurately controlled thus the film thickness. C. Levallois *et al.* deposited a-Si/a-SiN_x using magnetron sputtering. An index contrast of 1.9 between a-Si and a-SiN_x was obtained. The reflectivity of four and a half periods of a-Si/a-SiN_x attains 99.5% at 1.55 μm [8]. Compared with sputtering or chemical vapor deposition, thermal evaporation is relatively gentle because material is deposited with comparatively low kinetic energy, and without introducing plasma in the chamber or corrosive chemical reactions. But to obtain good adhesion of dielectric films, tightly controlled temperature is required [6]. The dielectric films deposited by ICP-CVD have advantages of high density and good adhesion to substrate [14]. In particular, ICP-CVD produces high quality dielectric films at low deposition pressures and temperatures with low damage, which is compatible with the lift-off process of VCSELs.

In this work, we designed and experimentally demonstrated the low-threshold single fundamental mode VCSELs with dielectric DBR mirror. The SiO_2/SiN_x dielectric films

Manuscript received April 5, 2021; revised June 8, 2021; accepted June 12, 2021. Date of publication June 16, 2021; date of current version July 6, 2021. This work was supported in part by National Key R&D Program of China under Grant 2018YFA0209000, and in part by the National Natural Science Foundation of China under Grants 61604007 and 61741407. *(Corresponding author: Qiang Kan.)*

Pingping Qiu, Ming Li, and Qiang Kan are with the Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China, with the Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing 100049, China, and also with the Beijing Key Laboratory of Low Dimensional Semiconductor Materials and Devices, Beijing 100083, China (e-mail: ppqiu@semi.ac.cn; liming01@semi.ac.cn; kanqiang@semi.ac.cn).

Bo Wu, Pan Fu, and Yiyang Xie are with the Key Laboratory of Optoelectronics Technology, Beijing University of Technology, Beijing 100124, China (e-mail: wubo@emails.bjut.edu.cn; fupan1201@163.com; xieyiyang@bjut.edu.cn).

Digital Object Identifier 10.1109/JPHOT.2021.3089710

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

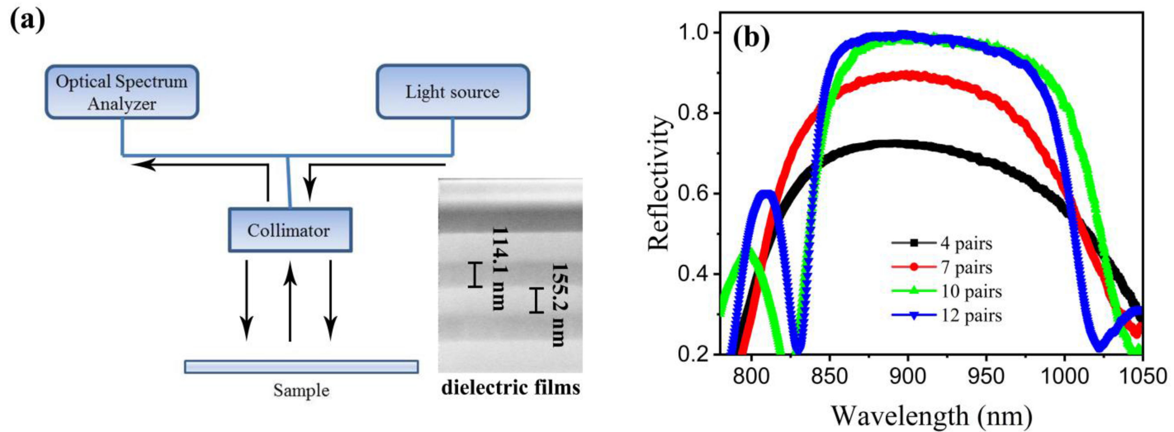

Fig. 1. (a) The spectral reflectance measurement setup and the cross-sectional SEM image of prepared SiO2/SiNx dielectric films. (b) Measured spectral reflectance of SiO2/SiNx dielectric films.

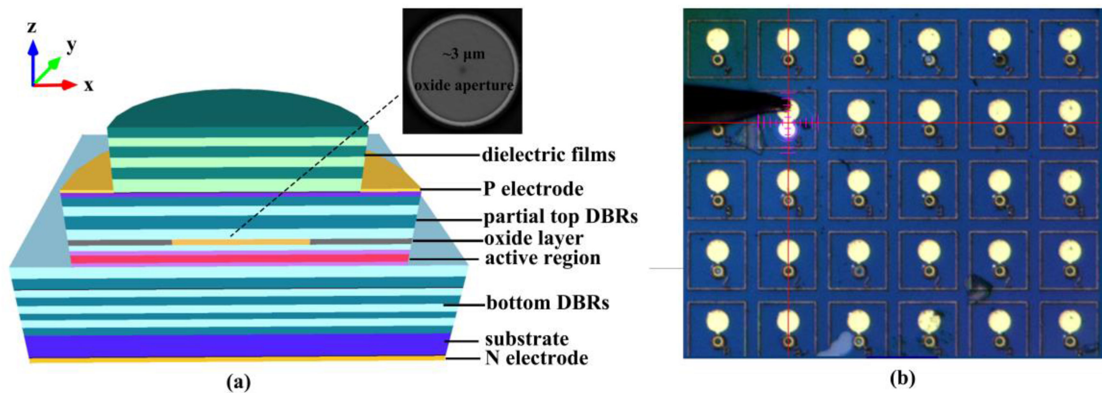

Fig. 2. (a) The schematic structure of VCSEL with SiO_2/SiN_x dielectric DBRs. (b) The microscope images of the fabricated VCSELs under wafer-level testing.

deposited by ICP-CVD were used to replace the conventional semiconductor DBRs. The prepared devices have low threshold current of 0.3 mA, single-mode peak power of 1.4 mW. The thermal behavior of the device is analyzed by estimating the thermal resistance according to the relationship of wavelength shift and dissipated power. And the beam property of the device is characterized by the divergence angles of the output beam. Based on the device, we further realized a polarization-stable single mode VCSEL by introducing a built-in grating.

II. Device Design and Fabrication

The SiO_2/SiN_x dielectric films developed in this work are deposited by using ICP-CVD. The refractive index of the SiO_2 and SiN_x determined by ellipsometry is 1.46 and 2.01 respectively. The refractive index contrast between SiO_2 and SiN_x is much larger than the conventional semiconductor DBRs, so fewer pairs of dielectric films are required to reach the high reflectivity for lasing. Here, we fabricated SiO_2/SiN_x dielectric films on quartz substrates, and measured the reflectivity. The spectral reflectance measurement setup is shown in Fig. 1(a).The cross-sectional scanning electron microscope (SEM) image of the prepared SiO_2/SiN_x dielectric films is shown on the bottom right corner of Fig. 1(a), indicating the thickness of SiO_2 (155.2 nm) and SiN_x (114.1 nm). A light source of broad spectrum is coupled to the fiber, through a collimator, and onto the surface of the sample with normal incidence. The reflected light then travels back through the collimator and into the fiber, then goes to an Optical Spectrum Analyzer (OSA). The OSA measures the amount of reflected light at each wavelength to get the spectral reflectance. As shown in Fig. 1(b), the measured reflectivity attains 0.72, 0.9, 0.98 and 0.995 at 4, 7, 10 and 12 pairs of SiO_2/SiN_x respectively.

The schematic structure of the device is shown in Fig. 2(a). The VCSELs epitaxial structure are grown by metal-organic chemical vapor deposition (MOCVD) on n-GaAs substrate. The active region consists of three undoped $In_{0.0915}GaAs/Al_{0.3}GaAs$ quantum wells embedded in one-λ thick $Al_{0.3}Ga_{0.7}As$ separate confinement hetero-structure layer. A 30-nm thick $Al_{0.98}Ga_{0.02}As$ is grown above the active region to form oxide aperture for current and optical confinement. The bottom DBRs consist of 37.5 pairs of Si-doped $Al_{0.12}Ga_{0.88}As/Al_{0.9}Ga_{0.1}As$ with doping level of 2.5×10^{18} cm^{-3}. And 4 pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.9}Ga_{0.1}As$ top DBRs are kept for the sake of current injection and protection of the active region [4], followed by 50-nm highly C-doped (2×10^{19} cm^{-3})

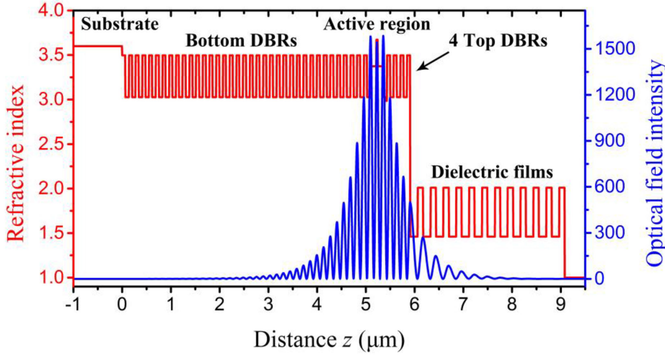

Fig. 3. The standing wave pattern and refractive index distribution of the VCSEL with SiO_2/SiN_x dielectric films.

TABLE I
LAYER THICKNESS AND REFRACTIVE INDEX OF THE SIMULATED DEVICES

Layer	Thickness (nm)	Refractive index
Dielectric films	153/111	1.46/2.01
4 Top DBRs	63.9/73.8	3.5/3.03
Oxide layer	30	2.99/1.65
One-λ cavity	116.1/30/116.1	3.37/3.67/3.37
Bottom DBRs	63.9/73.8	3.5/3.03
Substrate	5000	3.6

p-contact layer as well as the grating layer. In order to reduce the free-carrier absorption and the electrical series resistance, the first two top DBRs are C-doped at 2×10^{18} cm^{-3} for lightly doped regions, and the last two top DBRs have averaging doping level of 5×10^{18} cm^{-3}. And 20-nm grading layer with grading profile goes from $Al_{0.12}Ga_{0.88}As$ to $Al_{0.9}Ga_{0.1}As$ is inserted between $Al_{0.12}Ga_{0.88}As$ and $Al_{0.9}Ga_{0.1}As$. The dielectric film stacks are composed of 12 pairs of SiO_2/SiN_x. The fabrication processes of the devices are as follows. First, circular mesa is formed by $BCl_3/Ar/Cl_2$ inductively coupled plasma reaction ion etching (ICP-RIE) down to the active region with photoresist mask. Then $Al_{0.98}Ga_{0.02}As$ layer is selectively oxidized under 400°C to form the oxide aperture for transverse optical and current confinement. In situ near-infrared microscrope image of the oxide aperture is presented on the top right corner of Fig. 2(a) with aperture diameter of 3 μm for the mesa size of 48 μm. Afterwards, the ring-shaped P electrode (Ti/Au: 15/300 nm) is patterned by magnetron sputtering. The SiO_2/SiN_x dielectric films mesa, deposited by ICP-CVD at a temperature of 75°C, is easily formed with lift-off process. At last, the N electrode (AuGeNi/Au: 50/300 nm) is thermally evaporated. Fig. 2(b) presents the microscope images of the fabricated VCSELs under wafer-level testing.

To verify the design, an optical simulation for the field enhancement inside the structure is presented in Fig. 3. It was performed by using the commercial software FDTD Solutions based on finite-difference time domain method. The layer thickness and refractive index (referred to the single-effective oscillator model [15]) of the simulated structure are shown in Table I. As can be seen from Fig. 3, the optical field (blue line) is maximized across the active region positioned at an antinode of the standing wave in the vertical resonator, the high modal gain thus can be obtained through a resonant enhancement of the longitudinal optical confinement. Optical field confinement in the longitudinal direction is accomplished by the highly reflective semiconductor DBRs positioned below and SiO_2/SiN_x dielectric film stacks above the active region.

III. Results and Discussions

The Fig. 4(a) shows the measured light-current (L-I) curves of the fabricated device in the temperature range from 5°C to 45°C. The device has low threshold current of ∼0.3 mA. The maximum output power attains 1.6 mW at 5°C and reduces to 1.2 mW at 45°C. The reduction in output power is mainly due to the increased internal losses resulted from the elevated temperature. Fig. 4(b) plots the spectra of the same device under different bias currents from 1 mA to 5 mA, at 25°C under continuous wave operation. The device maintains single-mode operation throughout all bias currents. The side-mode suppression ratio (SMSR) exceeds 30 dB at the bias current of 5 mA. The lasing wavelength was red-shifted from 905.78 nm (1 mA) to 910.84 nm (5 mA). A wavelength-tuning coefficient of ∼1.26 nm/mA was measured.

In VCSELs, a temperature increase can be caused by an ambient temperature increase and, more importantly, by the internal heating of the active region. A high temperature in internal device will degrade the output performance and lifetime [16]–[18]. The thermal behavior of the VCSELs can be characterized by thermal resistance. According to the relationship of emission spectra and dissipated power, the thermal resistance R_{th} can be determined from $R_{th} = \Delta T/\Delta P_{diss} = (\Delta\lambda/\Delta P_{diss})/(\Delta\lambda/\ \Delta T)$ [18], [19]. $\Delta\lambda/\Delta P_{diss}$ is estimated by the fundamental mode peak emission wavelength shift rate versus the variation of the dissipated power, where the $P_{diss} = I\times V\text{-}P_{output}$. $\Delta\lambda/\Delta T$ is estimated by the fundamental mode peak emission wavelength shift rate versus the heat-sink temperature variation. The emission spectrum under different injection currents at ambient temperature from 5°C to 45°C is recorded using the OSA. To ensure no thermal wavelength shift appears, the fundamental mode peak emission wavelength without internal heating (at P_{diss} $= 0$ mW) is obtained by simple linear extrapolation. Fig. 5(a) plots the fundamental mode peak emission wavelength versus dissipated power. The rate $\Delta\lambda/\Delta P_{diss}$ increases with increasing ambient temperature. $\Delta\lambda/\Delta P_{diss}$ is 0.253±0.008, 0.256±0.006, 0.258±0.007, 0.265±0.005, 0.269±0.005 nm/mW at the temperature of 5°C, 15°C, 25°C, 35°C, and 45°C, respectively. Fig. 5(b) shows the extracted peak emission wavelength shifting with varied ambient temperature. We can easily see that the wavelength shifts with ambient temperature linearly with a slope of 0.062 nm/°C, as shown in Fig. 5(b). Thus, the thermal resistance depending on the ambient temperature can be derived. The calculated values of R_{th} under different ambient temperature are plotted in Fig. 6, which is comparable to the counterpart of

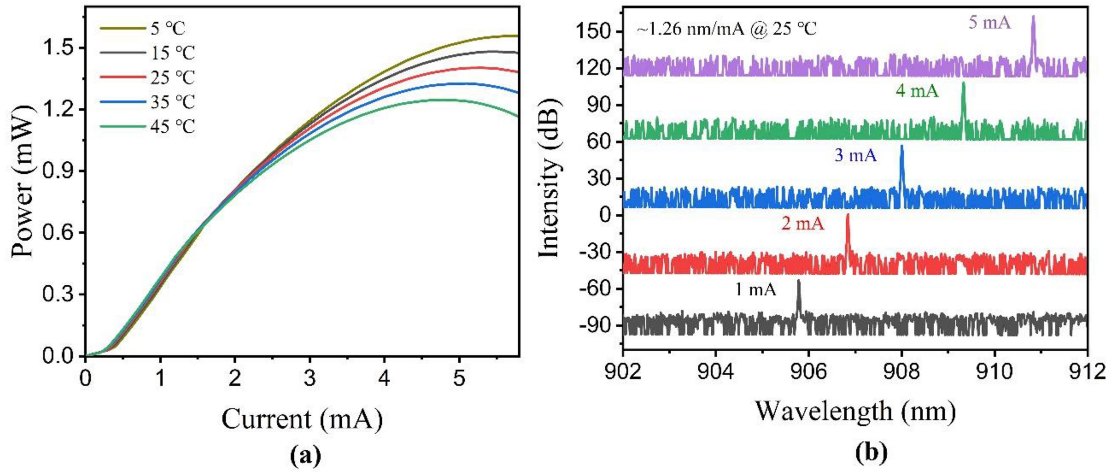

Fig. 4. (a) L-I curves of the device in the temperature range from 5°C to 45°C. (b) Spectra of the device taken at bias current of 1 mA, 2 mA, 3 mA, 4 mA and 5 mA respectively at the temperature of 25°C.

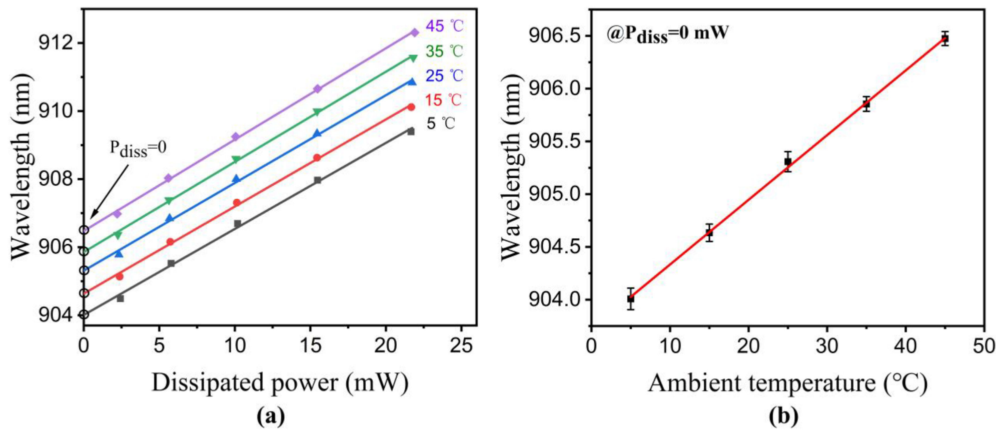

Fig. 5. (a) The fundamental mode peak emission wavelength versus dissipated power under different ambient temperatures. (b) The extracted fundamental mode peak emission wavelength without internal heating (at $P_{diss} = 0$ mW) under different ambient temperatures with a slope of 0.062 nm/°C.

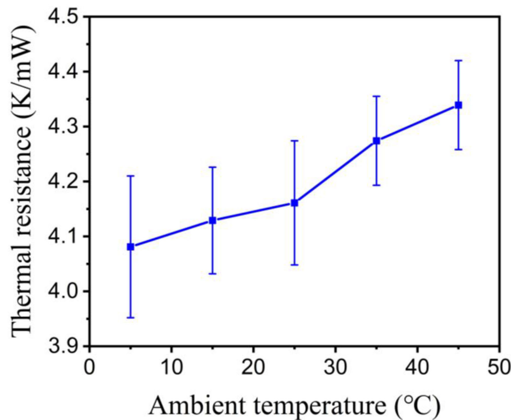

Fig. 6. Thermal resistance R_{th} under different ambient temperature.

the GaAs-based VCSELs [18], [20]. The thermal resistances increase with increasing ambient temperature.

According to the ambient-temperature-dependent thermal resistance, the actual temperature in active region can be calculated from $T_{active} = T_{ambient}+R_{th}\times P_{diss}$ [18], [20]. Fig. 7(a) plots the output power curve and active region temperature of the device versus injection current at ambient temperature of 25°C. The active region temperature attains 116°C at the injection current of 5 mA. Fig. 7(b) presents the colormap of the active region temperatures versus both injection current and ambient temperature, where we can see that the active region temperature increases with both injection current and ambient temperature. The active region temperature attains 135°C at the saturation current of 4.8 mA for the ambient temperature of 45°C.

To characterize the beam property of the device, the far field patterns (FFPs) are measured at room temperature under continuous wave operation. The measured FFP in Fig. 8(a) shows a single lobe exhibiting Gaussian-like profile. The divergence angles of the output beam estimated from the full-width-half-maximum (FWHM) of the FFP are shown in Fig. 8(b) and (c). The FFPs had a divergence angle of 21.4° and 20.3° in the x (Fig. 8(b)) and y (Fig. 8(c)) directions respectively for the drive current of 5 mA. The average divergence angles are between 20.4° and 21.2° depending on the drive current.

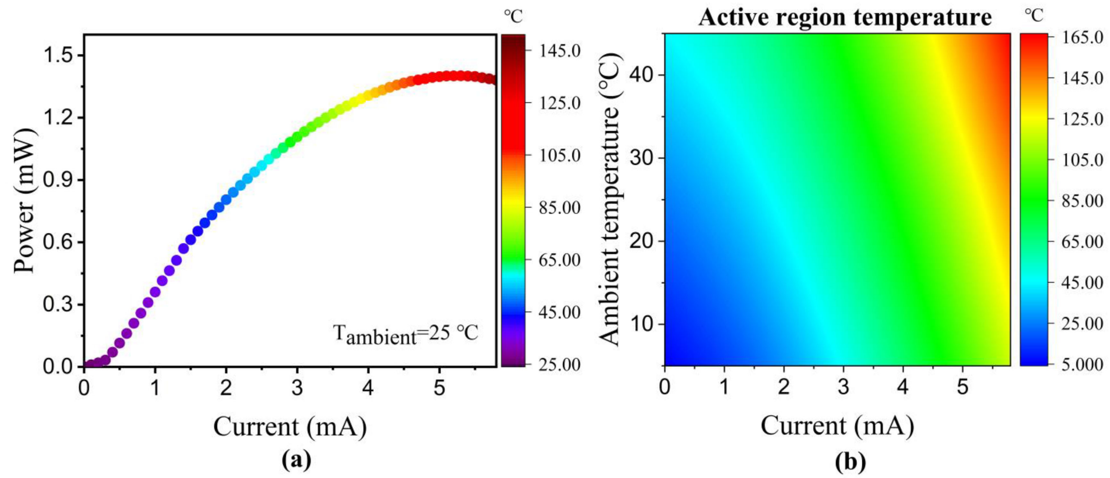

Fig. 7. (a) Power curves of the device with color coding of active region temperature at the ambient temperature of 25°C. (b) Colormap of the active region temperatures versus both injection current and ambient temperature.

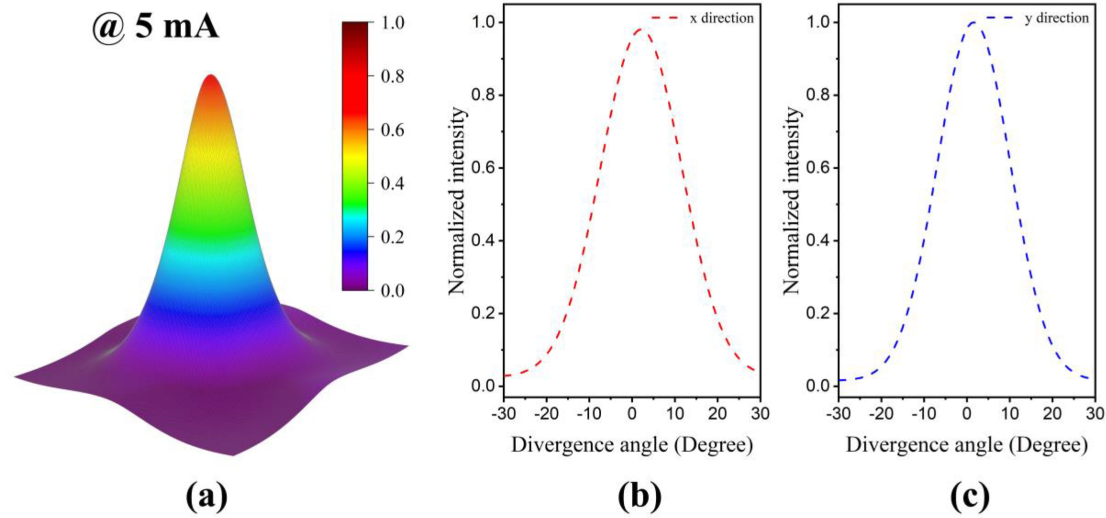

Fig. 8. (a) The FFP of the device at the current 5 mA. (b) and (c) are the measured divergence angles of the device in the x and y directions respectively for the drive current of 5 mA.

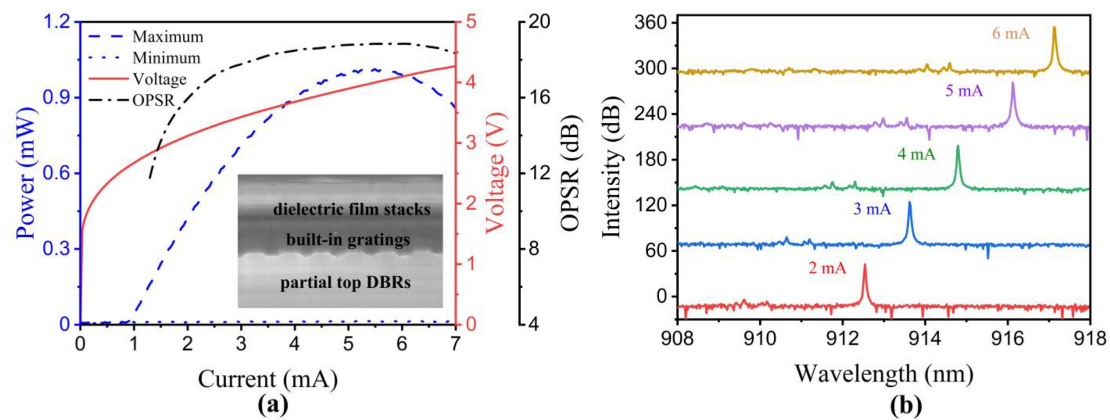

Fig. 9. (a) Polarization-resolved operation characteristics of the VCSEL with built-in gratings. The inset shows the cross-sectional SEM image of the device. (b) Spectra of the device taken at bias current of 2 mA, 3 mA, 4 mA, 5 mA and 6 mA respectively at the temperature of 25°C.

Single-mode VCSELs have been widely employed in data center research [21], [22]. However, for many applications, the VCSELs are required not only to be single-mode, but also to be polarization-stable for high system performance [23], [24]. Unfortunately, VCSELs inherently have an unstable and hardly predictable polarization due to cylindrical symmetry and isotropic gain. This increases the relative intensity noise of VCSELs and limits their use in polarization-sensitive applications [23], [24]. Typical methods used to control the polarization of VCSELs include introducing a polarization-dependent gain by an oriented substrate [25], an asymmetric resonator [26], or introducing polarization-dependent mirror loss by surface grating [27], [28]. As for the dielectric DBRs VCSEL, the surface grating is difficult to prepare due to the poor conductivity of dielectric films. Here we introduce built-in gratings into the device to control the polarization state. The gratings with period of 300 nm, duty cycle of 0.6, and an etch depth of 50 nm, are fabricated by focused ion beam before depositing dielectric films. Mass-production can be written using e-beam lithography and etched using ICP-RIE. Fig. 9(a) presents the polarization-resolved operation characteristics of the VCSEL with built-in gratings, where we can see that the device exhibits a strong polarization control. This can be attributed to the polarization-dependent mirror loss introduced by the built-in gratings. The magnitude of the OPSR defined by $10\log(P_{max}/P_{min})$ is around 19 dB. The optical powers P_{max} and P_{min} are measured behind a polarizer, whose transmission direction is oriented orthogonal and parallel to the grating strips, respectively. The inset in Fig. 9(a) shows the cross-sectional SEM image of the device, indicating the built-in gratings. Fig. 9(b) plots the spectra of the device under different bias currents from 2 mA to 6 mA, at 25°C under continuous wave operation. The device maintains single-mode operation throughout all bias currents with SMSR exceeds 40 dB.

IV. Conclusion

In summary, we prepared SiO_2/SiN_x dielectric films as DBR mirror. With such highly reflective dielectric film stacks, we developed a low threshold single fundamental mode VCSEL. The device has a threshold current of 0.3 mA, peak single fundamental mode power of 1.4 mW. The thermal properties are analyzed by estimating the thermal resistance of the device according to the relationship of wavelength shift and dissipated power, which is comparable to the counterpart of the GaAs-based VCSELs. Furthermore, we demonstrate the polarization control of the device by introducing built-in gratings. By modifying the semiconductor DBRs mesa, lithographically defined pattern can be integrated to the device.

References

[1] A. Larsson, "Advances in VCSELs for communication and sensing," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 6, pp. 1552–1567, Nov./Dec. 2011.

[2] A. Liu *et al.*, "Vertical-cavity surface-emitting lasers for data communication and sensing," *Photon. Res.*, vol. 7, no. 02, pp. 24–39, Feb. 2019.

[3] P. Westbergh, J. S. Gustavsson, Å. Haglund, M. Skold, A. Joel, and A. Larsson, "High-speed, low-current-density 850 nm VCSELs," *IEEE J. Sel. Topics Quantum Electron.*, vol. 15, no. 3, pp. 694–703, May/Jun. 2009.

[4] M. C. Y. Huang *et al.*, "A surface-emitting laser incorporating a high-index-contrast subwavelength grating," *Nature. Photon.*, vol. 1, no. 2, pp. 119–122, Feb. 2007.

[5] I. Kenichi, "Forty years of vertical-cavity surface-emitting laser: Invention and innovation," *J. Appl. Phys.*, vol. 57, no. 8S2, Jul. 2018, Art. no. 08PA01.

[6] G. Kedawat *et al.*, "Fabrication of artificially stacked ultrathin ZnS/MgF_2 multilayer dielectric optical filters," *ACS Appl. Mater. Interfaces*, vol. 5, no. 11, pp. 4872–4877, May 2013.

[7] T. Maier, G. Strasser, and E. Gornik„ "Monolithic integration of vertical-cavity laser diodes and resonant photodetectors with hybrid Si_3N_4-SiO_2 top Bragg mirrors," *IEEE Photon. Technol. Lett.*, vol. 12, no. 2, pp. 119–121, Feb. 2000.

[8] C. Levallois *et al.*, "Design and fabrication of GaInAsP-InP VCSEL with two a-Si/a-SiN_x Bragg reflectors," in *Proc. Int. Workshop Phys. Appl. Semicond. LASERS*, Mar 2005, Art. no. hal-00491400.

[9] M. V. Ramana Murty *et al.*, "An 850 nm dielectric guide VCSEL for data communication links," in *Proc. IEEE Photon. Soc. Summer Topicals*, Playa del Carmen, Mexico, 2010, pp. 213–214.

[10] T. H. Oh and O. B. Shchekin, "Single-mode operation in an antiguided vertical-cavity surface-emitting laser using a low-temperature grown algaas dielectric aperture," *IEEE Photon. Technol. Lett.*, vol. 10, no. 8, pp. 1064–1066, Aug. 1998.

[11] C. Lei *et al.*, "$ZnSe/CaF_2$ quarter-wave Bragg reflector for the vertical-cavity surface-emitting laser," *J. Appl. Phys.*, vol. 69, no. 11, pp. 7430–7434, Feb. 1991.

[12] A. Palatnik *et al.*, "Fabrication of dielectric Bragg reflectors composed of CaF_2 and ZnS for delicate lasing materials," in *Proc. CLEO: OSA Tech. Dig. Opt. Soc. Amer.*, 2015, Art. no. AM3K.8.

[13] D. Sun *et al.*, "Sub-mA threshold 1.5-μm VCSELs with epitaxial and dielectric DBR mirrors," *IEEE Photon. Technol. Lett.*, vol. 15, no. 12, pp. 1677–1679, Dec. 2003.

[14] P. Wei *et al.*, "Surface passivation of In0.83Ga0.17As photodiode with high-quality SiN layer fabricated by ICPCVD at the lower temperature," *Infrared Phys. Technol.*, vol. 62, pp. 13–17, Oct. 2014.

[15] A. Afromowitz Martin, "Refractive index of Ga1-xAlxAs," *Solid State Commun.*, vol. 15, no. 1, pp. 59–63, Jul. 1974.

[16] M. Xun *et al.*, "Analysis of thermal properties of 940-nm vertical cavity surface emitting laser arrays," *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 158–163, Jan. 2021.

[17] J. H. Wang *et al.*, "Thermal analysis of oxide confined VCSEL arrays," *Microelectron. J.*, vol. 42, no. 5, pp. 820–825, May 2011.

[18] H. Li, P. Wolf, X. Jia, J. A. Lott, and D. Bimberg, "Thermal analysis of high-bandwidth and energy-efficient 980 nm VCSELs with optimized quantum well gain peak-to-cavity resonance wavelength offset," *Appl. Phys. Lett.*, vol. 111, no. 24, Dec. 2017, Art. no. 243508.

[19] T. Flick *et al.*, "Measurement of the thermal resistance of VCSEL devices," *J. Instrum.*, vol. 6, no. 1, Sep. 2011, Art. no. C01021.

[20] R. Michalzik, *VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers*, Berlin, Germany: Springer-Verlag, 2013.

[21] C. Y. Peng, J. Qiu, T.-Y. Huang, C.-H. Wu, M. Feng, and C.-H. Wu, "850 nm single-mode vertical-cavity surface-emitting lasers for 40 Gb/s error-free transmission up to 500 m in OM4 fiber," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 99, Jan. 2020.

[22] K. Hsuan-Yun *et al.*, "Single-mode VCSEL for pre-emphasis PAM-4 transmission up to 64Gbit/s over 100–300m in OM4 MMF," *Photon. Res.*, vol. 6, no. 7, p. 666, Jul. 2018.

[23] A. Al-Samaneh *et al.*, "Polarization-stable vertical-cavity surface-emitting lasers with inverted grating relief for use in microscale atomic clocks," *Appl. Phys. Lett.*, vol. 101, pp. 640–649, Oct. 2012.

[24] J. M. Ostermann, F. Rinaldi, P. Debernardi, R. Michalzik, "VCSELs with enhanced single-mode power and stabilized polarization for oxygen sensing," *IEEE Photon. Technol. Lett.*, vol. 17, no. 11, pp. 2256–2258, Nov. 2005.

[25] G. Verschaffelt *et al.*, "Polarization stabilization in vertical-cavity surface-emitting lasers through asymmetric current injection," *IEEE Photon. Technol. Lett.*, vol. 12, no. 8, pp. 945–947, Aug. 2000.

[26] S. Riyopoulos and E. Nhan, "Polarization selection due to scattering losses in nonaxisymmetric vertical cavity surface emitting laser cavities," *Appl. Phys. Lett.*, vol. 85, pp. 3038–3040, Oct. 2004.

[27] J. M. Ostermann, P. Debernardi, and R. Michalzik, "Surface grating VCSELs with dynamically stable light output polarization," *IEEE Photon. Technol. Lett.*, vol. 17, no. 12, pp. 2505–2507, Dec. 2005.

[28] E. Haglund *et al.*, "High-power single transverse and polarization mode VCSEL for silicon photonics integration." *Opt. Exp.*, vol. 27, no. 13 Jun. 2019, Art. no. 18892.