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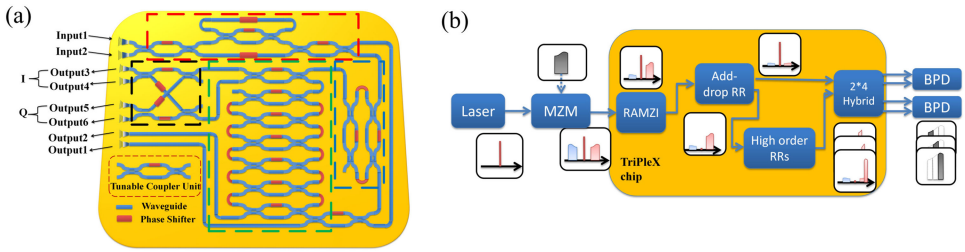

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Programmable RF Receiver Related On-Chip Photonic Processor

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Abstract: This study reports and experimentally demonstrates a programmable on-chip photonic processor towards different RF receiver configurations. The Si_3N_4 processor is built by interconnecting independent subunits such as simple and complex Mach-Zehnder interferometers and Ring resonators. The design, fabrication, and characterization of a dedicated chip are described. As a proof of concept, it can be used as a reconfigurable filter with distinct frequency response. More importantly, a thorough RF receiver related passive processor including out-of-band suppression, carrier-sideband routing, channelization filtering, as well as I-Q mixing prior to an optical detection stage. This is effective proof of a programmable integrated processor encompassing most passive filtering and routing subunits for broadband photonic RF receiver.

Index Terms: Programmable, Si_3N_4 nanoprocessor, reconfigurable filter, Mach-Zehnder interferometers, ring resonators.

1. Introduction

Being an important branch of the RF industry, Radio Frequency Integrated Circuits (RFICs) for filters are making continuous progress in optimizing the performance as well as subdividing the functionalities. Especially the evolutions of RF filter circuits have become a weather vane that might determine the system performance. However, filter circuits face a crucial challenge at the current trend of high throughput market expansion – their sizeable dimensions are not compatible [1], [2]. Less selectivity and tunability at high frequencies as well as massive uncertainty during design and fabrication prevent further miniaturization of the filters for cost-effective, high-speed applications. The bulky nature of passive RF components prevents further miniaturization of the RF chips for

cost-effective, high-speed applications. Off-chip components could partially solve this limitation, but at the cost of a reduced level of integration and an additional parasitic caused by packaging.

One way to address this is to consider their implementation using an integrated photonics approach, whereby a photonic integrated circuit (PIC) is employed to provide a flexible implementation and filters with the added bonus of reconfigurability and potential multi-task operation [3]–[6]. It brings advantages related to low-loss transportation, broadband operation enabling capability for multi-octave receivers, and the flexibility of reconfigurable RF response. Work reported so far on PIC filtering can be summarized into three categories.

The first and most extensive type is based on Mach-Zehnder interferometers (MZI), which includes designs based on cascaded MZIs [7], [8], ring resonator-assisted MZI (RAMZI) [9]–[12], and MZIs combined with other tunable components [13], [14] and so on. Notably, RAMZI contains fundamentally ring resonators embedded in a Mach-Zehnder interferometer. They can appear in the interferometer structure in different numbers and positions to fulfill diverse functionalities. The design of FSR of ring resonators is always related to that of MZI, and ring resonators are acted as optimization components to improve the shape characteristics of the interferometer structure filter. So we prefer to classify RAMZI with the MZI category rather than ring resonators or others. Narrowband silicon on-chip filters are formed, for example, by three-stage and four-stage cascaded MZIs which are feature fast-reconfigurable filters with bandwidths down to 400MHz and tunable center wavelength over 10GHz through full control over single-unit cells, respectively [7], [8]. The mature fabrication technology enriches the variation of MZI filters in all kinds of platforms. Classic schemes for RAMZI [9] were used to demonstrate a monolithically integrated filter for the first time, with all main active and passive components into an indium phosphide chip. It allowed a flat-top passband response tuned from 2.5 to 5.5GHz. Other topologies like combining MZI and semiconductor optical amplifiers (SOAs) [13] and Sagnac loops [14] can also be employed to implement reconfigurable filters.

The second type of RF-photonic integrated filter is based on the use of ring resonators (RRs) as an essential building block. Compared to MZIs, RRs show increased wavelength sensitivity, which leads to a higher resolution as an RF filter. RR based PIC filters have been reported showing flat-top narrowband and excellent extinction ratio (out of band signal rejection) characteristics [15]–[21]. An on-chip RF photonic filter based on four cascaded RRs [20] exhibits a representative flat top filter with bandwidth tuning from 300 MHz to 25 GHz. The frequency response is fully programmable, and at the same time, the configurability is phase and amplitude sensitive.

The third option for implementing PIC RF filters uses on-chip stimulated Brillouin scattering (SBS) [22]–[27]. They have enabled MHz range highly selective RF notch filters [24] and high-resolution characteristics by using high nonlinearity waveguides [25]–[27]; it remains the requirement to assemble all the necessary components towards chip-level hybrid or monolithic integration.

An overview of representative on-chip filters in the past decade is listed in Table 1. From a practical perspective, most of the achievements are aimed at improving the performance of single-function filtering. Very little work involves integrating a series but reconfigurable components into a specific application. For Photonics RF receivers including broadband communication and high-throughput satellite communication, a set of filtering processes with different functions are required between RF modulation and optical detection, such as sideband or carrier selection, noise suppression, channel division, phase control, and so on. As shown above, most of the current on-chip filters are optimized for a specific filtering function, prepared based on different materials and interfaces, and do not have integrated back-end processing capabilities. Here we report and demonstrate a general multitask processor built by interconnecting independent on-chip subunits such as simple and complex Mach-Zehnder and Ring resonator filters on Si_3N_4 waveguide platform [32]. Each subunit is independently adjustable by proper programming of their internal basic constituent units formed by tunable couplers and phase actuators. According to the integrated programmable principle [28], this chip can be used as a reconfigurable filter with distinct frequency response. More importantly, a combination of all on-chip subunits allows a thorough RF receiver capability encompassing out-of-band suppression, carrier- sideband routing, narrow channelization, as well as thermo- optic I-Q mixing, and so on. The proof-of-concept result expects

TABLE 1
Overview of Representative on-Chip Filters in the Past Decade

Structure	Material	3dB BW (GHz)	Flat top	FSR (GHz)	NTE	Application	Year	Ref
5th RRs	SOI	1-2	Y	50	5	Signal processors	2010	[15]
Cascaded MZI	SOI	1.563	N	13.5	3	Down conversion	2013	[7]
Spiral Cavity RRs	SOI	2.625	N	25	N.A.	Optical comb filters	2010	[20]
RAMZI	SOI	23-173	N	100-200	5	WDM systems	2014	[11]
Cascaded MZI	SOI	>0.4	Y	10	26	Optical lattice filters	2011	[8]
RAMZI	InGaAsP/InP	2.5-5.5	Y	20	6	Signal processing	2016	[9]
RRs+SOA	InGaAsP/InP	3.9-7.1	Y	26.5	21	N.A.	2011	[21]
RAMZI+SOA	InGaAsP/InP	1.9-5.4	Y	23.5-47	29	N.A.	2011	[13]
8th RRs	Si_3N_4	0.072	Y	1.4	17	reconfigurable IMUX	2014	[16]
RAMZI+ Sagnac loop	Si_3N_4	0.6	N	12.5	5	clock multiplication	2018	[14]
N-SCISSOR	Si_3N_4	1.2-2.5	Y	12.5	6	Signal processors	2016	[19]
PPER	SOI	0.005	N	N.A.	2	low-distortion signal processing	2018	[22]
RRs array	SOI	40	Y	1000	4	Reconfigurable Add–Drop	2019	[17]
SBS +RRs	Si_3N_4	0.26	N	N.A.	3	Positive gain photonic link	2019	[23]
SBS on chip	SOI	0.033–0.088	N	30	7	Signal processors	2015	[24]
SBS on chip	As_2S_3	0.03-0.44	Y	30	N.A.	On-chip microwave filters	2016	[26]
RAMZI +RRs +HC	Si_3N_4	**0.39-8.6**	**Y**	**19/13**	**23**	**Reconfigurable Signal processors**	**2020**	**This work**

the chip's ability to complete the most passive processing of photonics RF receiver in the optical domain, shows potential compact advantage for Photonics RF receiver.

2. Principles

2.1 Processor Design and Layout

For a photonic integrated programmable processor, a reconfigurable programmable core is subject to the action of different input optical and electrical signals and is controlled by an electronic board. The processor's critical element is the optical core composed of several interconnected and independent tunable signal processing subunits. Each subunit comprises several tunable basic units (TBUs) and fixed photonic waveguides [28], [30], and [31].

Fig. 1a shows the TBU level layout of the proposed photonic chip. The TBU comprises two internal 3dB directional couplers and one or two thermo-optic phase shifters, as shown in the bottom left inset of Fig. 1a. The circuit contains 16 basic TBUs that are structured in four different programmable subparts: 4 units placed in the upper form an RAMZI structure. The second subpart is an add-drop RR implemented by 3 TBUs placed at the right. The third subpart is a cascaded RR N^{th}–order filter ($1 \leq N \leq 5$) implemented by 7 TBUs placed in the center. And finally, the fourth subpart is a photonic hybrid coupler (HC) implemented by means of 2 TBUs.

The purpose of including four diverse structures inside this chip is to integrate most of the passive processing required for on-chip RF reception, as shown in Fig. 1b. The functions of each subpart are expressed as follows. RAMZI is used as a single-sideband filter to reduce out-of-band distortions. Add-drop RR is able to separate the carrier and the RF sideband. Cascaded RR N^{th}–order filter can select several narrowband channels from the wideband RF signal. Last, a hybrid coupler is used to combine optical carrier from Add-drop RR and the selected RF channel

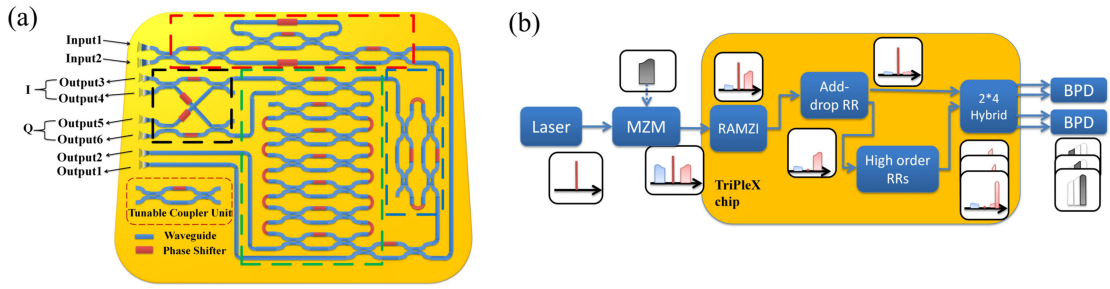

Fig. 1. Layout diagram of the photonic chip: (a) TBU level layout description, (b) System-level description.

from Cascaded RRs with reconfigurable phase relationship towards different kinds of the receiver like BPD (Balanced Photodetector) / coherent receiver/ I-Q receiver, and so on.

As shown in Fig. 1a, there are 2 input ports and 6 parallel output ports. The two input ports are directly connected to the left-side TBU in RAMZI subpart. Inside the asymmetric interferometer, a ring resonator with a thermo-optic phase shifter inside is located in the upper branch and allows a roundtrip length of ΔL - twice the length difference of two branches of the RAMZI structure. As a critical part of the filter selectivity, each coupling coefficient and inner phase difference of the RAMZI structure can be tuned individually, resulting in a GHz band flat-top frequency response, which can be detected by edge coupling through the output1 port. Following the RAMZI, an add-drop RR is connected to the lower port of its right-hand-side exit TBU, and the combined output of these two units can be accessed, if required, by the convenient connection of the RR through port to the output2 port. The RR drop port leads instead to the connection with ensuing subparts. The RR roundtrip length equals ΔL/2, providing the same free spectral range (FSR) as that of the RAMZI unit.

Concerning the third subunit implementing the high-order cascade RR filter, the configuration of the internal TBUs allows the implementation of cascaded N^{th}–order RRs where $1 \leq N \leq 5$, where higher-order structure results in higher selectivity of the frequency response. For example, with $N = 5$ and suitable programming of the phase shifters leading to symmetric filter coefficients, flat-top passband responses with bandwidth lower than 500MHz can be achieved.

For cascaded ring resonators filter, different ring number means diverse frequency response. Naturally, the more rings in a filter, the much narrower passband bandwidth the filter can obtain [7], [16, and [18]. However, not only the filter orders determine the 3dB bandwidth, but different coupling coefficients (Kappa) could also result in different bandwidth and full-range frequency response. As shown in Fig. 2a and Fig. 2b, when 4th or 5th order RRs are prepared in this chip, diverse frequency responses of the passband filter are achieved by optimizing different coupling coefficients. From the two numerical results above, we can see that no matter the order of ring resonators, a reconfigurable range of 3dB bandwidth could always be reached. What matters is the shape factor (rectangular coefficient) of the entire passband as shown by the intersection of the different curves at the bottom of the above two figures on the horizontal axis. General, the more rings in the filter, the better the shape factor can be when building a narrower bandwidth frequency response. According to the development of cost-effective ADC performance, 300-500MHz is an acceptable analog bandwidth for signal digitalization in a RF receiver. Therefore, in this scheme, we tend to design a cascaded Nth–order RRs subpart, which includes a reconfigurable passband filtering function with the minimum bandwidth of about 300MHz-500MHz, and an order of ring resonators up to 5.

The last subsystem is a 2$*$4 photonic HC, which includes two TBUs and a taper cross waveguide with heaters inside. Output signals of HC coming from signals combination from either the add-drop RR or the high-order RRs. According to the reception mode required by the RF receiver system, this

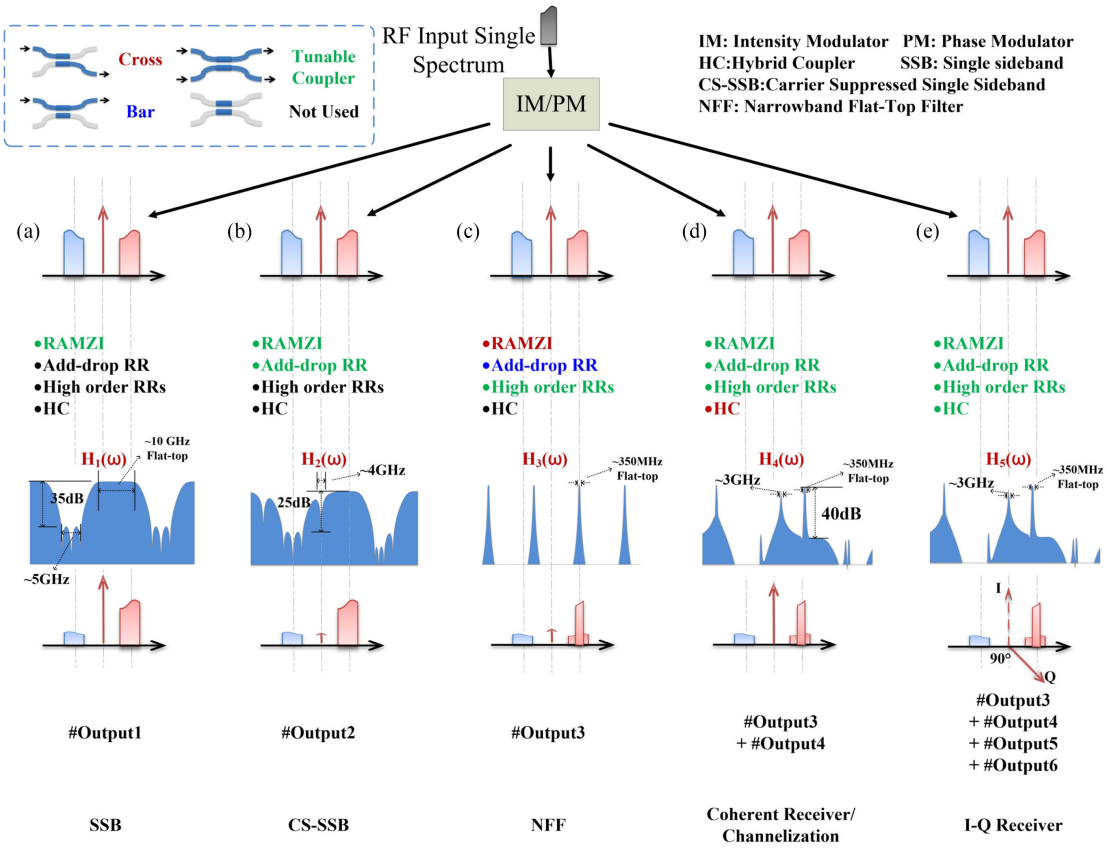

Fig. 2. Illustration of simulated spectrum for different processor configurations: (a) Sigle sideband filter with flat-top passband width of 10GHz while stopband width ranging among 1.5GHz-7GHz, (b) CS-SSB with carrier stopband range of 2GHz-6GHz, (c) NFF with narrow flat-top passband range of 300MHz-600MHz, (d) Coherent Receiver /Channelization, (e) I-Q receiver for Image-Reject Processor.

part is designed to provide as normal couplers or I-Q couplers by configuring the phase indifference between carrier and sideband signals. Therefore, four ports (output 3 to output 6) provide the output signal that can be coupled to PD (photodetectors), BPDs (balanced photodetectors), or I-Q receivers, respectively.

2.2 Multifunctional Operation Description

It should be noted that, since each TBU can be independently programmed to operate as a directional coupler or an optical switch in a cross or bar state providing phase-controlled optical routing, the overall circuit can implement a considerable number of functionalities beyond the RF receiver. Using this principle, the proposed architecture can be reconfigured to support different kinds of linear transformations between multiple input/output waveguides implementing a reconfigurable photonic processor.

Figure Fig. 2 illustrates, as an example, typical processing functionalities that can be implemented by suitable programming. In each case, we indicate whether a given subpart is in active mode (i.e., at least one of its internal TBUs is programmed as a tunable coupler), or in routing mode (its internal TBUs are programmed as cross or bar switches) or inactive. We also indicate the output ports to where the processed signals are routed, and the working states of the four processing subunits are also shown. For instance, Fig. 2a and Fig. 2b correspond to implementing

an independent or RF receiver related high-frequency (around 5-7 GHz) broadband Flat-Top filter that can be applied, for example, for single-sideband $H_1(\omega)$ (SSB) and CS-SSB $H_2(\omega)$ (Carrier Suppression SSB) filter, respectively. Note that when activating independently, the output signals are directed to output 1 and output 2, respectively, while the high-order RRs and HC subunits are not used. Otherwise, they are routed to the following add-drop RR for more complex functions. Fig. 2c illustrates the configuration leading to the implementation of a narrowband flat-top filter (NFF) $H_3(\omega)$ or a channelization filter. Here the RAMZI subunit is programmed to be in routing mode (cross-state), as well as the add-drop RR subunit (Bar state), while the high-order RRs subunit is programmed to be in an active state, and the HC subunit is unused. In this case, periodic of flat-top passband featuring a spectral down to 350 MHz (N $=$ 5) are achieved through output 3.

Fig. 2d and Fig. 2e illustrate two cases involving more complex signal processing functionalities towards RF reception mode kinds. The case shown in Fig. 2d ($H_4(\omega)$) corresponds to a set-up where the RAMZI, add-drop RR, and the high-order RRs subunits are actively programmed. The HC unit merely combines the output signals from two internal drop ports, resulting in mixed frequency response with one Lorentz sharp passband selects a single optical carrier, while another selects channels from a broadband frequency range. The RAMZI unit is programmed to operate as a GHz-band flat-top filter to suppress the lower sideband. The add-drop RR subunit is programmed to operate as a demultiplexer to separate the carrier and upper sideband, routing them to different spatial paths, so only a sideband signal is processed cascaded RRs subunit. The key asset that is exploited here from this subunit is its ability to provide a rectangular shape, flat-top passband, and high isolation to avoid interference channels. The configurable capacity here supports a passband width of several hundreds of MHz and a tunable center wavelength over one FSR, which could be beneficial to extract other channels in a broadband signal.

The processor's overall operation thus corresponds to a coherent receiver channelizer. A coherent receiver receives an orthogonally multiplexed signal in which the first (received) signal and second (local oscillator) signal have been orthogonally multiplexed before injecting into a photodetector. In this reconfigurable filter, as shown in Fig. 2d, coherent receiver mode could be achieved when the Hybrid Coupler (HC) works as a 2$*$1 coupler following a photodetector. Moreover, BPDs are always introduced into coherent receivers to increase the effective utilization rate of light and cancel out a large part of the noise. In this reconfigurable filter, as shown in Fig. 2e, BPD coherent receiver mode could be achieved when the Hybrid Coupler (HC) works as a 2$*$2 coupler following with a pair of photodetectors.

Furthermore, this operation can be extended to embrace as well that of an I-Q coherent receiver when two outputs are used together for heterodyning. IQ receiver is one of the most effective receive modes to reject image frequency. It can be treated as a pair of BPD coherent receivers where the HC works as a 2$*$4 coupler, following by two BPDs for orthogonal I branch and Q branch processing. This can be achieved, as shown in Fig. 2e ($H_5(\omega)$), by changing the HC subunit operation state from a normal combiner to a 2$*$4 90° hybrid coupler. It provides high image rejection and high in-band interference suppression for signal processing applications. The fundamental principle of photonic image rejection and the subsequent electrical signal processing can be found in references [34]–[35]. The chip is not limited to these functionalities but has only listed those for which we report experimental results in the next section.

3. Results and Discussion

3.1 Chip Die Description, Fabrication, and Packaging

This chip's mask layout was designed by using Product Development tool Kits (PDKs) from Synopsys and fabricated via TriPlex platform from LioniX BV. Thanks to the Symmetric Double-Stripe (SDS) Si_3N_4 waveguide technology [37] low-loss propagation ($<$0.1 dB/cm) can be achieved. A microphotograph, together with the relative mask layout of the chip, is shown in Fig. 3. The RAMZI, add-drop RR, as well as high-order RRs and HC, are integrated into a chip size of 8$*$16 mm^2 corresponding to Fig. 3a. Two different bend radii are employed in mask layout: the lower one that

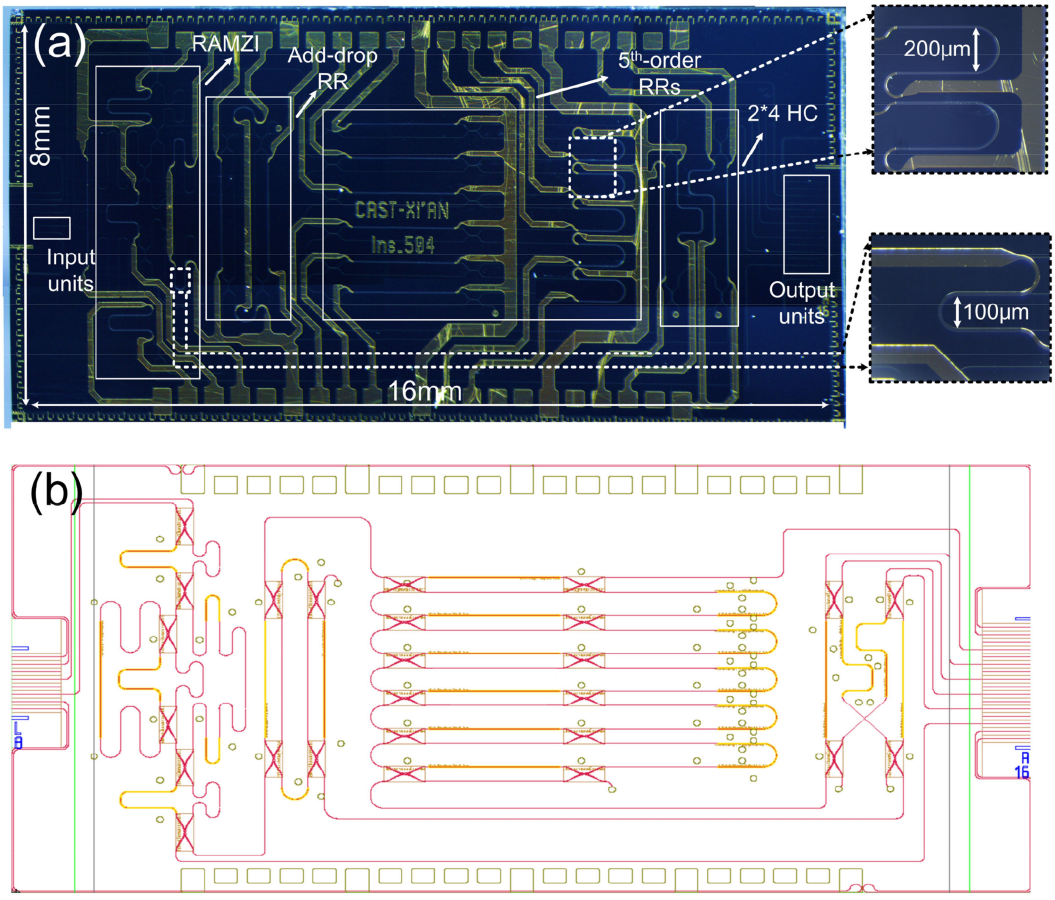

Fig. 3. Fabricated die. (a) Microphotograph of a fabricated die ($8*16mm^2$), (b) Mask layout design.

down to 100 μm is employed for components interconnection inside the subparts, which would reduce the footprint of the whole chip; the higher one with the value of 200 μm is used for parallel or bent heaters to prevent thermal crosstalk in dense areas such as the cascaded RRs and HC as shown in the insets of Fig. 3a.

The specification of the mask layout shown in Fig. 3b is described below. The longest circumference of RAMZI inter-arm delay difference and the inter ring resonator are designed to be 8.92 mm and 17.84 mm, respectively, resulting in an FSR of 19GHz. The length of each heater is equal to 2100 μm, to guarantee 2π phase shift ability for each phase actuator. The longest roundtrip length of the add-drop RR is designed to be 8.92 mm, resulting in the same FSR with RAMZI. The high-order cascaded RRs feature FSR of 13GHz, which corresponds to a round trip length of 13.04 mm for each ring. 11 heaters are incorporated into this structure for reconfigurable programming of its transfer function. The HC consists of a taper cross structure and two basic tunable units inside. To mitigate thermal crosstalk, the spaces between adjacent heaters as well as that between the heater and normal waveguides are kept to a value above 250 μm.

To simplify and stabilize the measurement processing, the chip is packaged and wire-bonded, as shown in Fig. 4a. In the packaging process, a printed circuit board (PCB) is placed next to the chip to which the bond pads' electrical connections are made. Figure 4b shows the size of the photonic chip as compared to a 1 € coin. A heatsink is designed and realized on top of which the chip is fixed. Figure 4c illustrates the microphotograph of the wire bonding details between DC pads and PCB. Input and output facets are edged coupled and aligned to single-mode polarization-maintaining

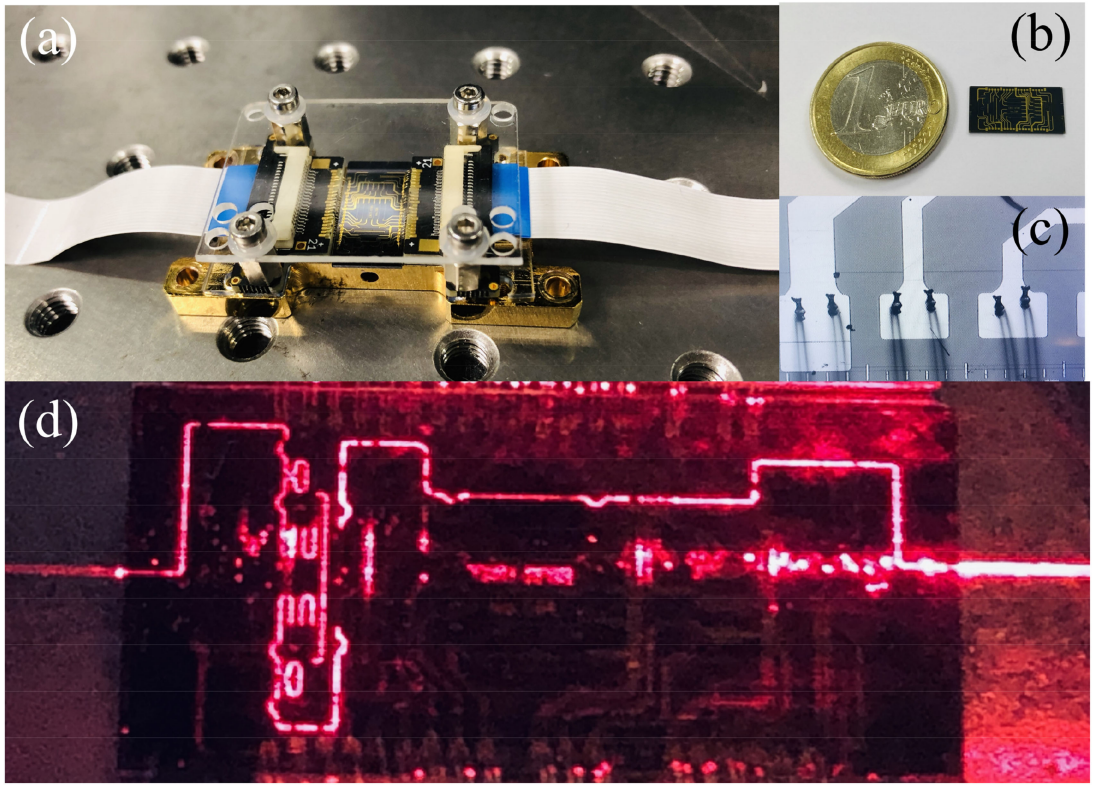

Fig. 4. Package specification: (a) Assembled structure with 42 wire bonding along two facets, (b) Die footprint compared to a 1€ coin, (c) Microphotograph of wire bonding, (d) Image of propagation path when coupled to a 637 nm red diode laser from input 1 to output 2.

fibers during measurement. Figure 4d finally illustrates a propagation path within the chip when coupled to a 637 nm red diode laser from input 1 to output 2.

3.2 Experiment and Discussion

To verify the performance of the processor, a proof-of-concept experiment based on the programming configurations described in section 2 is performed following the experimental set-up shown in Fig. 5a. A broadband modulator driven by a continuous-wave tunable laser and a vector-network-analyzer (VNA) provides the input signal to the photonic chip. All the output ports are edge coupled to an optical spectrum analyzer (OSA Yokogawa and BOSA) for measurement. TBUs inside the subunits of the chip are precisely, simultaneously, and independently programmed by means of multichannel DC current sources.

The overall chip insertion loss from input 1 to output 1 is around 6dB when connectorized polarization-maintaining fibers are used for edge coupling. Fig. 5b shows the frequency response corresponding to TBUs configuration described in Fig. 2a. In this condition, the filter acts as a sideband suppress filter after a DSB (Double sideband) modulator, and the passband bandwidth is wide enough to keep the carrier and one of the sidebands unfiltered but suppress other sidebands. It should be mentioned that all the experimental curves shown in Fig. 5 are described on a normalized scale. A flat-top passband is achieved with 0.5 dB ripple bandwidth of 6.4 GHz and 3 dB bandwidth of 8.6 GHz in 19 GHz periodic ranges. The measured out-of-band rejection is greater than 26 dB, limited in principle by the DC controller's precision as well as the OSA's resolution. The lower diagram in Fig. 5b shows the frequency tunability of $H_1(\omega)$ through controlling the phase

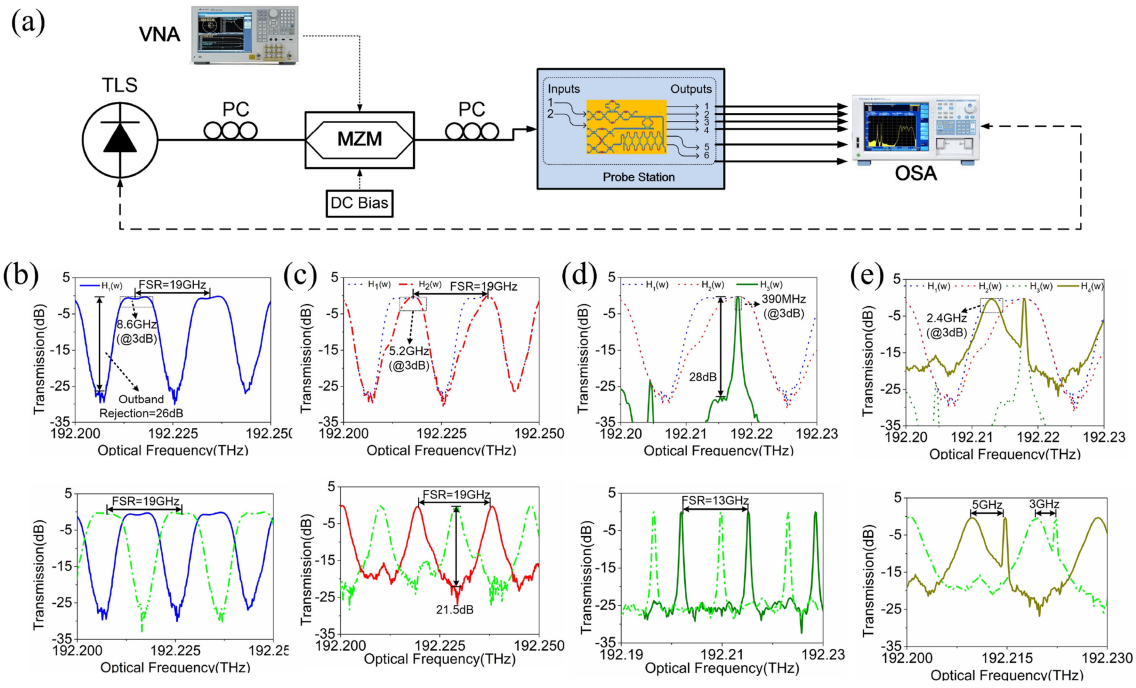

Fig. 5. Measurement results for different nanoprocessor settings: (a) Diagram of the experimental set-up for chip testing, (b), (c), (d), and (e): Results of power response (upper) and frequency tunability (lower) for different settings corresponding to the configurations described in Fig. 3a, Fig. 3b, Fig. 3c, and Fig. 2d, respectively. Individual power spectral responses of the involved subunits ($H_i(\omega)$, i = 1, 2, 3, 4) are displayed by dot and solid lines.

shifters in the RAMZI branch and inside the ring resonator simultaneously. Figure 5c shows the through and drop port responses of the RR in the configuration described in Fig. 3b. Here, the combination $H_2(\omega)$ provides an alternative passband with 3 dB bandwidth change from 5.2 GHz at the through port to 2.4 GHz at the drop port, typically. Fig. 5d corresponds to the narrowband flat-top filter configuration displayed in Fig 2c. In this case, the filter is programmed to exhibit a 3 dB bandwidth of 390 MHz and FSR of 13 GHz. Furthermore, power response comparison among different operations could be observed by a dot and solid curves inside diagrams.

Figure 5e presents the results for the configuration displayed in Fig. 2d. This results from activating subunits 1-3 and combining them in the HC subunit. As illustrated, there are two passbands of different characteristics adjacent to each other but with distinct bandwidths that are designed as described previously to be compatible with the information signal and local oscillator, which can be mixed in the HC subunit if configured as a 2∗4 90° hybrid coupler. Note that this configuration enables the operation as channelizer in WDM coherent systems as the frequency separation between two bandpass peaks can also be tuned as shown in the lower graph in Fig. 5e, since each one is implemented by independent sub units.

4. Conclusion

In summary, we reported and experimentally demonstrated a programmable on-chip RF-Photonic processor towards a photonic RF receiver that is composed of interconnected signal processing subunits. The chip has been fabricated in Si_3N_4 TriPleX technology and packaged for electrical programming, optical interfacing, and testing in the lab. Each subunit can be independently configured both as an active processing subsystem as well as a pure interconnecting 2∗2 device by proper programming of its internal TBUs, which are implemented by means of tunable balanced

Mach-Zehnder interferometers. As a proof of concept, several RF receivers' related configurations have been proved that include out-of-band suppression, carrier-sideband routing, channelization filtering, and I-Q mixing toward a different kind of reception mode. Moreover, in the next stage, we are going to combine the chip testing with the photonic system for more functional verification and further research. It is expected that future work can extend this concept to prove processors with an increased number of subunits to enable a much broader range of applications in communications, sensing, and signal processing.

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