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Weiwei Chen
Hongxiang Li
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Pengjun Wang
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Qiang Fu
Tingge Dai
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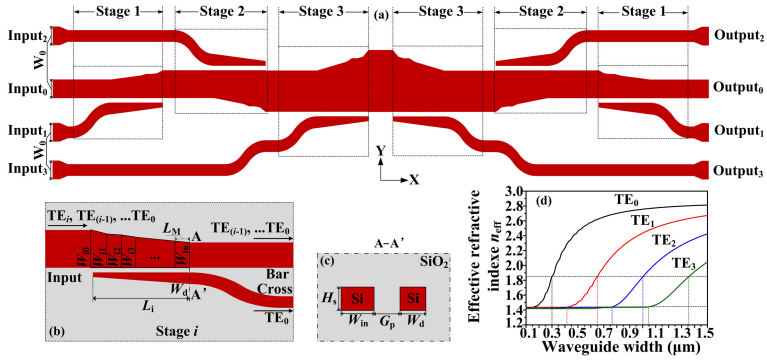

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Silicon Mode (de)Multiplexer Based on Cascaded Particle-Swarm-Optimized Counter-Tapered Couplers

Weiwei Chen,[1] **Hongxiang Li**,[1] **Bohao Zhang**,[1] **Pengjun Wang**,[2] **Shixun Dai**,[1,4] **Yuxiao Liu**,[1] **Jun Li**,[1] **Yan Li**,[1] **Qiang Fu**,[1] **Tingge Dai**,[3] **Hui Yu**,[3] **and Jianyi Yang**[3]

[1]Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo 315211, China
[2]College of Electrical and Electronic Engineering, Wenzhou University, Wenzhou 325035, China
[3]Department of Information Science and Electronics Engineering and Cyrus Tang Center for Sensor Materials and Applications, Zhejiang University, Hangzhou 310027, China
[4]Laboratory of Infrared Materials and Devices, The Research Institute of Advanced Technologies, Ningbo University, Ningbo 315211, China

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Abstract: In this paper, a design of a silicon mode (de)multiplexer based on cascaded counter-tapered couplers is proposed and investigated. By using the particle swarm optimization algorithm and finite difference time domain method, structural parameters of each counter-tapered coupler in our proposed mode (de)multiplexer are optimized so that high conversion efficiencies can be obtained and coupling lengths can be significantly shortened. The coupling lengths of counter-tapered couplers in the proposed silicon four-mode (de)multiplexer operating in transverse-electric polarization are 8 μm, 9 μm, and 10 μm. The corresponding conversion efficiencies are respectively 98.98%, 99.98%, and 98.68%. Experimental results show that, the fabricated device exhibits a demultiplexed crosstalk of -32.76 dB, -27.10 dB, -32.45 dB, or -33.29 dB at 1550 nm wavelength, when the fundamental transverse-electric mode is respectively launched into the ports Input_0, Input_1, Input_2, or Input_3. The measured demultiplexed crosstalk is less than -15.15 dB from 1525 to 1596 nm and lower than -18.12 dB from 1525 to 1561 nm.

Index Terms: Integrated optics, Silicon waveguide, Mode (de)multiplexer, Counter-tapered coupler.

1. Introduction

As the number of parallel processing cores continues to increase, the demand for high-capacity communication between cores and memories would become a tremendous challenge [1]. To address such challenge, silicon-based optical interconnects with the advantage of massive parallelism, high speed, broad bandwidth, and excellent complementary metal-oxide-semiconductor

(CMOS) compatibility can offer an attractive solution [2]–[4]. As is well known, multi-level modulation, wavelength division multiplexing, and polarization division multiplexing are conventional approaches to enhance the transmission capacity. Besides that, mode-division multiplexing (MDM) using each guided mode to act as an independent data channel is drawing a great attention for providing an additional degree of freedom to further increase the transmission capacity [5].

For realizing a densely integrated MDM system, mode (de)multiplexers are one of the key functional components. Up to now, various approaches have been developed to experimentally demonstrate mode (de)multiplexers on the silicon-on-insulator (SOI) platform, such as grating assisted couplers (GACs) [6], [7], adiabatic couplers (ACs) [8]–[12], densely packed multimode waveguide arrays (DPMWAs) [13], [14], inverse design [15]–[17], asymmetric directional couplers (ADCs) [18]–[21], asymmetric Y-junctions [22]–[24], and tapered directional couplers (TDCs) [25], [26]. Although the fabricated GAC-based mode (de)multiplexers can realize low crosstalk, their bandwidths are limited. For the reported AC-based or DPMWA-based mode (de)multiplexers, they can have the low crosstalk level over the broad bandwidth, but relatively large areas are occupied. To achieve compactness, inverse-designed mode (de)multiplexers have been introduced. Nevertheless, it is not easy to expand mode channels further. The ADC-based mode (de)multiplexers can exhibit excellent scalability and good performance, but they are susceptible to fabrication errors owing to the required precise phase matching. By contrast, mode (de)multiplexers based on asymmetric Y-junctions or tapered directional couplers as mode-evolution-based devices are broadband and high tolerance to fabrication errors [16], [27]. However, in reality, it is hard to obtain a very sharp branching angle for the asymmetric Y-junction. By controlling the waveguide width and spacing, the tapered directional coupler provides a promising option for forming the mode (de)multiplexer. But the lengths of the reported TDC-based mode (de)multiplexers are conventionally very long. Thus, it is challenging to achieve a mode (de)multiplexer with compact footprint, low crosstalk, broad bandwidth, and excellent scalability, especially when mode (de)multiplexers are used to construct hybrid (de)multiplexers or switches [28]–[30].

In this paper, we propose a design of a silicon mode (de)multiplexer based on cascaded particle-swarm-optimized counter-tapered couplers. Structural parameters of each counter-tapered coupler are optimized by taking advantage of the particle swarm optimization (PSO) algorithm and finite difference time domain (FDTD) method, and thus high conversion efficiencies can be achieved within the greatly reduced coupling lengths for our designed mode (de)multiplexer. For the designed silicon four-mode (de)multiplexer operating in transverse-electric polarization, the coupling lengths are 8 μm, 9 μm, and 10 μm, and the corresponding conversion efficiencies are 98.98%, 99.98%, and 98.68%. To experimentally demonstrate the viability of this design, the device comprising a four-channel mode multiplexer, a multimode straight waveguide, and a four-channel mode demultiplexer is fabricated on the SOI platform. Experimental results reveal that, for the fabricated device, the demultiplexed crosstalk less than -15.15 dB within a bandwidth from 1525 to 1596 nm and lower than -18.12 dB from 1525 to 1561 nm can be obtained.

2. Principle and Design

Fig. 1(a) shows the structure of a pair of the introduced silicon-based mode (de)multiplexers using cascaded particle-swarm-optimized counter-tapered couplers. A detailed drawing and cross-sectional view of the counter-tapered coupler involved are illustrated in Fig. 1(b) and 1(c). The proposed silicon-based mode (de)multiplexers using cascaded particle-swarm-optimized counter-tapered couplers could be designed for both transverse-electric (TE) and transverse-magnetic (TM) polarizations. Fig. 1(d) describes the effect of the waveguide width on effective refractive indexes of guided modes in a 220-nm-thick silicon strip waveguide at 1550 nm. Here, SiO_2 and Si given by Lumerical FDTD Solutions software are used and TE modes are considered. As seen in Fig. 1(b) and (d), for the counter-tapered coupler in the *i*-th stage, when the effective refractive index of the *i*-th-order ($i = 1, 2 \ldots$) mode in a tapered waveguide is equal to the one of the fundamental mode in the adjacent taper waveguide, the mutual conversion between the fundamental mode and

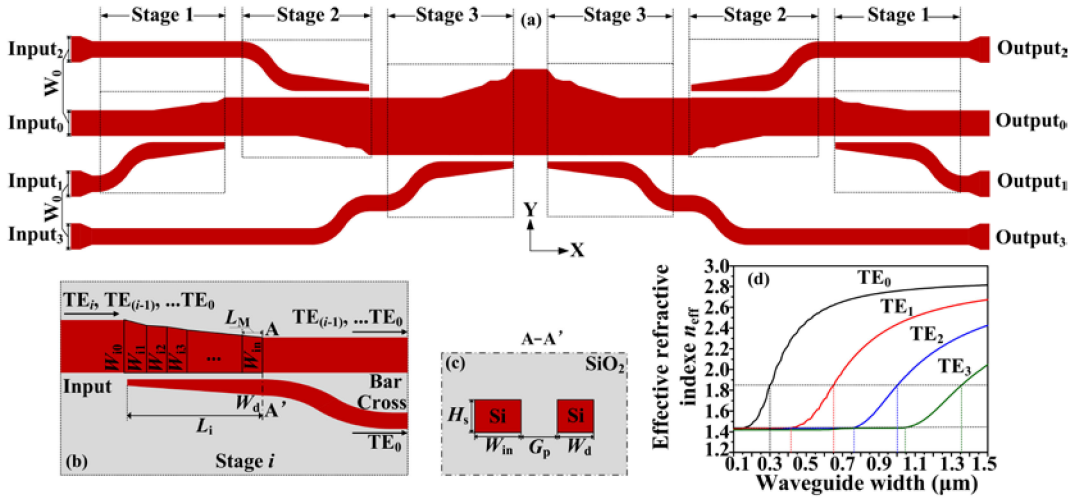

Fig. 1. (a) Schematic of the proposed silicon-based mode (de)multiplexers (b) A detail drawing of the particle-swarm-optimized counter-tapered coupler (c) Corresponding cross-sectional view of the coupling region (d) Calculated effective refractive indexes of eigenmodes in a silicon strip waveguide.

the *i*-th-order mode is realized. In order to achieve excellent performance and compact footprint, structural parameters of each counter-tapered coupler are properly designed.

Note that in Fig. 1(a)–(c), for the counter-tapered coupler in the *i*-th stage, a tapered waveguide in the coupling region is divided into n ($n \geq 1$) segments. Each segment has the same length L_{M} and the width of the segment is labeled as W_{ix} ($x = 0, 1, 2, \ldots, n$). In this work, the FDTD method and PSO algorithm are used to optimize the number n and the width W_{ix}. The definition of the optimization figure of merit (FOM) is given by FOM1 $= P_{\mathrm{Cross\_TEi\_TE0}}$ for the case of $1 \leq x \leq (n-3)$, while FOM is written as FOM2 $= \min(P_{\mathrm{Cross\_TEi\_TE0}}/P_{\mathrm{Bar\_TEi}}, P_{\mathrm{Bar\_TE(i\text{-}1)}}/P_{\mathrm{Cross\_TE(i\text{-}1)\_TE0}}, P_{\mathrm{Bar\_TE(i\text{-}2)}}/P_{\mathrm{Cross\_TE(i\text{-}2)\_TE0}}, \ldots P_{\mathrm{Bar\_TE0}}/P_{\mathrm{Cross\_TE0\_TE0}})$ for the case of $(n-2) \leq x \leq n$. Here, $P_{\mathrm{Cross\_TEi\_TE0}}$ stands for the optical power of $\mathrm{TE_0}$ mode received at the Cross port and $P_{\mathrm{Bar\_TEi}}$ represents the optical power of $\mathrm{TE_i}$ mode received at the Bar port when the $\mathrm{TE_i}$ mode is injected into the Input port at 1550 nm for the counter-tapered coupler in Stage *i*. Each segment's width is regarded as the particle's position and the variation range of segment's width is treated as the velocity of the particle. The position and velocity of the particle are updated by using the following equations [31].

$$ve_{k+1} = w_I \times ve_k + r_1 \times rand() \times (bp_k - ps_k) + r_2 \times rand() \times (gp_k - ps_k) \quad (1)$$

$$ps_{k+1} = ps_k + ve_k \quad (2)$$

where ve_k and ps_k ($k = 1, 2, \ldots$) stand for the particle's velocity and position, bp_k and gp_k represent the individual best position and the global best position, r_1, r_2, w_I and *rand*() are respectively the cognitive rate, the social rate, the inertial weight and the random number uniformly distributed between 0 and 1. The related optimization steps in each stage are as follows.

1) Assign the variable n and set $x = 0$.
2) Initialize the states of particles, including the velocity and position.
3) Set $x = x + 1$ and FOM = FOM1, if $x < n$ is satisfied. Otherwise, set $n = n + 1$ and return to step 1.
4) Set FOM = FOM2, if $x \geq (n-2)$ is satisfied. Otherwise, go to step 5.
5) Carry out FDTD simulation, calculate the corresponding FOM, obtain the individual and global best positions, and update the position and velocity by utilizing (1) and (2).
6) Go to step 7, if the number of iterations reaches the maximum. Otherwise, return to step 5.

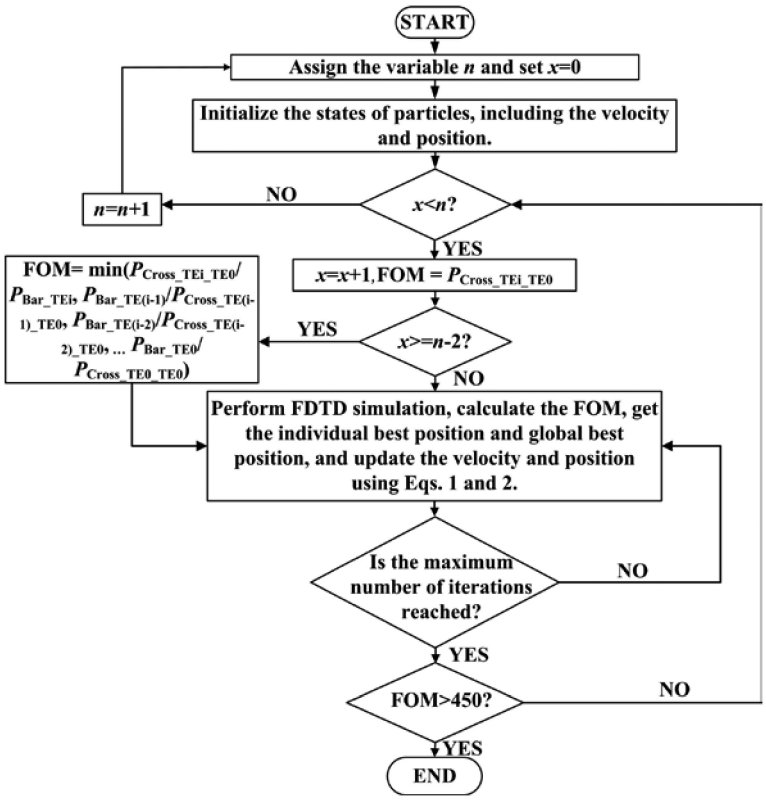

Fig. 2. Flowchart.

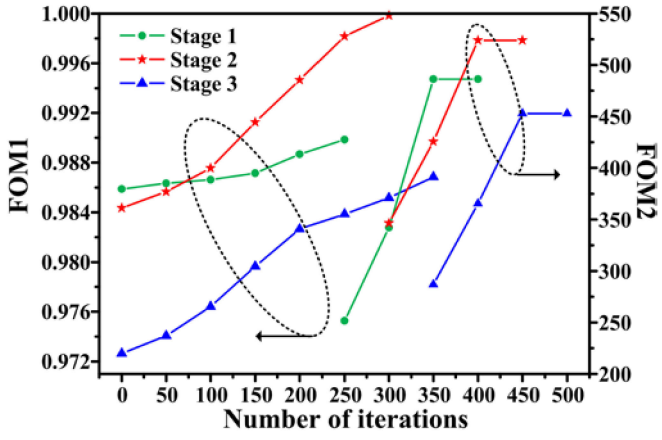

Fig. 3. FOM1 and FOM2 as a function of the number of iterations for the counter-tapered couplers in Stage 1, Stage 2 and Stage 3.

7) Finish the optimization process, if the value of FOM meets the requirements. Otherwise, return to step 3.

The corresponding flowchart is shown in Fig. 2. Fig. 3 describes FOM1 and FOM2 as a function of the number of iterations for the counter-tapered couplers in Stage 1, Stage 2, and Stage 3. In the optimization process, r_1 and r_2 are chosen as $r_1 = r_2 = 2$, the length L_{M} is selected to be 1 μm, the gap G_{p} is set to be 100 nm, and the widths W_{10}, W_{18}, W_{20}, W_{29}, W_{30}, and W_{310} are fixed. The

TABLE 1
Segments' Optimum Widths in μm for Tapered Waveguides in Different Stages

Stage	Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
Stage 1	W_{10}	0.85	W_{11}	0.85	W_{12}	0.76	W_{13}	0.72	W_{14}	0.66
	W_{15}	0.58	W_{16}	0.56	W_{17}	0.53	W_{18}	0.45		
Stage 2	W_{20}	1.05	W_{21}	1.04	W_{22}	0.97	W_{23}	0.98	W_{24}	0.97
	W_{25}	0.93	W_{26}	0.89	W_{27}	0.89	W_{28}	0.88	W_{29}	0.85
Stage 3	W_{30}	1.40	W_{31}	1.36	W_{32}	1.32	W_{33}	1.30	W_{34}	1.25
	W_{35}	1.22	W_{36}	1.21	W_{37}	1.18	W_{38}	1.14	W_{39}	1.10
	W_{310}	1.05								

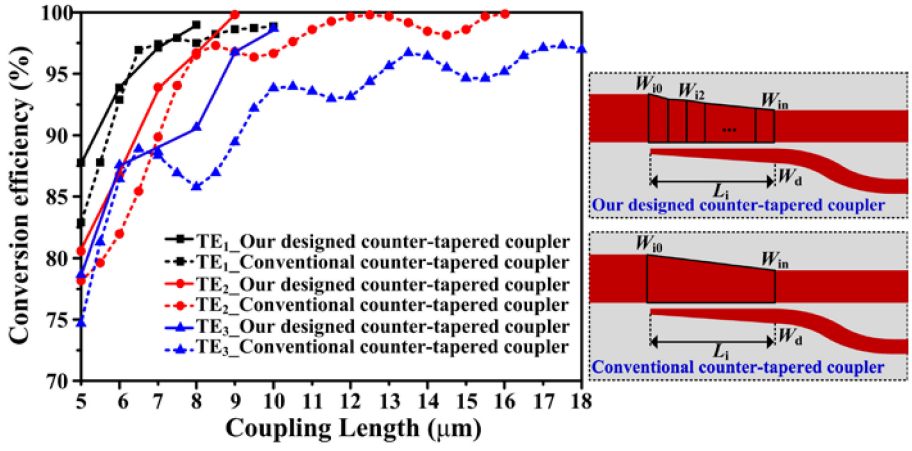

Fig. 4. Conversion efficiencies of the two types of counter-tapered couplers as a function of the coupling length.

optimal widths of segments for tapered waveguides in different stages are summarized in Table 1. It takes about 46 hours, 53 hours, and 60 hours to obtain the optimal widths of segments for tapered waveguides in Stage 1, Stage 2, and Stage 3 on a computer with a 4-core central processing unit (Inter(R) Core(TM) i7-4790), respectively. A comparison of the two types of counter-tapered couplers is shown in Fig. 4. As illustrated in Fig. 4, our designed counter-tapered couplers can have high conversion efficiencies in shorter coupling lengths. When the lengths L_1, L_2 and L_3 are chosen as $L_1 = 8$ μm, $L_2 = 9$ μm, and $L_3 = 10$ μm, conversion efficiencies of our designed counter-tapered couplers can reach 98.98%, 99.98%, and 98.68%.

Fig. 5 illustrates the simulated light propagation in our designed silicon-based mode (de)multiplexers using cascaded particle-swarm-optimized counter-tapered couplers at 1550 nm. As illustrated in Fig. 5(a)–(d), the functionality of our designed silicon-based mode (de)multiplexers can be implemented well. Fig. 6 shows the optical transmission of a pair of our designed silicon-based mode (de)multiplexers as a function of the wavelength when the waveguide width variation ΔW is set to be -10 nm, 0 nm, or 10 nm. As described in Fig. 6, when the waveguide width variation ΔW is 0 nm, the designed device with the TE_0 mode launched into the ports $Input_0$, $Input_1$, $Input_2$, or $Input_3$ can exhibit a demultiplexed crosstalk of -26.19 dB, -24.92 dB, -23.03 dB, or -23.80 dB and an insertion loss of 0.23 dB, 0.05 dB, 0.14 dB, or 0.41 dB at an operating wavelength of 1550 nm. When the wavelength changes from 1500 to 1600 nm, the IL is less than 0.56 dB and the CT is lower than -17.68 dB. Here, the IL is defined as $IL_m = -10\log(P_{Outputm}/P_{Inputm})$, where $P_{Outputm}$ and P_{Inputm} respectively stand for the optical output power received from the output port

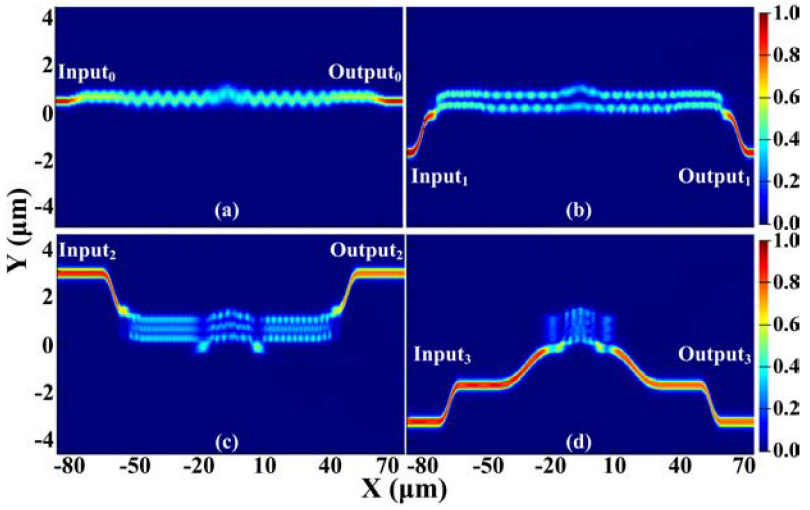

Fig. 5. Simulated light propagation in our designed silicon-based mode (de)multiplexers with TE_0 modes launched into the ports (a) $Input_0$, (b) $Input_1$, (c) $Input_2$, and (d) $Input_3$.

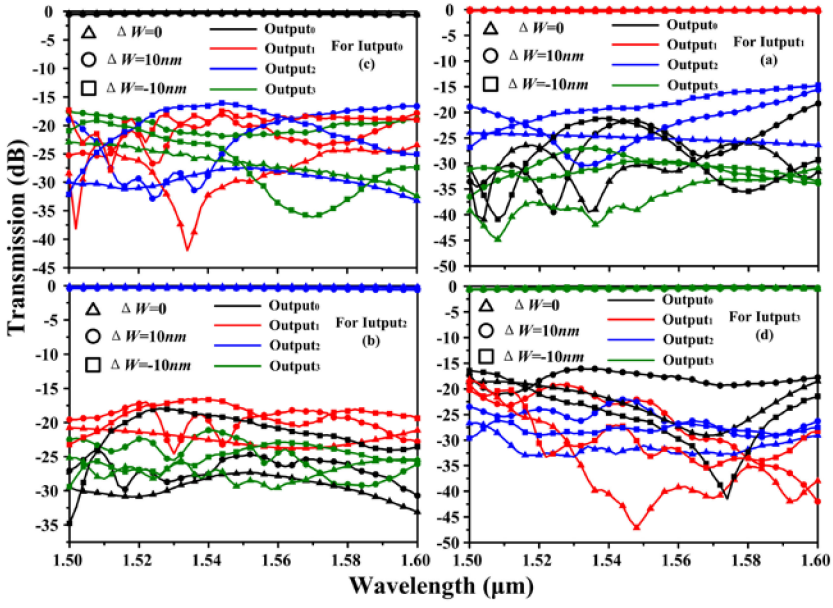

Fig. 6. Simulated transmission spectra of a pair of our designed silicon-based mode (de)multiplexers with different values of the waveguide width variation ΔW.

$Output_m$ and the optical power launched into the input port $Input_m$ ($m = 0, 1, 2, 3$). The definition of the demultiplexed crosstalk is described as the ratio of the maximum power at the undesired output port to the power at the desired output port. If the waveguide width variation ΔW is -10 nm, the corresponding IL and CT will be respectively lower than 0.64 dB and -15.21 dB within a bandwidth from 1500 to 1590 nm. For the case of $\Delta W = 10$ nm, the IL is smaller than 0.69 dB and the CT is less than -15.57 dB from 1500 to 1600 nm. Fig. 7 depicts conversion efficiencies of the four modes in our proposed silicon-based mode demultiplexer changing with the angle θ. W_w represents the

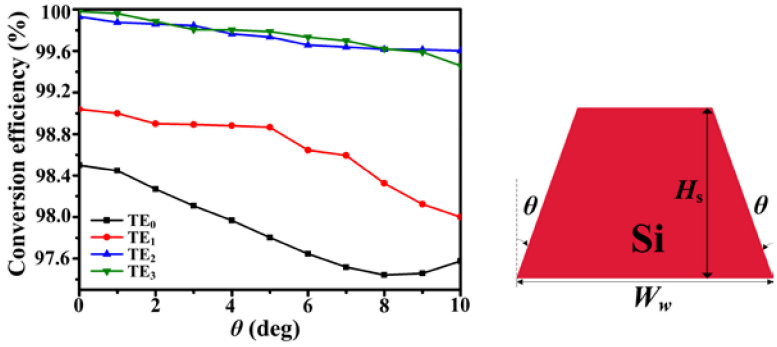

Fig. 7. Conversion efficiencies of the four modes in our proposed silicon-based mode demultiplexer as a function of the angle θ.

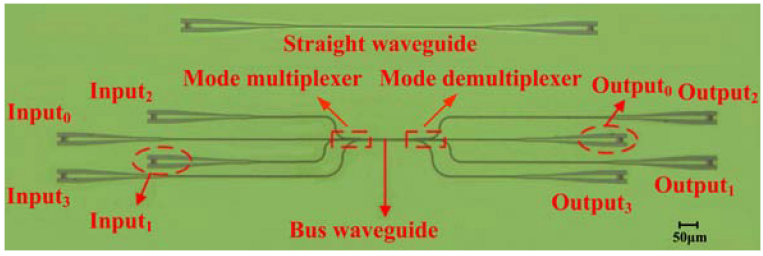

Fig. 8. Microscope image of the fabricated device.

width of the silicon waveguide. As shown in Fig. 7, it can be seen that conversion efficiencies would gradually decrease with the increase of the angle θ.

3. Fabrication and Characterization

The designed silicon-based mode (de)multiplexers using cascaded particle-swarm-optimized counter-tapered couplers are fabricated on an SOI wafer with a top silicon of 220 nm thickness and a buried oxide layer of 2 μm thickness. Structures are patterned and fully etched by utilizing electron-beam lithography and inductively coupled-plasma dry etching. A plasma-enhanced chemical vapor deposition process is used for forming a 1.5-μm-thick SiO_2 layer as the upper cladding layer. The microscope image of a straight waveguide and a fabricated device consisting of a mode multiplexer, a bus waveguide, and a mode demultiplexer is illustrated in Fig. 8.

To characterize the fabricated device, a broadband (1525 nm–1600 nm) amplified spontaneous emission source and an optical spectrum analyzer (YOKOGAWA AQ6317B) are used. The transmission spectra are obtained at the four output ports as the light beam is injected into each one of the input ports. Fig. 9 depicts the measured transmission spectra. The measured transmission is normalized with reference to the measured transmission of a straight waveguide on the same chip. From Fig. 9, it is seen that, as the TE_0 mode is injected into the ports $Input_0$, $Input_1$, $Input_2$, or $Input_3$, the measured demultiplexed crosstalk of the fabricated device is respectively -32.76 dB, -27.10 dB, -32.45 dB, or -33.29 dB at a wavelength of 1550 nm. Within a bandwidth from 1525 to 1596 nm, the fabricated device can have a demultiplexed crosstalk less than -15.15 dB and an insertion loss smaller than 4.73 dB. The demultiplexed crosstalk can be lower than -18.12 dB from 1525 to 1561 nm. The main reasons behind the contradictions between simulated and experimental results are given below: firstly, the sidewall roughness of the fabricated waveguide causes the scattering loss [32], secondly, spectral ripples could be induced by the fabrication imperfection of grating couplers [12], and thirdly, the widths of the fabricated waveguides could be inconsistent with

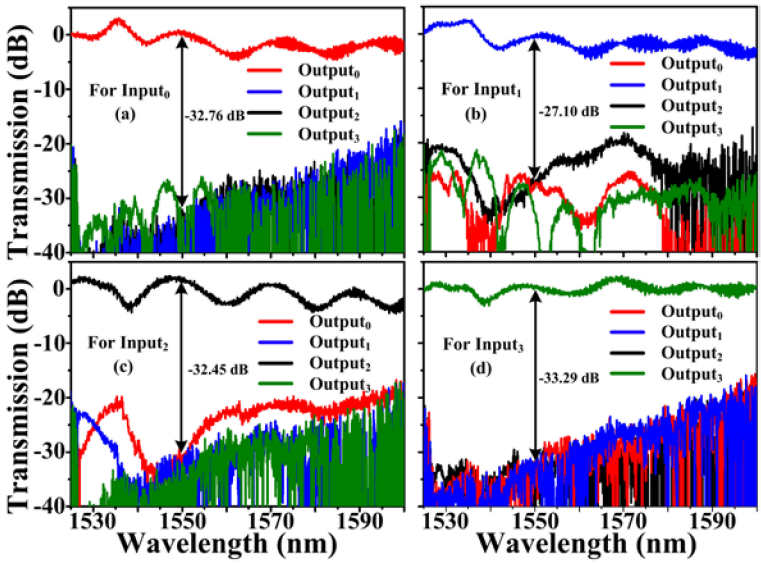

Fig. 9. Measured transmission spectra of the fabricated device.

Table 2
Comparison of the Reported Fabricated Silicon Four-Mode (de)Multiplexers

Structure	Channels	Bandwidth (nm)	Insertion Loss (dB)	Crosstalk (dB)	Coupling Length (μm)			
AC [11]	4(TE)	1500-1600	<1.30	<-23.00	150 (TE_0-TE_1)	150 (TE_0-TE_2)	150 (TE_0-TE_3)	
inverse design [17]	4(TE)	1510-1570	<1.50	<-14.60	6[a] (TE_0, TE_0, TE_0- TE_0, TE_1, TE_2, TE_3)			
ADC [19]	4(TM)	~20	<1.00	≤-23.00	4.50 (TM_0-TM_1)	7.00 (TM_0-TM_2)	9.70 (TM_0-TM_3)	
TDC [28]	4(TE)	1535-1570	~<2.40[b]	~<-14.00[b]	22.50 (TE_0-TE_1)	40.50 (TE_0-TE_2)	60.00 (TE_0-TE_3)	
Subwavelength grating [30]	4(TE2+TM2)	1540-1550	<6.60	<-18.70	300 (TE_0-TE_0)	300 (TE_0-TE_1)	300 (TM_0-TM_0)	300 (TM_0-TM_1)
This Work	4(TE)	1525-1596	<4.73	<-15.15	8.00 (TE_0-TE_1)	9.00 (TE_0-TE_2)	10.00 (TE_0-TE_3)	

[a]The length of an angled taper waveguide. [b]The values of insertion loss and crosstalk are estimated from Fig. 3 in Ref. [28].

the optimal widths of the designed waveguides owing to fabrication errors so that the demultiplexed crosstalk and insertion loss would be affected. Additionally, due to the limited bandwidth of the light source, the measured bandwidth of our fabricated device is not as large as the simulated one. A comparison of our device with other fabricated silicon four-mode (de)multiplexers is summarized in Table 2. As seen in Table 2, although the inverse-designed mode (de)multiplexer has an ultra-compact size, it is not easy to add more mode channels. The ADC-based mode (de)multiplexer operating in TM polarization can achieve compact footprint, low crosstalk, and small insertion loss. However, as is known, according to the coupling length $L_c = \pi / (\beta_{even} - \beta_{odd})$ associated with the difference between the propagation constant of the even mode and that of the odd mode [33], the required coupling length for TM polarization is shorter than the one for TE polarization. When our proposed mode (de)multiplexers is designed for TM polarization, the corresponding coupling lengths are 5 μm, 7 μm, and 9 μm. The simulated insertion loss and crosstalk can be respectively lower than 0.25 dB and -23.17 dB within a bandwidth from 1528 to 1560 nm. Compared with reported fabricated silicon four-mode (de)multiplexers using couplers operating in TE polarization, the coupling lengths of our proposed device can be significantly shortened. Additionally, our proposed device can realize low crosstalk, broad bandwidth, and good scalability. In order to improve the demultiplexed crosstalk, expand the bandwidth, and lessen the insertion

loss further, high-quality fabrication processes are needed to reduce the sidewall roughness, realize high-performance grating couplers, and improve the accuracy [34]. Our design of the silicon mode (de)multiplexer using cascaded particle-swarm-optimized counter-tapered couplers is also suitable to be fabricated in foundry platforms and the corresponding structural parameters ought to be redesigned according to the minimum feature size design rule.

4. Summary

In conclusion, we have proposed and investigated a design of a silicon mode (de)multiplexer utilizing cascaded particle-swarm-optimized counter-tapered couplers. For our designed silicon mode (de)multiplexers, high conversion efficiencies can be realized within compact coupling lengths. For the fabricated device composed of a four-channel mode multiplexer, a bus waveguide, and a four-channel mode demultiplexer, the measured demultiplexed crosstalk is respectively -32.76 dB, -27.10 dB, -32.45 dB, or -33.29 dB at 1550 nm wavelength when the TE_0 mode is injected into the port $Input_0$, $Input_1$, $Input_2$, or $Input_3$. The demultiplexed crosstalk can be less than -15.15 dB within a bandwidth from 1525 to 1596 nm and lower than -18.12 dB from 1525 to 1561 nm. With the characteristics of compact footprint, high CMOS compatibility, broad bandwidth, low crosstalk, and good scalability, our introduced silicon mode (de)multiplexer utilizing cascaded particle-swarm-optimized counter-tapered couplers provides an attractive choice for constructing multi-dimensional-multiplexing optical network-on-chip.

References

[1] T. Alexoudi *et al.*, "Optics in computing: From photonic network-on-chip to chip-to-chip interconnects and disintegrated architectures," *J. Lightw. Technol.*, vol. 37, no. 2, pp. 363–379, Jan. 2019.

[2] X. Chen *et al.*, "The emergence of silicon photonics as a flexible technology platform," *Proc. IEEE*, vol. 106, no. 12, pp. 2101–2116, Dec. 2018.

[3] A. H. Atabaki *et al.*, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," *Nature*, vol. 556, no. 7701, pp. 349–354, Apr. 2018.

[4] A. Rahim, T. Spuesens, R. Baets, and W. Bogaerts, "Open-access silicon photonics: Current status and emerging initiatives," *Proc. IEEE*, vol. 106, no. 12, pp. 2313–2330, Dec. 2018.

[5] G. F. Li, N. Bai, N. B. Zhao, and C. Xia, "Space-division multiplexing: The next frontier in optical communication," *Adv. Opt. Photon.*, vol. 6, no. 4, pp. 413–487, Dec. 2014.

[6] Y. He *et al.*, "Silicon high-order mode (De)Multiplexer on single polarization," *J. Lightw. Technol.*, vol. 36, no. 24, pp. 5746–5753, Dec. 2018.

[7] G. F. R. Chen, T. Wang, K. J. A. Ooi, A. K. L. Chee, L. K. Ang, and D. T. H. Tan, "Wavelength selective mode division multiplexing on a silicon chip," *Opt. Express*, vol. 23, no. 6, pp. 8095–8103, Mar. 2015.

[8] J. J. Xing, Z. Y. Li, X. Xiao, J. Z. Yu, and Y. D. Yu, "Two-mode multiplexer and demultiplexer based on adiabatic couplers," *Opt. Lett.*, vol. 38, no. 17, pp. 3468–3470, Sep. 2013.

[9] L. Sun, Y. Yu, G. Y. Chen, and X. L. Zhang, "Silicon mode multiplexer processing dual-path mode-division multiplexing signals," *Opt. Lett.*, vol. 41, no. 23, pp. 5511–5514, Dec. 2016.

[10] Z. R. Zhang, Y. Yu, and S. N. Fu, "Broadband on-chip mode-division multiplexer based on adiabatic couplers and symmetric Y-junction," *IEEE Photon. J.*, vol. 9, no. 2, pp. 1–7, Apr. 2017.

[11] F. Guo and T. Chu, "Silicon mode (de)multiplexers with parameters optimized using shortcuts to adiabaticity," *Opt. Express*, vol. 25, no. 8, pp. 9160–9170, Apr. 2017.

[12] L. H. Xu *et al.*, "Ultra-Broadband and compact two-mode multiplexer based on subwavelength-grating-slot-assisted adiabat coupler for the Silicon-on-Insulator platform," *J. Lightw. Technol.*, vol. 37, no. 23, pp. 5790–5800, Dec. 2019.

[13] H. N. Xu and Y. C. Shi, "Broadband nine-channel mode-division (de) multiplexer based on densely packed multimode waveguide arrays," *J. Lightw. Technol.*, vol. 35, no. 22, pp. 4949–4953, Nov. 2017.

[14] K. X. Chen, L. Liu, and S. L. He, "Mode division multiplexing based on supermodes in densely packed uniform waveguide array (DPUWA)," *IEEE Photon. J.*, vol. 12, no. 2, pp. 1–10, Apr. 2020.

[15] L. F. Frellsen, Y. Ding, O. Sigmund, and L. H. Frandsen, "Topology optimized mode multiplexing in silicon-on-insulator photonic wire waveguides," *Opt. Express*, vol. 24, no. 15, pp. 16866–16873, Jul. 2016.

[16] W. J. Chang *et al.*, "Ultra-compact mode (de) multiplexer based on subwavelength asymmetric Y-junction," *Opt. Express*, vol. 26, no. 7, pp. 8162–8170, Apr. 2018.

[17] H. C. Xie *et al.*, "Highly compact and efficient four-mode multiplexer based on pixelated waveguides," *IEEE Photon. Technol. Lett.*, vol. 32, no. 3, pp. 166–169, Feb. 2020.

[18] Y. H. Ding, J. Xu, F. D. Ros, B. Huang, H. Y. Ou, and C. Peucheret, "On-chip two-mode division multiplexing using tapered directional coupler-based mode multiplexer and demultiplexer," *Opt. Express*, vol. 21, no. 8, pp. 10376–10382, Apr. 2013.

[19] D. X. Dai, J. Wang, and Y. C. Shi, "Silicon mode (de)multiplexer enabling high capacity photonic networks-on-chip with a single-wavelength-carrier light," *Opt. Lett.*, vol. 38, no. 9, pp. 1422–1424, May 2013.
[20] L. W. Luo *et al.*, "WDM-compatible mode-division multiplexing on a silicon chip," *Nat. Commun.*, vol. 5, no. 3069, pp. 1–7, Jan. 2014.
[21] J. P. Nath, N. Dhingra, G. J. Saxena, and E. K. Sharma, "Compact mode division (de)Multiplexer based on collaterally coupled SOI waveguides," *IEEE Photon. Technol. Lett.*, vol. 32, no. 10, pp. 595–598, May 2020.
[22] J. B. Driscoll, R. R. Grote, B. Souhan, J. I. Dadap, M. Lu, and R. M. Osgood, "Asymmetric y junctions in silicon waveguides for on-chip mode-division multiplexing," *Opt. Lett.*, vol. 38, no. 11, pp. 1854–1856, Jun. 2013.
[23] W. W. Chen *et al.*, "Silicon three-mode (de)multiplexer based on cascaded asymmetric Y junctions," *Opt. Lett.*, vol. 41, no. 12, pp. 2851–2854, Jun. 2016.
[24] H. Q. Li *et al.*, "Experimental demonstration of a broadband two-mode multi/demultiplexer based on asymmetric Y-junctions," *Opt. Laser Technol.*, vol. 100, pp. 7–11, Mar. 2018.
[25] J. Wang *et al.*, "Broadband and fabrication-tolerant on-chip scalable mode division multiplexing based on mode-evolution counter-tapered couplers," *Opt. Lett.*, vol. 40, no. 9, pp. 1956–1959, May 2015.
[26] D. X. Dai *et al.*, "10-Channel Mode (de)multiplexer with dual polarizations," *Laser Photon. Rev.*, vol. 12, no. 1, pp. 1–9, Jan. 2018.
[27] S. Gross, N. Riesen, J. D. Love, and M. J. Withford, "Three-dimensional ultra-broadband integrated tapered mode multiplexers," *Laser Photon. Rev.*, vol. 8, no. 5, pp. L81–L85, Sep. 2014.
[28] Y. Tan, H. Wu, S. P. Wang, C. L. Li, and D. X. Dai, "Silicon-based hybrid demultiplexer for wavelength- and mode-division multiplexing," *Opt. Lett.*, vol. 43, no. 9, pp. 1962–1965, May 2018.
[29] Y. Zhang, R. H. Zhang, Q. M. Zhu, Y. Yuan, and Y. K. Su, "Architecture and devices for silicon photonic switching in wavelength, polarization and mode," *J. Lightw. Technol.*, vol. 38, no. 2, pp. 215–225, Jan. 2020.
[30] Y. He, Y. Zhang, H. W. Wang, L. Sun, and Y. K. Su, "Design and experimental demonstration of a silicon multi-dimensional (de)multiplexer for wavelength-, mode- and polarization-division (de)multiplexing," *Opt. Lett.*, vol. 45, no. 10, pp. 2846–2849, May 2020.
[31] Y. Zhang *et al.*, "A compact and low loss Y-junction for submicron silicon waveguide," *Opt. Express*, vol. 21, no. 1, pp. 1310–1316, Jan. 2013.
[32] E. Jaberansary, T. M. B. Masaud, M. M. Milosevic, M. Nedeljkovic, G. Z. Mashanovich, and H. M. H. Chong, "Scattering loss estimation using 2-D fourier analysis and modeling of sidewall roughness on optical waveguides," *IEEE Photon. J.*, vol. 5, no. 3, pp. 1–10, Jun. 2013.
[33] B. E. Little and W. P. Huang, "Coupled-mode theory for optical waveguides," *Prog. Electromagn. Res.*, vol. 10, pp. 217–270, Jun. 1995.
[34] M. Pantouvaki *et al.*, "50 Gb/s silicon photonics platform for short-reach optical interconnects," in *Proc. Opt. Fiber Commun. Conf.*, 2016, Paper Th4H.