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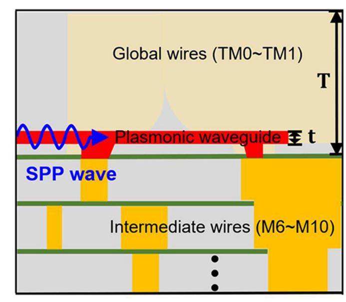

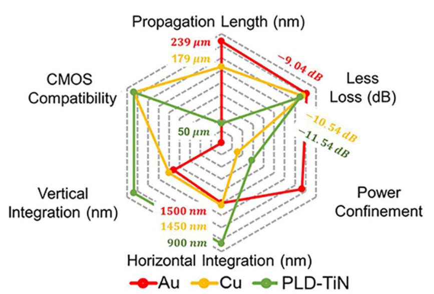

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The Design of CMOS-Compatible Plasmonic Waveguides for Intra-Chip Communication

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Abstract: A CMOS-compatible plasmonic waveguide with a metal or metal-like strip sandwiched in-between dielectrics has been proposed for intra-chip communication in the more-than-Moore era. A sequence of numerical models has been presented to evaluate the plasmonic waveguide performance. For device-level consideration, we demonstrated through simulations that Cu (1450 nm pitch) and PLD-TiN (900 nm pitch) plasmonic waveguides symmetrically sandwiched by SiO_2 with much smaller and hence denser interconnects, are promising candidates for use in global wires for the asynchronous communication. This design of plasmonic waveguide can bridge the CMOS circuitry and high-speed communication at optical frequencies within chip. For a system-level assessment, both of them have the same bandwidth throughput of ~19.8 Gbps. The other performance parameters of Cu and PLD-TiN plasmonic waveguides are respectively, signal latency of ~0.18 ps and 0.19 ps, energy dissipation per computing bit of $\sim 2.5 \times 10^{-3}$ fJ/bit and 3.8×10^{-3} fJ/bit, and 25% crosstalk coupling length of 155 μm and 125 μm. These findings suggest that plasmonic waveguide for intra-chip communication surpass those of existing electronic interconnects for all the categories of performance parameters.

Index Terms: CMOS-compatible plasmonic waveguide, Long-range SPP, high integration density, Signal latency, Energy dissipation, Link throughput, Crosstalk effect.

1. Introduction

In the pursuit of Moore's law for traditional electronic integrated circuits, innovation is required to overcome the challenges in both physics and economics beyond the 10 nm node [1]. These challenges include overcoming the diffraction limit of photolithography, maintaining the bandwidth per computing interconnect and lowering the power consumption of data movement. The available bandwidth per computing operation continues to drop and will likely reach its limit at 5 nm CMOS technology node according to the 2013 International Technology Roadmap for Semiconductor (ITRS) [2]. The increasing demand of data rates requires novel interconnect technologies to replace classical electronic wires, particularly in terms of signal latency, energy dissipation per bit, wire throughput, crosstalk effect and higher level of integration.

Beyond that, the interconnect delay time remains a significant challenge towards the realization of purely electronic circuits operating above $\sim$10 GHz. In stark contrast, photonic devices possess an enormous bandwidth ($\sim 10^{12}$ Hz). Unfortunately, dielectric photonic components are hampered in their size by the laws of light diffraction [3]. Plasmonic devices operating at optical frequencies ($\sim 10^{13}$ to 10^{15} Hz) are able to realize high speed data transport and large bandwidth. Since these electrical signals in CMOS circuitry work at optical frequencies, they can be converted to optical signals by a plasmonic actuator at the wavelength we have chosen (1550 nm), if the need arises to output them for external transmission through optical fibers [4]–[7]. Electrons traveling in electronic wire are limited in speed to only 2.2×10^6 m/s, while the surface plasmon polaritons (SPP) propagating along plasmonic waveguides can reach a speed of 2.7×10^8 m/s, very close to the speed of light. According to the chart of the operating frequencies versus critical dimensions in different chip-scale device technologies [8], plasmonics has the potential to play an unique and important role in enhancing the processing speed of future integrated circuits. They interface naturally with electronic devices being similar in dimension but working at the speed of photonic devices. In the prevailing 10 nm technology from Intel [9], it is seen that the global wires (top metals) with pitch of $\sim$11 μm for asynchronous communication occupy a large footprint both in the vertical and lateral directions. To satisfy the requirements of high-speed data transport, several choices of materials are available for plasmonic waveguides such as metals [10], transition metal nitrides [11] and transparent conducting oxides [12], perovskite oxides and chalcogenides [13].

The remainder of the paper is organized as follows. In Section 2, we propose an architecture of plasmonic interconnects integrated with tunnel junction within IC chip, which can increase both the chip density and improve data transfer rate effectively. In Section 3, we investigate the symmetrical multilayer structures (I-M-I) which is being proposed for use in plasmonic interconnects. CMOS-compatible Cu and PLD-TiN plasmonic waveguides sandwiched by SiO_2 show superior performance in signal latency, energy dissipation, link throughput and crosstalk immunity over traditional Cu wires. Finally, our conclusions are summarized in Section 4.

2. Architecture of Plasmonic Interconnect Integrated With Tunnel Junction in IC Chip

In the back-end-of-line (BEOL) of 10 nm CMOS technology [9], the local wires (Metal 0 to Metal 5) and intermediate wires (Metal 6 to Metal 10) are deposited layer by layer with pitches in the range of 36 to 160 nm. They exhibit the desirable interconnect characteristics of a small RC delay, low noise and high-speed data transport. However, in the level of asynchronous communication within chip the global wires (top metal layers) are much thicker (thickness, T $\sim$ 6 μm) and with a wider pitch ($\sim$1 to 11 μm) than the metal layers beneath (local and intermediate wires), in order to decrease the series resistance and improve the Q-factor for broader bandwidth data transport. However, they consume a lot of chip area. Thus, the footprint and data transport efficiency of global wires will increasingly impede the pursuit of chip scaling beyond the 10 nm node. We propose to replace the global wires (Fig. 1(a) in beige) with plasmonic waveguides (in red) for asynchronous blocks communication to save chip area and improve data transport speed. Without external clock signals, a data packet (e.g., 64 bits) can be transmitted within chip intermittently. The surface plasmon

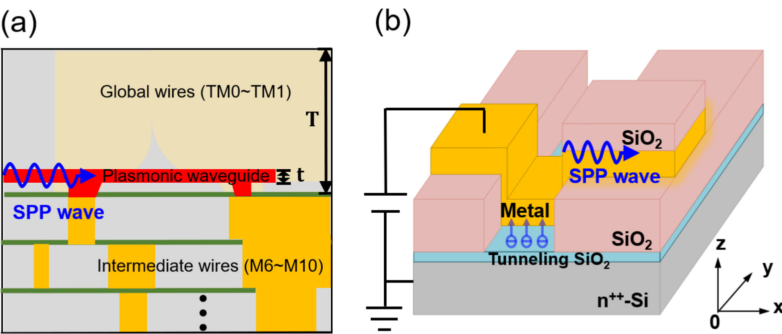

Fig. 1. Architectural concept of monolithic integration of integrated circuit with plasmonic technology. (a) Cross-section of BEOL structure in plasmonic technology, the global wires (in beige) are replaced by plasmonic waveguide (in red) in top metal level. The thickness of plasmonic interconnect (t) is much thinner than that of global wire (T). (b) Schematic illustration of the device consisting of tunnel junction (Metal-Insulator-Silicon, MIS) integrated with a plasmonic waveguide. The electrons inelastically tunnel through the oxidation barrier (tunneling SiO_2) to excite SPP wave (blue wiggle arrow) propagating along the insulator-metal-insulator (I-M-I) plasmonic waveguide (x-direction) under a forward bias on metal electrode.

polaritons (SPP) carrier waves (in blue) can be generated at both the interfaces of top global metal and propagate along the interfaces at optical frequencies. As will be shown later, when the metal is thin enough, two hybridized modes are formed. The thickness (t) of top global metal wires can be reduced to tens of nanometers and the pitch is reduced to around 1 μm. The signal transmission performances under the categories of signal latency, power dissipation and crosstalk far exceed those of traditional electronic interconnects. Fig. 1(b) shows a tunnel junction, whereby its tunneling current excites the plasmons in its metal electrode which also serve as a plasmonic waveguide. The tunnel junction effectively functions as a plasmon source. Thus, the SPP waves propagate along the plasmonic waveguide. This has been verified experimentally in our previous work [14]. For CMOS compatibility, metal-insulator-silicon tunnel junction (MIS TJ) as a plasmonic source is one of the best candidates to convert electron to plasmon via inelastic tunneling, which has been also proven theoretically in our previous work [11]. In this work, we focus on the design and optimization of an I-M-I plasmonic waveguide for intra-chip communication.

In a given plasmonic waveguide, many different SPP modes can be excited at each individual metal-dielectric interface and they interact with one another to form hybrid modes [16], [17]. The metal layers proposed for intra-chip interconnects are always sandwiched between two dielectric layers, which is often referred to as the insulator-metal-insulator (I-M-I) structure. Since plasmonic waveguides will substitute for the traditional global wire (top metal) in an IC chip, we commence by considering the SPP modes in the symmetric I-M-I configuration of a thin metal or metal-like strip sandwiched between the dielectric films. When the two SPP modes at the two metal/insulator interfaces couple with each other at small thickness of the metal or metal-like strip [16], [20], the modes hybridize to form the long-range (LR) and short-range (SR) SPP with different propagation constants. As its name implies, the LR-SPP has been shown to be superior to SR-SPP in terms of signal transmission and is the one chosen for applications.

The mode properties of SPPs are investigated by means of the finite-element method (FEM) using the commercial software COMSOL^{TM} with the scattering boundary condition and the simulation domain surrounded by a rectangular perfectly matched layer (PML) in order to avoid reflection and to confine the geometry. Scattering boundary condition is applied to make the boundary transparent for a scattered wave. The degenerate n-Si has complex dielectric constant ($\varepsilon_1 + i * \varepsilon_2$) which at the wavelength of interest viz. 1550 nm is taken to be ($7.84 - i * 0.0008$) [21], whereas Au is ($-112.0 + i * 24.6$). As mentioned above, we only consider the SPP modes in the I-M-I configuration of a thin Au strip sandwiched between SiO_2 films. When the thickness of the Au strip is reduced to several tens of nanometers, the two individual SPP modes at both interfaces of the Au strip with the insulators are transformed into two p-polarized bound hybridized modes,

that exhibit distinct dispersion characteristics and a distinct evolution with structure parameters (dielectric constant, ε and Au thickness, t). The configuration of the transverse magnetic field results from the redistribution of the charge density in the Au film due to the surface plasmon resonance [22]. As we mentioned before, in the actual circuit implementation, the SPP would be excited by tunnel junctions [14], [23], but since a physical model is not firmly established and the experimental technique is not mature, we thus use the conventional method to generate the SPP waves optically in our model. Although a spectrum of wave vectors of SPP is generated by a tunnel junction, a single-wavelength SPP wave can be coupled into a definite plasmonic waveguide selectively with the use of a surface grating to improve excitation efficiency, which is not the subject of the current paper.

3. Design of I-M-I Plasmonic Interconnects

For data transmission, in an environment where the LR-SPP and SR-SPP have very different propagation characteristics, the long-range surface plasmon-polaritons (LR-SPP) is naturally selected. For a symmetrical I-M-I plasmonic waveguide, it is of interest to increase the LR-SPP propagation length by suppressing SR-SPP during the initial mode competition between LR- and SR-SPP propagation. The propagation length L_D, is defined as the exponent of the power decay given by e^{-x/L_D} as the wave propagates. The SPP working frequency corresponding to the optical wavelength of 1550 nm is chosen for plasmonic waveguide design so that the chip's output can be transmitted as an optical signal via an optical fiber. Taking a 40 nm Au strip sandwiched between $\mathrm{SiO_2}$ dielectric films for example in our numerical model, the LR-SPP propagation length reaches 239 μm, while the SR-SPP propagation length is $\sim$ 10.3 μm. The LR-SPP is the dominant mode for data transmission in I-M-I plasmonic waveguide. While Au (free carrier density of 5.90×10^{22} $\mathrm{cm^{-3}}$and real dielectric constant of -112.0 at 1550 nm) is the standard plasmonic metal used, it cannot be used in Si foundries and CMOS-friendly materials such as Cu and PLD-TiN with sufficient free carrier density (Cu: 8.50×10^{22} $\mathrm{cm^{-3}}$ and PLD-TiN: 6.75×10^{22} $\mathrm{cm^{-3}}$) and negative real dielectric constant (Cu: -119.0 and PLD-TiN: -75.0 at 1550 nm) in the visible to near-infrared are the alternatives [24], [25]. It is known that the electrical and optical properties of metal-nitride film can be tuned during film growth, which offers flexibility in design than the use of pure metal (Cu, Al) with fixed properties. In this work, we propose to use single crystalline PLD-TiN film for plasmonic waveguide grown by pulsed laser deposition (PLD). The PLD-TiN is deposited on the sapphire substrate with a thickness of 45 nm using a growth temperature of 950 $^{\circ}$C, at a $\mathrm{N_2}$ pressure of 1.0×10^{-4} Torr, $\mathrm{N_2}$ gas flow of 2 sccm, and a RF power of 250 W. The stoichiometric ratio of $\mathrm{Ti_xN_y}$ equals to 0.48 : 0.52 verified by Rutherford Back scattering spectroscopy, which is controlled accurately in this deposition by applying the plasma source in the PLD chamber [26]. The permittivity of this PLD-TiN film was characterized by ellipsometry in the wavelength range of 325 nm to 2000 nm ($\varepsilon_2 = -83.24$ at 1550 nm) and the electrical properties of carrier density (7.99×10^{22} $\mathrm{cm^{-3}}$), electron mobility ($2.64\ \mathrm{cm^2/(V \cdot s)}$), and resistivity ($29.54\ \mu\Omega \cdot \mathrm{cm}$) were measured by the physical property measurement system (PPMS). Both the optical and electrical properties shown above indicated that PLD-TiN is a promising candidate for plasmonic waveguide application.

An important parameter for waveguides is power confinement factor (PCF) defined as the ratio of mode power carried through the metal or metal-like waveguide's cross section with respect to the entire mode power carried by the guide and in the adjacent dielectrics. The power confinement factor can be expressed as [22],

$$\mathrm{PCF} = \frac{\left|\iint_{A_c} S_x ds\right|}{\left|\iint_{A_\infty} S_x ds\right|} \tag{1}$$

where A_c is taken as the area of the waveguide core and A_∞ applies the entire waveguide cross section, S_x refers to the x component (propagation direction) of the Poynting vector. Here, only the power confinement of LR-SPP is of consequence for signal transmission since the SR-SPP has

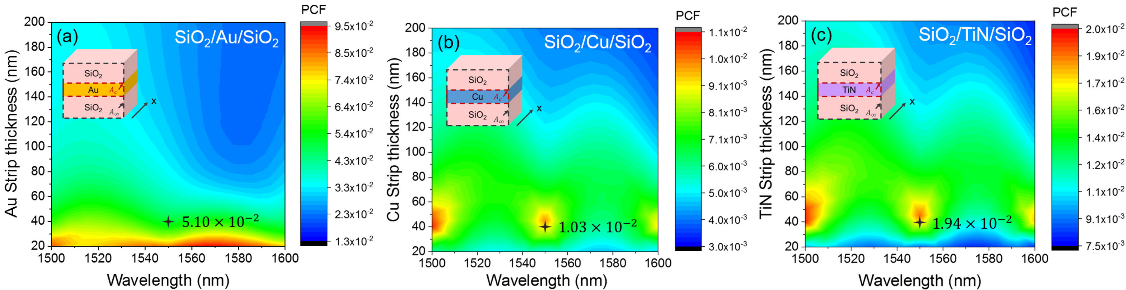

Fig. 2. Power confinement factor of SiO_2/metal/SiO_2 plasmonic waveguide, (a) SiO_2/Au/SiO_2, (b) SiO_2/Cu/SiO_2, and (c) SiO_2/PLD-TiN/SiO_2. The black cross marks the power confinement factors (PCFs) of the plasmonic waveguides with a 40 nm metal sandwiched in SiO_2 film and working at SPP frequency corresponding to that of 1550 nm optical wavelength.

only a short propagation length. In order to compare the LR-SPP propagation characteristics of Au, Cu, and PLD-TiN plasmonic waveguides, we standardized the metal film thicknesses to 40 nm in this work, since the cut-off thickness of TM mode in this I-M-I structure is less than 40 nm. As the thickness of the metal film decreases, the mode penetrates progressively deeper into the top and the bottom dielectric films and less is retained in the metal film [22]. According to our simulation, the propagation constant of the TM mode tends asymptotically towards a transverse electromagnetic (TEM) wave propagating in the top and bottom dielectric films, as the thickness of metal film is less than 40 nm. For a given metal thickness of 40 nm and width of 500 nm, the power confinement factors as shown in Fig. 2 for Au, Cu and PLD-TiN I-M-I plasmonic waveguides increase with the decreasing in the metal or metal-like film thickness. From the contour plots of Fig. 2(a) to (c), the better power confinement factors (red region) are located at metal or metal-like film with thickness in the range of a couple of tens of nanometers, which indicates that much energy is bounded at the interface of metal/dielectric in plasmonic waveguides. Using the film thickness of 40 nm and the SPP frequency corresponding to that at the optical communication transmission wavelength of 1550 nm, we make a comparison of power confinement of LR-SPP among SiO_2/Au/SiO_2, SiO_2/Cu/SiO_2, and SiO_2/PLD-TiN/SiO_2 plasmonic waveguides and obtain the PCFs of 5.10×10^{-2}, 1.03×10^{-2}, and 1.94×10^{-2}, respectively. In summary, SiO_2/PLD-TiN/SiO_2 plasmonic waveguide gives a better power confinement, nearly twice that of SiO_2/Cu/SiO_2 plasmonic waveguide.

Symmetrical I-M-I structures are shown to be more favorable for longer propagation length [27]. We will next give some design considerations of SPP waveguide with regard to LR-SPP propagation characteristics. A comparison of interconnect level performances between electronic and plasmonic wires will be presented.

3.1 Device-Level Performance

Our work is intended to present an optimal design for plasmonic wiring in the BEOL of Si chip with crosstalk constraints. The schematic of electronic/ plasmonic interconnect is shown Fig. 3(a) and (b) where adjacent wires are laid out in the horizontal and vertical directions. For digital signal along x-axis in traditional electronic Cu wires, the crosstalk effect is the result of capacitive coupling, $C_{\text{wire}-\text{wire}}$, between a victim and an adjacent aggressor wire [28]. Similar to crosstalk effect in electronic wires, Fig. 3(c) and (d) show that electromagnetic field coupling is possible between adjacent plasmonic wires, either in-plane or out-of-plane, during data transmission. In plasmonic waveguides shown in Fig. 3(c) and (d), the SPP wave is launched along the x-axis from terminal P_1 to P_3. We expect the square wave signal travelling along the aggressor plasmonic waveguide from P_1 to be received at P_3 without distortion. Sometimes, the electromagnetic field may couple to the victim waveguide, and the SPP mode can be found at terminal P_4. The criterion in determining the separation (gap and isolation) of the plasmonic waveguides is 25% of energy being transferred to the victim waveguide from the aggressor waveguide [28] at the end of a 100 μm line. In the case of

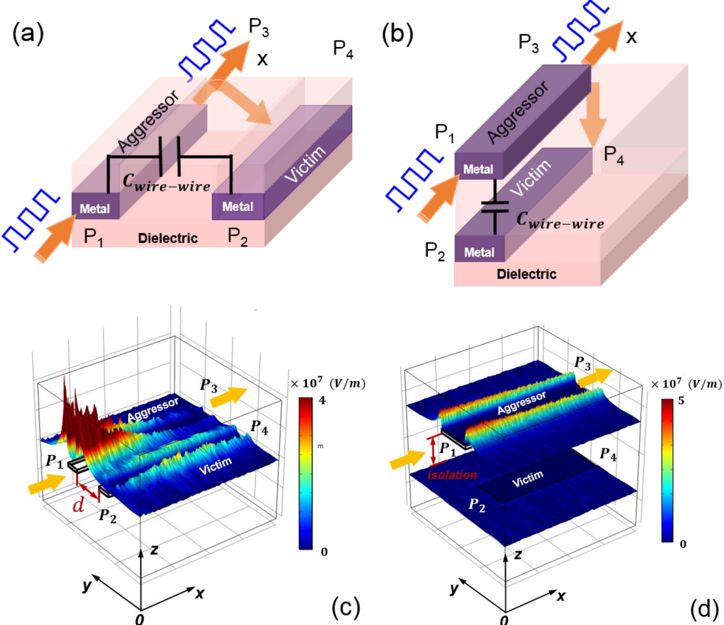

Fig. 3. Electronic Cu wires geometry where a victim wire's potential is changed as a result of capacitive coupling, $C_{\text{wire-wire}}$, to adjacent aggressor wires (a), and capacitive coupling between two metal layers (b). Plasmonic wires geometry where an aggressor wire's electromagnetic field may couple to adjacent victim wire horizontally and vertically in (c) and (d), respectively.

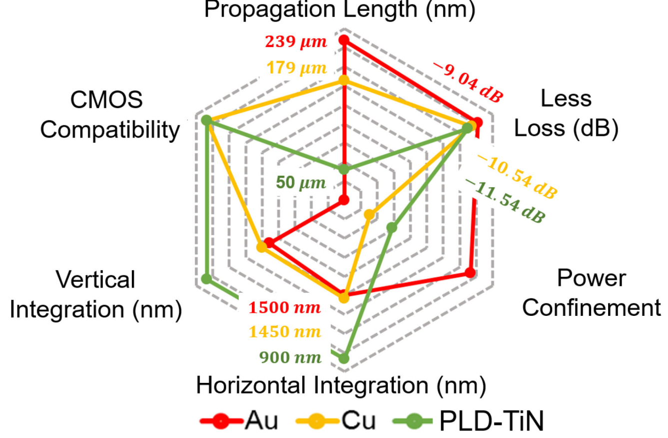

Fig. 4. Figure of merits in Au, Cu and PLD-TiN plasmonic waveguides. Propagation length of plasmonic waveguides: Au 239 μm, Cu 179 μm and PLD-TiN 50 μm. Loss of plasmonic waveguide: Au -9.04 dB, Cu -10.54 dB and PLD-TiN -11.54 dB, and the pitches are 1500 nm, 1450 nm, and 900 nm in Au, Cu, and PLD-TiN waveguide, respectively.

two Au strips of thickness $t = 40$ nm, each of width $w = 500$ nm embedded in SiO_2 dielectric films, the gap (lateral separation) between the two Au strips should be larger than 1000 nm (in Fig. 4(c)), and the isolation (vertical separation) between two metal layers should be larger than 1100 *nm* (in Fig. 4 (d)) to avoid crosstalk effect in plasmonic interconnects.

Based on our numerical crosstalk models, the design rules of plasmonic waveguides are presented in Table 1. Compared to the dimensions of global Cu wires in Intel 10 nm node [3], the thickness (t) of metal of 40 nm in plasmonic waveguide is much smaller than the electronic Cu wire thickness (T) of 6 μm. Based on the criterion of crosstalk between two adjacent plasmonic waveguides, the gaps between Au, Cu and PLD-TiN strips in lateral direction for a waveguide length

Table 1
Design Rules of Plasmonic Waveguides and Traditional Cu Wires with 100 μm Length

Interconnects	Electronic Cu wires	Plasmonic waveguide (λ=1550 nm)		
		Au	Cu	TiN
Gap between lines (25% energy loss)	5.5 μm	1000 nm	950 nm	400 nm
Isolation between lines (25% energy loss)	> 6 μm	1100 nm	1000 nm	600 nm
Metal thickness	6 μm	40 nm	40 nm	40 nm

Gap: lateral separation; isolation: vertical separation

of 100 μm are 1000, 950, 400 nm, and the isolations between two plasmonic waveguides in vertical direction are 1100, 1000, 600 nm, respectively. For larger gap spacing and hence longer coupling length, to save computing resources, the actual length (coupling length) by which 25% of energy in the aggressor line is transferred to the victim line, is calculated based on the effective mode indices calculated for the 100 μm length. The effective mode indices are related to the coupling length by using the equation of $L_{\text{coupling}} = \frac{\pi}{k_0(n_{\text{odd}} - n_{\text{even}})}$ [29], where n_{odd} is the effective refractive index of odd mode and n_{even} is the effective refractive index of even mode.

We benchmarked three different plasmonic interconnects, viz. classical Au waveguide, Cu and PLD-TiN plasmonic waveguide options. We also contrasted their characteristics and given some design guidelines of propagation length, loss [30], power confinement [28] and crosstalk immunity [31] as defined in the references given for each term. As seen in the normalized characteristics constructed in a spider chart Fig. 4, Au plasmonic waveguide has superior propagation length of 239 μm, which is longer than 179 μm of Cu plasmonic waveguide and 50 μm of PLD-TiN waveguide. The plasmonic interconnect is currently limited by the performance of generation and detection of the SPP with transducer coupling efficiencies of the transmitter and of the receiver to a plasmonic waveguide (electron-plasmon coupling efficiency) ~~of~~ to a total of 14% [14]. The total loss of a 100 μm long plasmonic waveguide can be expressed as a sum of propagation loss in the plasmonic waveguide α_{WG}, loss of electron-plasmon conversion in the transmitter α_T, and loss of plasmon-electron conversion in receiver α_R, viz. $\alpha_{tot} = \alpha_{WG} + \alpha_T + \alpha_R$, $\alpha_{WG_Au} = \frac{20}{ln(10)} \times \frac{2\pi}{\lambda} \times Im(n_{eff}) \times 100 = -0.5$ dB, $\alpha_{WG_Cu} = -2$ dB, and $\alpha_{WG_TiN} = -3$ dB, $\alpha_T + \alpha_R = 10 \times \log_{10}(0.14) = -8.54$ dB. Assuming that there is no loss due to coupling to adjacent waveguides, the total loss of these three plasmonic waveguides (α_{tot}) are -9.04 dB, -10.54 dB, and -11.54 dB, respectively. In this figure of merits diagram shown in Fig. 4, we have plotted it such that the larger area of the polygon the better is the performance.

3.2 System-Level Performance

Keeping asynchronous communication in mind, the interconnect level performance inherently relies on the characteristics of propagation speed, energy efficiency, data capacity and safe distance from crosstalk coupling.

In this section, we investigate the performance of electronic and plasmonic technologies with respect to signal latency, energy dissipation per bit, interconnect throughput, and 25% crosstalk coupling length between two adjacent wires. Signal latency is presented in Fig. 5(a), for a conventional electronic Cu wire versus a plasmonic interconnect of Cu for a SPP frequency corresponding to that of an optical wavelength of 1550 nm as the global metal. The signal latency is defined as the time it takes a data packet to travel from the sender block to the receiver block during which time the receiver block is unable to perform any operation. It is strictly determined by series resistance R and the capacitance $C_{\text{wire-wire}}$QQ between wires. Nevertheless, based on surface electromagnetic wave transmission, the latency of plasmonic waveguide is defined as $\frac{L}{v_g}$, where v_g

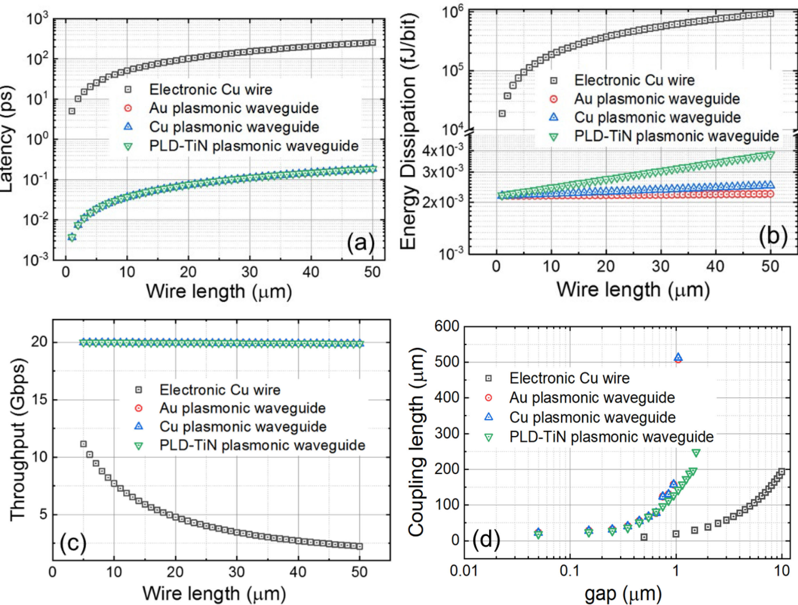

Fig. 5. Comparison of (a) point-to-point signal latency, (b) energy dissipation per computing bit, (c) link throughput with a fixed packet size (64 bits) versus wire length L of 1 $\sim$ 100 μm for electric Cu wire and plasmonic waveguides (Au, Cu and PLD-TiN). (d) coupling length comparison between electric Cu wire and plasmonic waveguides (Au, Cu and PLD-TiN).

is the group velocity ($v_g = \frac{\partial \omega}{\partial k_{spp}}$). Due to the distinct propagation speed of electrons (2.2 $\times$ 10^6 m/s) and surface plasmon ($<$ 2.7 $\times$ 10^8 m/s), the signal latency is only 0.18 ps and 0.19 ps for Cu and PLD-TiN plasmonic waveguide respectively, which is much smaller than that of electronic Cu wires (250 ps). The energy dissipation shown in Fig. 5(b) is directly related to the performance of the chip network. Within chip, it will impact on integration density, temperature budgets, whereas externally, it will influence the overall chip power consumption and battery life.

The energy dissipation per bit for electronic Cu wire as presented in Fig. 5(b) can be calculated on average as $\langle E_{ele} \rangle = \frac{1}{2}\ C_{wire-wire} V_{dd}^2$ [32], where $V_{dd} =$ 1.0 V in current CMOS technology. We compare the energy dissipation directly with shot-noise limited transmission of SPP. For an on-chip interconnect network, a BER for signal transmission on an integrated circuit is taken to be 10^{-15} [33]. We therefore require a mean value <m> = 34 plasmons per bit in a victim waveguide to transmit information with a BER of 10^{-15}. The loss during transmission with an attenuation constant α requires that the average energy dissipation per bit be $\langle E_{spp} \rangle = \frac{1}{2}\hbar\omega \langle m \rangle e^{\alpha \cdot L}$. Shot noise limited detection of an ideal coherent state with a mean value of $\langle m \rangle$ for logical 1 and 0 plasmons for logical 0 results in a BER equal to $\frac{1}{2} e^{(-\langle m \rangle)}$ [28]. With increase in the wire length, the energy consumption of electronic Cu wire increases exponentially, but the power consumption of plasmonic waveguides increases only linearly. Comparing the energy dissipation, we obtain a value of 10^6 fJ/bit energy dissipation at the end of electronic Cu wire of length L = 100 μm, while the much lower power consumption of 2.2 $\times$ 10^{-3} fJ/bit, 2.5 $\times$ 10^{-3} fJ/bit, 3.8 $\times$ 10^{-3} fJ/bit for Au, Cu and PLD-TiN plasmonic waveguides, as seen in Fig. 5(b).

There is another critical metric for evaluating interconnect performance, i.e. throughput of link, which is the capability in terms of the number of bits that can be delivered by the interconnect in a given time period. Usually, the interconnect throughput is defined as follows [32],

$$\text{Throughput} = D / \left(\frac{D}{\text{Capacity}} + \text{Latency} \right) \tag{2}$$

$$\text{Capacity} = 2 \times BW \times log_2^M \tag{3}$$

where D is data packet size, typically 64 bits, *BW* is the bandwidth of interconnects (10^9 Hz for electronic wires and 10^{12} Hz for plasmonic wires). $M = 2$, represents the binary logic computation. The values of latency in different interconnect technologies are shown in Fig. 5(a). With these values the throughput of electronic and plasmonic wires are calculated and the results shown in Fig. 5(c). The throughput of plasmonic wires is maintained 19.8 Gbps without degradation with propagation distance.

In the interconnect hierarchy, the crosstalk is typically quantified by a coupling length for a given gap spacing between the aggressor and victim lines, which is defined in section IV. The voltage transient on a victim wire subject to adjacent aggressor wires in electronic interconnection can be calculated from coupled line theory using distributed RC models [34]. As shown in Fig. 5(d), the coupling length with regards to 25% energy coupled to victim line are 12.5 μm and 155 μm in electronic Cu wires and plasmonic Cu wires, respectively for the wire spacing of 1 μm. The 25% crosstalk coupling length for PLD-TiN plasmonic waveguide is 125 μm. This result reflects the fact that the integration density of global wires can be improved significantly by using plasmonic waveguides for intra-chip communication.

4. Conclusion

An optimized CMOS-compatible dielectric-metal-dielectric (I-M-I) plasmonic waveguides is proposed for intra-chip communication consisting of 40 nm thick Cu or PLD-TiN sandwiched between SiO_2 with lateral line gap of 950 nm and 400 nm, respectively for lines of up to 100 μm long. It is validated that the plasmonic waveguides have many superior features in terms of propagation loss, power confinement, integration density, signal latency, energy efficiency, link throughput and crosstalk immunity, which is promising to replace traditional electronic Cu lines in the global wires. To be fully compatible with Si mass production, Cu and PLD-TiN plasmonic waveguide are considered with Cu achieving a longer propagation length of 179 μm to that of 50 μm for PLD-TiN. To achieve a higher-level of integration, PLD-TiN plasmonic waveguide with much smaller pitches of 900 *nm* than that of 1450 *nm* in Cu plasmonic waveguide. Both Cu and PLD-TiN are the promising candidates in global wires for high performance asynchronous communication, due to their advantages of small signal latency, respectively, of $\sim$0.18 ps and 0.19 ps, energy dissipation per computing bit of $\sim 2.5 \times 10^{-3}$ fJ/bit and 3.8×10^{-3} fJ/bit, wire throughput for both of $\sim$19.8 Gbps, and 25% crosstalk coupling length of 155 μm and 125 μm for 1μm spacing. For the properties presented above, plasmonic waveguides may well serve as an outstanding interconnect between asynchronous blocks on Si chips. By increasing the synergy between different functional blocks, plasmonic interconnect, working at the optical frequency corresponding to the wavelength of 1550 nm, is able to unleash the full potential of nanoscale functionality.

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