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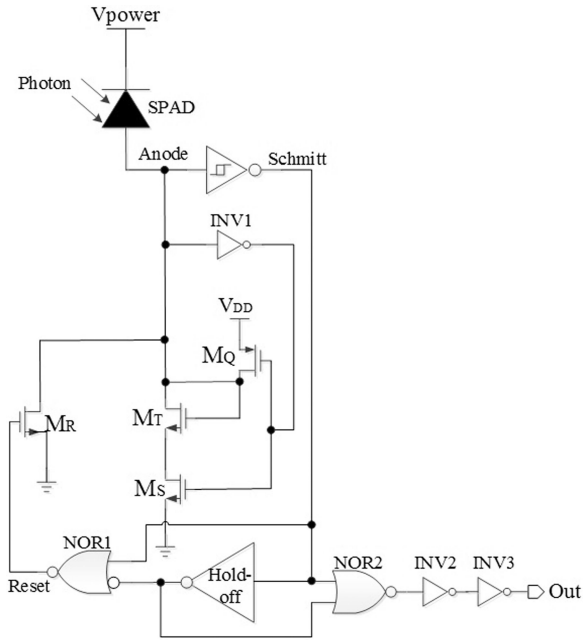

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A Compact High-Speed Active Quenching and Recharging Circuit for SPAD Detectors

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Abstract: A compact high-speed active quenching and recharging circuit (AQRC) is proposed for single-photon avalanche diode (SPAD) detectors fabricated in standard 0.18 μm CMOS technology. A novel sensing and quenching scheme is employed to speed up the process of avalanche detection, enabling a low afterpulsing probability and a high photon-counting rate. The simulation and experimental results indicate that the sensing and quenching time is reduced down to 0.7 ns and the maximum photon-counting rate is close to 200 Mcps (counts per second), meanwhile the afterpulsing probability as low as 0.75% is obtained. Due to the compact configuration, the area occupation of the AQRC is only 306 μm^2. Such outstanding advantages suggest that the proposed AQRC is very suitable for the miniaturized and high-speed SPAD-array detectors.

Index Terms: Single-photon avalanche diode (SPAD), active quenching and recharging circuit (AQRC), photon-counting rate, afterpulsing probability.

1. Introduction

Owing to its prominent advantages of single-photon level sensitivity, picosecond timing resolution, low cost, and low power consumption, single-photon avalanche diode (SPAD) detectors fabricated in the scaled CMOS technologies are increasingly employed in many fields [1]–[4], such as fluorescence lifetime imaging (FLIM), laser imaging detection and ranging (LIDAR), Raman spectroscopy, 3D imaging, and deep learning aided signal detection. In each SPAD detector, a quenching and recharging circuit that is directly connected with the SPAD is necessarily demanded to cut off avalanche current and to reset the device to the excess bias state as fast as possible once an avalanche ignition is sensed. To restrain the afterpulsing effect and enhance the detectable photon-counting rate, it is highly required to reduce the sensing and quenching time, as well as the resetting time. The passive-quenching is a simple solution, which is provided by the voltage drop across a high-value ballast resistor [5], [6], nevertheless, it limits the maximum photon-counting rate and also causes a high afterpulsing probability (AP) because of the very slow quenching and recharging process. In order to overcome these drawbacks, the active-quenching concept is commonly adopted to speed up the quenching of avalanche current [7], [8], which opens a way to the practical application of high-speed SPAD detectors. Various fast active quenching and recharging circuits (AQRCs) have been reported [9], [15]. A dual-threshold quenching and recharge circuit was implemented in [11] with the utilization of an High-voltage (HV) 0.18μm CMOS technology. A very

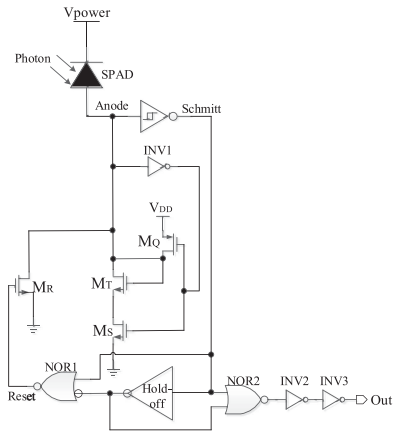


Fig. 1. Proposed active-quenching and recharging circuit.

low AP is obtained with a dead time of 6 n s and a detectable maximum photon-counting rate is up to 66 Mcps (counts per second). Reference [12] proposed a fast mixed passive-active quenching through a prompt positive feedback technique in a 0.35 μm CMOS technology, exhibiting a low AP ($<$1.3%) with 20 ns dead time and a medium maximum counting rate of 50 Mcps. A fast cascoded quenching circuit fabricated in a 0.35-μm CMOS process was presented in [15]. A minimal AP of 0.9% was achieved for 9.5 ns dead time at 6.6 V excess bias. However, some of them acquire the rapid avalanche quenching at the expense of the complex circuit structure and large area occupation, while others cannot achieve the low afterpulsing probability and high photon-counting rate simultaneously though the simple circuit structures are applied.

In this work, a compact AQRC is presented, aiming at lowering the probability of afterpulsing and improving the counting rate of photons by use of a simple circuit configuration. The innovative solution not only minimizes the avalanche sensing and quenching time but also highly enhances the reliability of the quenching and recharging process. The paper is organized as follows. In Section 2, the circuit structure and principle are introduced. The simulation analysis is performed in Section 3. Section 4 gives experimental results and makes discussions. Finally, conclusions are summarized in Section 5.

2. Circuit Design

The complete schematic of the proposed AQRC is shown in Fig. 1, which includes sensing and quenching, recharging, and signal output modules. The sensing and quenching module is a positive feedback loop consisting of three transistors (M_S, M_T, and M_Q) and an inverter (INV1). A Schmitt-trigger, a NOR gate, a hold-off circuit, and a reset transistor M_R form the recharging module. The signal output module is composed of a NOR gate and two inverters (INV2 and INV3).

The operation principle of the AQRC is described as follows and Fig. 2 illustrates the timing diagram of the circuit nodes. In stand-by condition, the anode voltage of the SPAD lowers to the ground and the output of the Schmitt-trigger is at a high voltage, thus the final output is the low level. Once an avalanche is triggered by an incident photon, the avalanche current rises rapidly to its peak. Since the avalanche current quickly flows across a very high resistance provided by the diode-connected M_T and transistor M_S, the anode voltage is swiftly increased and the avalanche is immediately sensed. Soon, the output of the INV1 goes low and the transistor M_S is off, blocking the avalanche path and starting to starve the current. At the same time, the transistor M_Q is switched on and the potential of the anode rises rapidly to supply voltage by a positive feedback loop. As a result, the current drops quickly and the avalanche is quenched in a very short time. It is worth noting that only when the anode voltage goes above the high threshold of the Schmitt-trigger, that

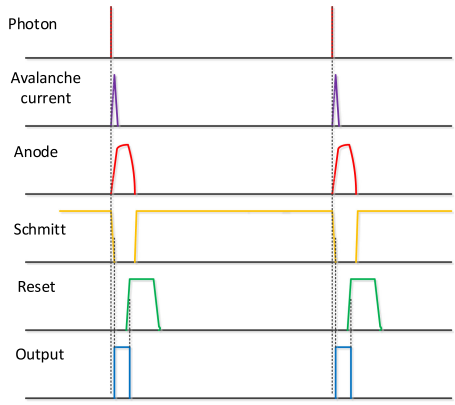


Fig. 2. Timing diagram of the circuit nodes when the avalanche events occur.

is, after the avalanche current has been completely quenched, the Schmitt-trigger begins to flip and then the circuit enters into the recharging stage. After a short delay, the 'Reset' signal is generated, causing the transistor M_R to turn on, accordingly, the circuit is recharged to its initial condition for the next photon detection. The final output is determined by the output of the NOR gate, which is changed synchronously with the Schmitt-trigger and the hold-off circuit. After the output of the NOR is shaped by the two inverters of INV1and INV2, the final output becomes an ideal pulse signal with a steep edge to facilitate further signal processing.

From the above analysis, it can be seen that the proposed AQRC has the following advantages: the avalanche current can be sensed and quenched quickly by the positive feedback loop, greatly reducing the afterpulsing probability, and further improving the photon-counting rate by setting low hold-off time. In addition, the adoption of Schmitt-trigger can ensure that the recharge operation will begin only after the avalanche has been completely quenched, which helps to enhance the reliability of quenching behavior. Besides, the simple circuit configuration makes it very compact and miniaturized, which is fit for the large-scale array integration.

3. Simulation Results

The proposed AQRC was implemented in SMIC standard 0.18-μm CMOS technology. Transistors M_S and M_T are designed with minimum-size ($W = 2W_{min}$, $L = L_{min}$) to reduce loading capacitance. They can maintain a quiescence on-resistance of about 25 MΩ and provide an effective initial passive quenching. Affected by the parasitic capacitance of SPAD devices, the reset transistor M_R is devised with a relatively larger size ($W = 20 \cdot W_{min}$, $L = L_{min}$) for rapid and reliable reset operation although it will increase the area occupation. If a small reset transistor is adopted, it cannot ensure the SPAD device is reliably recharged to the excess voltage state. The hold-off circuit is composed of five inverters in series to effectively suppress the afterpulsing effect. The presented AQRC was simulated in the Cadence environment using the BSIM3v3 models for the MOS transistors. A Verilog-A SPAD model has been developed to accurately simulate various behaviors of SPAD devices such as avalanche ignition, dark counts, afterpulsing, and parasitic capacitance effect [16], [17]. For a SPAD device with 10-μm active diameter, the used basic model parameters are given as follows. As the avalanche current reaches a latch current value (about 100 μA), the corresponding reverse bias voltage is obtained as the breakdown voltage. Subsequently, the avalanche current is linearly increased with the bias voltage, the reciprocal of the slope of the reverse *I-V* curve is extracted as the breakdown series resistance. From the tested reverse *I-V* curve of the SPAD, the extracted breakdown voltage (V_{break}) and the breakdown series resistance (R_{break}) are 15.5 V and 3.07k Ω, respectively. Additionally, through the theoretical calculations using the actual doping profile and device size, the anode and cathode constant stray capacitances C_{as} and C_{cs} of both

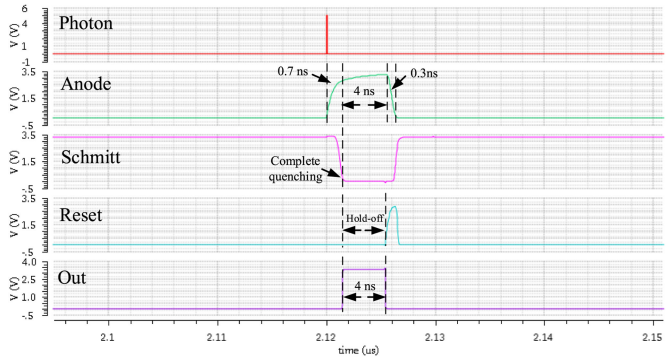
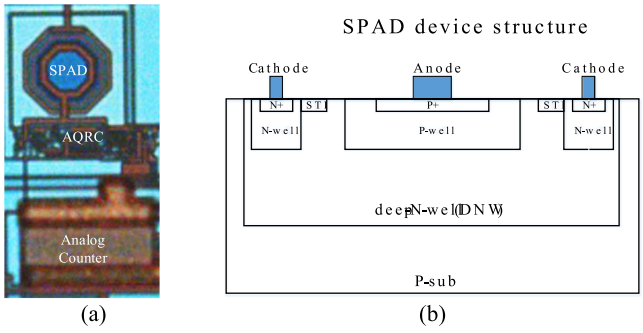


Fig. 3. Simulated waveforms of circuit nodes.



(a) (b)

Fig. 4. (a) Die micrograph of the SPAD pixel with the proposed AQRC and (b) the cross-section of the presented SPAD structure.

about 0.783 pF, and the zero-bias depletion region capacitance C_{j0} of about 1.31 $\times$ 10^{-8} F/cm^2 were obtained.

Fig. 3 depicts the waveforms of the Anode, Schmitt, Reset, and Out nodes through post-layout simulation considering the parasitic effect of the layout. It is seen that when an incident photon excites an avalanche event, the anode voltage is immediately charged by avalanche current. Shortly, the active quenching is triggered and the increase of the anode voltage is accelerated. After a short time, the active quenching process ends and the anode voltage no longer increases. Apparently, the avalanche is quickly sensed and quenched in a very short time of 0.7 ns at the excess bias voltage (V_{EX}) of 3.5 V. Also, it is noted that the Schmitt-trigger flips and starts the recharging operation only after the avalanche is completely quenched. After the hold-off time of about 4 ns, the 'Reset' signal is produced so that the anode voltage of SPAD is grounded, as a result, the circuit goes back to its initial state. As seen in Fig. 3, the reset time of the AQRC is about 0.3 ns. Finally, we can distinctly observe that the output avalanche pulse becomes a perfect pulse signal with a very steep edge. The proposed AQRC exhibits an overall dead time of about 5 ns, thus a maximum photon-counting rate close to 200 Mcps (counts per second) is expected.

4. Experimental and Discussion

The AQRC was fabricated in SMIC standard 0.18-μm CMOS technology. Fig. 4(a) illustrates the die micrograph of a pixel that includes a SPAD device, an AQRC, and an analog counter. Fig. 4(b) shows the cross-section of the presented SPAD with a P-well/ deep N-well (DNW) structure. The whole SPAD active device is located within a DNW. The avalanche region is formed by the PN junction between the P-well and the DNW. Lack of P-well guard ring bordering the device active

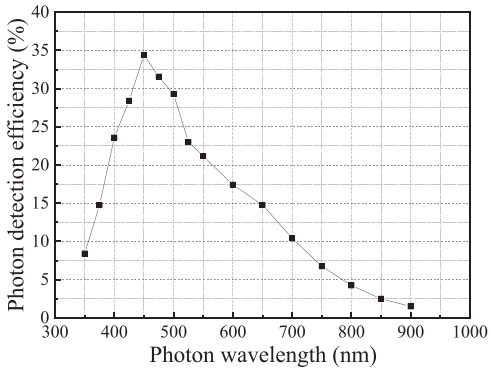


Fig. 5. Tested PDE of the SPAD device versus the photon wavelength at VEX = 3.5 V.

area, a "virtual" guard ring is formed by the DNW with the retrograde doping profile. The overall area occupation of the single-pixel (SPAD and front-end circuit) is about 1600 μm^2, where the AQRC occupies an area of 34 μm $\times$ 9 μm and the SPAD device has an active area diameter of 10 μm, yielding a high fill-factor of nearly 21%. After that, the AQRC integrated with a SPAD device was bonded and mounted on a printed circuit board (PCB). To observe transient avalanche pulses, the AQRC is connected with the high-speed probe of a Tektronix MDO 3104 oscilloscope through the SMA socket on the PCB.

Firstly, the reverse *I-V* characteristic of the SPAD device was tested. The tested breakdown voltage is about 15.5 V for the P-well / DNW structure in 0.18-μm standard CMOS technology. Subsequently, the photon detection efficiency (PDE) of the SPAD device versus different photon wavelengths was measured at the excess bias voltage of 3.5 V, as shown in Fig. 5. In the photon wavelength range from 350 nm to 900 nm, the PDE rises rapidly as the wavelength increases, then drops. The peak PDE is about 34% at 450 nm and 2.5% at 850 nm.

In order to enhance the circuit driving capacity for the performance measurements, the AQRC is followed by an on-chip output buffer supplied with 1.8 V. The measured output waveform of the AQRC at $V_{EX} = 3.5$ V is shown in Fig. 6(a). Due to the influence of the load capacitances from the oscilloscope probe and the circuit PAD, the rising edge and falling delay time of the output avalanche pulse is greatly enlarged. To evaluate the time-dependent performance of the AQRC, the load capacitance of about 15 pF is considered in the circuit simulation and the simulated transient waveform is illustrated in Fig. 6(b). By comparison, the simulated avalanche pulse waveform is completely consistent with the test waveform, including rising and falling time, which validates the correctness and reliability of the circuit performance. Fig. 6(c) illustrates multiple consecutive avalanche pulses by illumining the SPAD with a pulsed light source. It is clearly found that the minimum interval between two consecutive pulses approaches zero nanoseconds. Fig. 6(d) further depicts the simulated avalanche output waveforms working at the maximum count rate without an on-chip output buffer. It can be seen that the maximum count rate can approach 200 Mcps for the SPAD pixel when there is no influence of the large load capacitances.

The DCR at different excess biases was measured by counting the avalanche pulses over a certain time window. At the excess bias of 3.5 V, the DCR value is about 6.9 kHz at room temperature. Further, we tested the afterpulsing suppression ability of the AQRC. The AP value is evaluated by means of an inter-avalanche time histogram method [18]. Since the obtained histogram of the experimental noise distribution shows an exponential curve behavior, the AP for a specific dead-time value can be extracted using the area between the experimental and its fitting curves, divided by the area under the experimental curve. Fig. 7 depicts the extracted AP values as a function of excess voltage for different hold-off time values. It is seen that the AP is increased with the excess voltage for a given hold-off time, which is due to the higher avalanche trigger probability of SPAD devices at higher excess bias. It is also found that the AP values are significantly increased

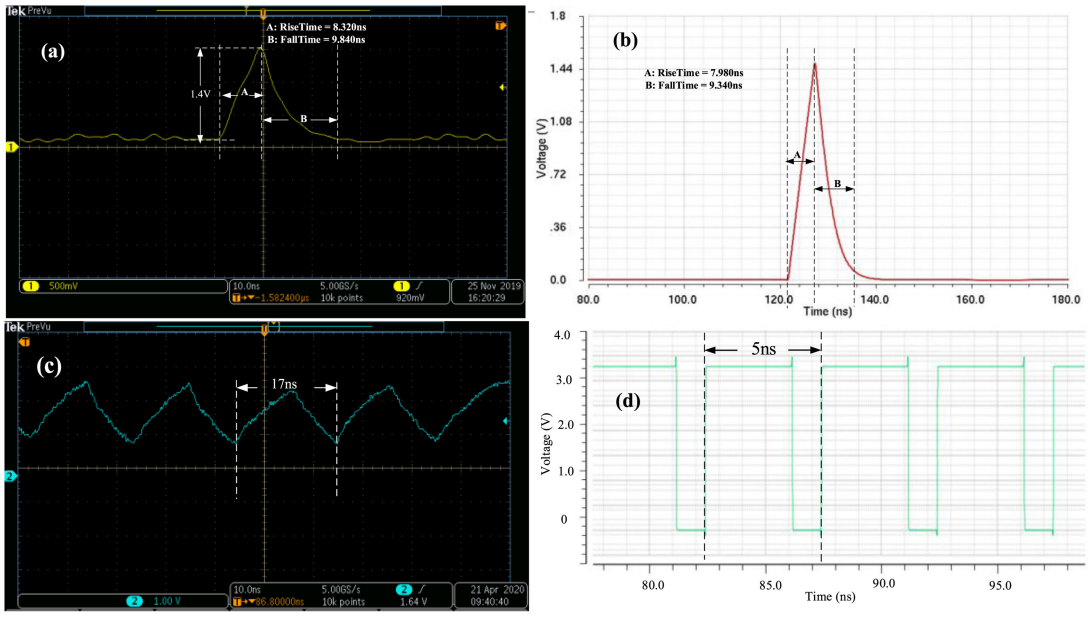


Fig. 6. Transient output avalanche pulse of the proposed AQRC. (a) Tested and (b) simulated single avalanche waveforms; (c) tested multiple consecutive avalanche output waveforms; (d) simulated avalanche output waveforms at maximum count rate without on-chip output buffer.

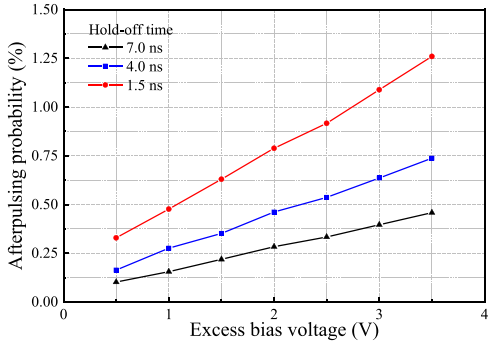


Fig. 7. Extracted AP as a function of excess bias voltage for different hold-off times at room temperature.

with the decrease of the hold-off time of the AQRC. At $V_{EX} = 3.5$ V, the AP values are only 1.25%, 0.75%, and 0.45% for three different hold-off times of 1.5 ns, 4.0 ns, and 7.0 ns, respectively, which are significantly lower than the ones reported in the published literature [12], [15], [19]. It is experimentally proved that the proposed AQRC has a strong ability to suppress afterpulsing effect, even if the applied hold-off time is very short.

Table 1 compares the performance of the proposed AQRC with the reported ones fabricated in various CMOS technologies [10]–[12], [15], [18]–[20]. In these reported state-of-the art AQRCs, the quenching mechanism based on a positive feedback loop is generally adopted to reduce the quenching time. In our work, a similar positive feedback quenching mechanism is applied. The proposed AQRC realizes very short sensing and quenching time, greatly reducing the trapped probability of avalanche charge and thus effectively suppressing the afterpulsing effect. Importantly, the adoption of the Schmitt-trigger ensures that only after the avalanche current is completely quenched the final output signal is generated, thereby improving the reliability and stability of

TABLE 1
Summary of Performance Comparison Between the Proposed AQRC and the Reported Ones in the Literature

work	CMOS Tech. node (µm)	SPAD Diameter (µm)	Quenching Time (ns)	Hold-off (ns)	V_{EX} (V)	AP (%)	DCR (CPS)	Counting rate (Mcps)	Circuit Area (μm^2)
[10]	2	10	-	3-16	5	-	-	250	-
[11]	0.18	8	-	6	3.5	-	180	66	60
[12]	0.35	20	1	20	6	1.3	4.9 k	50	672
[15]	0.35	80	0.48	9.5	6.6	4.8	30.8 k	50	5026
[18]	0.18	12	-	3.3-30	1	-	26 k	-	264
[19]	HV 0.18	50	-	<6.2	5	5	-	160	32760
[20]	HV 0.18	80	-	<12.5	5	-	-	80	-
Our work	0.18	10	<0.7	4	3.5	0.75	6.9 k	200	306

the output avalanche pulse. Furthermore, the very fast quenching and resetting behaviors are implemented by a simple circuit structure, a low area occupation of about 306 μm^2 is obtained, which is much smaller than the reported high-speed AQRCs [15], [19]. In a combination with the use of the compact analog counter, the fill-factor of the presented SPAD pixel is up to 21.6%. It is obvious that the presented circuit achieves the fast quenching speed, low AP, high photon-counting rate, and low area occupation at the same time. Thanks to its excellent performance and small size, the presented AQRC is very suitable for the integration within a CMOS smart pixel for photon-counting, photon-timing, and 3D imaging applications.

5. Conclusion

An ultrafast active quenching and recharging circuit is presented for driving a SPAD detector. The compact circuit employs a positive feedback loop to quickly break the avalanche current, leading to a significant reduction of afterpulsing probability. Meanwhile, the Schmitt-trigger is used to improve the reliability of the quenching and recharging process. The AQRC integrated with a SPAD device was fabricated in 0.18-μm standard CMOS technology. After the AQRC was bonded and mounted on a PCB, the functionality of the AQRC was characterized. Also, the circuit simulation was performed to validate the AQRC performance using a SPAD Verilog-A model. The simulation and experimental results reveal that the presented AQRC can achieve a very short quenching time of fewer than 0.7 ns, a high maximum counting rate close to 200 Mcps, and a low AP of 0.75% for 4 ns hold-off time, whereas, it only occupies a small area of 306 μm^2. The work provides a promising solution to acquire a high-speed and compact active-quenching circuit integrated into the SPAD pixel based on standard CMOS technology.

Acknowledgments

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