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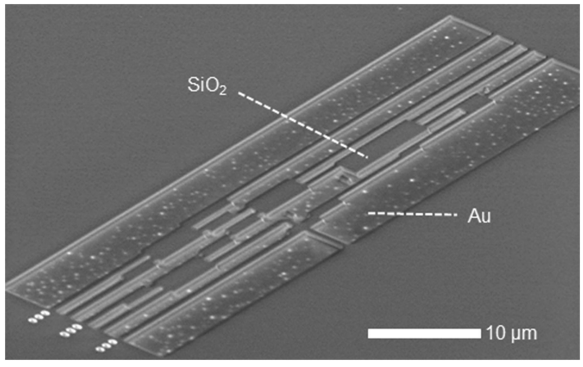

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Feasibility of Cascadable Plasmonic Full Adder

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Abstract: The concept and configuration of a plasmonic cascadable full adder are proposed, whose logic operation is carried out by interference of surface plasmons and whose circuits are formed only with single- and multiple-mode plasmonic waveguides. This full adder is fabricated by patterning a SiO_2 film deposited on a metal film using complementary metal-oxide-semiconductor-compatible processes except for the material of metal. The redundant surface plasmons present after interference are drained from the waveguides by forming radiation ports, and metal bumps are formed in the circuits to prevent stray light recoupling with the waveguides. The logic operation of the circuits is numerically confirmed by the three-dimensional finite-difference time domain method, and the difference in surface plasmon intensity between logic level "0" and "1" is numerically estimated to be 1.5 dB even for the worst case. These simulations were experimentally confirmed for some input signal patterns using scanning near-field microscopy, and the surface plasmon intensity distributions monitored coincide well with those simulated.

Index Terms: Surface plasmon polariton, logic circuit, plasmonic waveguide, full adder.

1. Introduction

Modern social evolution is incredibly rapid, and an enormous amount of information is transmitted and processed every day worldwide. Further, high-performance computational simulations are now indispensable in various fields such as medical science, meteorology, and disaster prevention. The hardware performance necessary to process such massive amounts of information, however, is gradually trailing the required speed evolution. This performance saturation mainly originates from the information processing speed of silicon integrated circuits (ICs), and various trials have been carried out to enhance their operating speeds and increased amounts of information. Optical computing is a solution for the need for enhanced information processing speed. For this purpose, optical and plasmonic logic circuits have been developed and some half or full adders have been numerically or experimentally proposed, whose structures were composed of semiconductor optical amplifiers, Mach-Zehnder interferometers, or resonators [1]–[12]. For optical logic circuits, operation at light speed without nonlinear effects and simple structure without complex components are desirable to solve the performance saturation.

From the viewpoint of operation speed and constructed circuit size, plasmonic logic circuits are an attractive candidate. Surface plasmon polaritons (SPPs) include electromagnetic waves that

propagate along a conductor surface at the speed of light and collective oscillations of electrons coupled with the optical field at the nanoscale beyond the diffraction limit of propagating lightwaves. This attribute of SPPs enables plasmonic circuits to be constructed within the nano/microscale regions, and thus narrower than those of propagating lightwave circuits. To construct plasmonic circuits, numerous plasmonic waveguides have been developed and reported, such as slot waveguides [13], [14], index waveguides [15]–[18], grooved waveguides [19], [20], and hybrid waveguides [21], [22]. Among them, waveguides consisting of a dielectric stripe deposited on a metal film are technically simple (design and fabrication) and easy to translate to waveguide devices and to integrate with silicon ICs. Therefore, we have developed plasmonic components and circuits using waveguides consisting of a SiO_2 stripe on a metal film [23].

Plasmonic circuits generally exhibit heavy losses. However, plasmonic circuits formed with the waveguides consisting of a SiO_2 stripe on a metal film, which is in the range of less than a few hundred micrometers, exhibit relatively low loss when compared with electric circuits [23]. It is, therefore, feasible that plasmonic logic circuits can operate with relatively low loss at light speed if they can be fabricated within the range. This paper proposes and discusses one such plasmonic logic circuit for plasmonic circuits integrated with silicon ICs.

The concept and configuration of the full adder is discussed in Section 2. The design, fabrication, and evaluation are discussed in Sections 3 and 4, respectively. The results obtained are summarized in Section 5.

2. Basic Design of Plasmonic Full Adder

Some of the authors have previously developed a half adder comprising single-mode and multimode waveguides fabricated simply by patterning a SiO_2 film deposited on a metal film [24]. The logic operation in this half adder was carried out by converting the phase difference of the coherent input signals to the spatial intensity distribution using interference. This design and fabrication process of the half adder were extended herein to those of a full adder, which operated as a Boolean logic circuit. Novel concepts were introduced to the full adder in addition to the operations of the half adder, including the following: 1) the carry-out signal phase synchronously coincided with those of all input signals to ensure cascade connection (i.e., the difference in path length between an output port of the carry-out signal and all input ports was an integral multiple of the SPP wavelength); 2) the output signals other than carry-out signals on the first- and second-digit were not required to coincide with each other because these were connected to electronic circuits; and 3) a few waveguide components were newly developed to construct the circuit.

In micro/nanoscale waveguides shorter than or comparable to the wavelength of a lightwave propagating in free space, the phase of the wave can be precisely controlled by the shape and length of the waveguide using recent fabrication techniques. This enables the spatial intensity distribution of SPPs to be precisely controlled in waveguides. Phase control is possible only in the waveguides, and SPPs originating from one source must be used to maintain a constant frequency and to count the phase. In addition, redundant SPPs after interference have to be drained from the waveguides to obtain a clear intensity distribution that corresponds to Boolean logic, otherwise the interference pattern will correspond little to the correct pattern in the waveguides. For example, for two SPPs mixed with an antiphase in a waveguide, the SPPs change from the propagation mode into the radiation mode, though a portion of them stay in the waveguide without radiation. Some radiation ports for these redundant SPPs are therefore needed to eliminate them. In addition, propagating light (i.e., SPPs radiated from waveguides) must be suppressed from coupling with the waveguides again, wherefore metal bumps were introduced into the circuits. A conceptual schematic of the top and the cross-sectional views of the developed waveguide are shown in Fig. 1. These circuits can be simultaneously fabricated using a complementary metal-oxide-semiconductor (CMOS)-compatible process. The SPPs were excited at an incident grating and then divided into several waveguides, whereupon the propagating SPPs were individually modulated in each waveguide and introduced to the logic circuits. For modulation, a few modulators are applicable to generate plasmonic signals [25], [26].

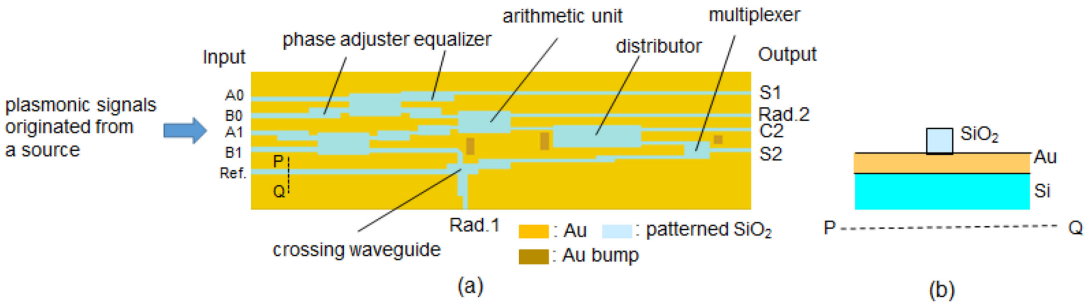

Fig. 1. (a) A conceptual schematic of top view of full adder and (b) the cross-sectional view of waveguide along the P – Q dashed line in (a).

3. Configuration of Plasmonic Full Adder

3.1 Logic Circuit

The full-adder circuit takes two binary numbers and adds the numbers on the same digit excepting the least significant digit, and then outputs the operation results including the carry-out from the lower digit. To obtain this performance, the full adder was designed to comprise five input ports, three output ports, two types of phase adjusters, an arithmetic unit, a distributor, an equalizer, a multiplexer, and three types of single-mode waveguides, as shown in Fig. 1. The five input ports include the two binary inputs of the first digit (A0 and B0); those of the second digit (A1 and B1); and an input from which SPPs are continuously inputted to induce interference (Ref.). The three output ports include the first digit output (S1), the second digit output (S2), and the carry-out (C2), which were set in the circuit. The C2 port was the output port of the carry-out signal whose phase was designed to be constantly equal to that of input signals. The emission ports Rad.1 and Rad.2 were for emission of redundant SPPs after interference of the plasmonic signals. The circuit was formed by combining single- and multimode waveguides (dielectric-loaded surface plasmon (DLSP) waveguide). Here, the multimode waveguides acted as multimode interferometers (MMIs) [27] and played the roles of phase adjuster, arithmetic unit, distributor, equalizer, and multiplexer. The phase change caused by inserting the MMI into a single-mode waveguide (i.e., phase difference between MMI and single-mode waveguide after propagating by the same length) was taken into consideration to exactly configure the phase of the C2 output port (hereafter, equivalent phase change of component). The multimode waveguide was also used to shift the intensity distribution to suppress cross-talk at the crossing single-mode waveguides [28]. In this study, the structure in Fig. 1 was formed using these components (waveguides), and fabricated by patterning a SiO_2 film deposited on an Au layer. Therefore, only the widths were different.

The logic formula for each output was set as follows:

$$S1 = A0 - B0, \tag{1.1}$$

$$S2 = 2 * A1 + 2 * B1 + A0 + B0 - 2.5 * Ref., \tag{1.2}$$

$$C2 = 2 * A1 + 2 * B1 + A0 + B0. \tag{1.3}$$

The table of working principle of the full adder is shown in Table 1. Every formula was formed by interference of SPPs in the circuit. The phases of all input signal coincided each other at the input ports and were synchronized with that of C2 at the output port. The phase of each signal was adjusted to 0 or 180 deg with the phase adjuster, and the phases at 0 and 180 deg were set to plus and minus, respectively. In Table 1, the defined intensities at the phase of 180 deg are indicated with "–" and blue lettering. For output port S2, the output levels were categorized into three levels: the logic level "0" represented by $(-1.5)^2$ – $(+2.5)^2$; and the level "1" represented by $<(\pm 0.5)^2$ and $>(+3.5)^2$. This was permissible because S2 was the only output to the electronic circuit and thus did not influence the carry-out signal of C2. These components and the logic circuit were designed

TABLE 1
Table of the Working Principle of the Full Adder

Input					C2		S2		S1	
B1	A1	B0	A0	Ref.	logic level	defined intensity	logic level	defined intensity	logic level	defined intensity
0	0	0	0	1	0	$(0)^2$	0	$(-2.5)^2$	0	$(0)^2$
0	0	0	1	1	0	$(1)^2$	0	$(-1.5)^2$	1	$(1)^2$
0	0	1	0	1	0	$(1)^2$	0	$(-1.5)^2$	1	$(-1)^2$
0	0	1	1	1	0	$(2)^2$	1	$(-0.5)^2$	0	$(0)^2$
0	1	0	0	1	0	$(2)^2$	1	$(-0.5)^2$	0	$(0)^2$
0	1	0	1	1	0	$(3)^2$	1	$(0.5)^2$	1	$(1)^2$
0	1	1	0	1	0	$(3)^2$	1	$(0.5)^2$	1	$(-1)^2$
0	1	1	1	1	1	$(4)^2$	0	$(1.5)^2$	0	$(0)^2$
1	0	0	0	1	0	$(2)^2$	1	$(-0.5)^2$	0	$(0)^2$
1	0	0	1	1	0	$(3)^2$	1	$(0.5)^2$	1	$(1)^2$
1	0	1	0	1	0	$(3)^2$	1	$(0.5)^2$	1	$(-1)^2$
1	0	1	1	1	1	$(4)^2$	0	$(1.5)^2$	0	$(0)^2$
1	1	0	0	1	1	$(4)^2$	0	$(1.5)^2$	0	$(0)^2$
1	1	0	1	1	1	$(5)^2$	0	$(2.5)^2$	1	$(1)^2$
1	1	1	0	1	1	$(5)^2$	0	$(2.5)^2$	1	$(-1)^2$
1	1	1	1	1	1	$(6)^2$	1	$(3.5)^2$	0	$(0)^2$

via the three-dimensional finite-difference time-domain (3D-FDTD) method using electromagnetic wave analysis software (Pointing for Optics, Fujitsu). The grid size for the design and simulation of the full adder was set at 50 nm and a perfectly matched layer (PML) was used as the boundary conditions to suppress the reflection from the surroundings of the calculation area. For each of the components described in Section 3.2, a grid size of 20 nm or lower was often used for their exact designs and performance simulations.

3.2 Plasmonic Components

The design of the components required to construct the logic circuit employed the following procedure: 1) the effective refractive indexes in the thickness direction were calculated by solving the characteristic equation of the DLSP waveguide; and 2) the frequently-used dispersion relation (Eq. (2)) was obtained for the plasmonic waveguides by substituting the effective refractive index into the characteristic equation obtained by the effective index method, such that

$$\beta_n \sim n_r k_0 - (\nu + 1)\pi\lambda_0/4n_r W_e^2, \tag{2}$$

where β_ν is the propagation constant; n_r is the equivalent refractive index of the SiO_2 mesa-stripe waveguide; k_0 is the wave number in free space; ν is the mode number; λ_0 is the light wavelength in free space; and W_e is the effective waveguide width. Here, the wavelength of incident light for SPP excitation was set at 1310 nm, and the refractive indices were set at $0.4496 + i8.2907$ for Au and 1.4468 for SiO_2, respectively. The thickness of the SiO_2 film was set at 500 nm so that only a single mode existed in the direction of the thickness for all components.

3.2.1 Single-Mode Waveguide: Three types of DLSP waveguides with the various widths of 300, 400, and 600 nm were used to form the circuit. The 600 nm-wide waveguide was mainly used to stably transmit plasmonic signals with a single mode. The waveguides with 300- and 400-nm widths were used as short-range connections between MMIs to quickly eliminate the influence of higher-order modes introduced to the single-mode waveguide from the MMI output port. This is because the higher-order modes propagate along a single-mode waveguide for some length owing to Fresnel reflections within the waveguide.

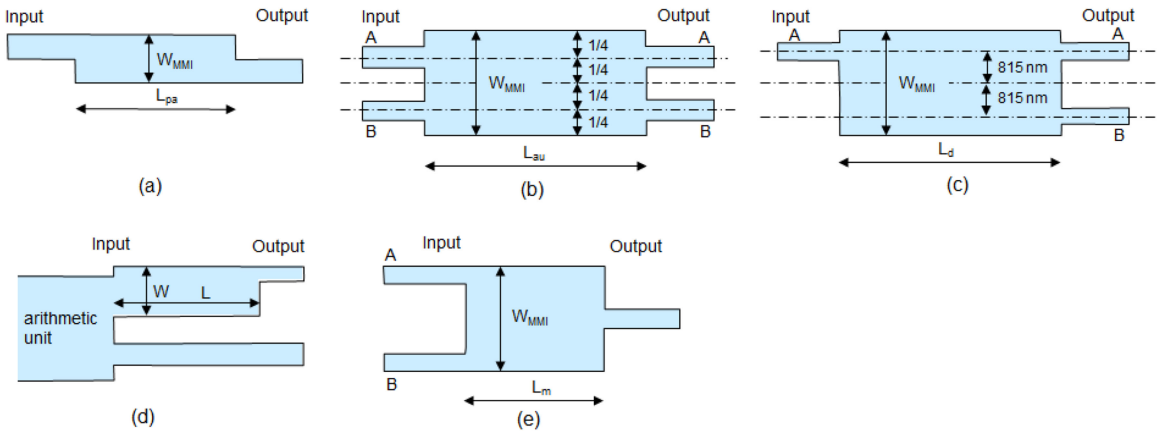

Fig. 2. Plasmonic components developed to construct full adder. (a) phase adjuster, (b) arithmetic unit, (c) divider, (d) equalizer, and (e) multiplexer.

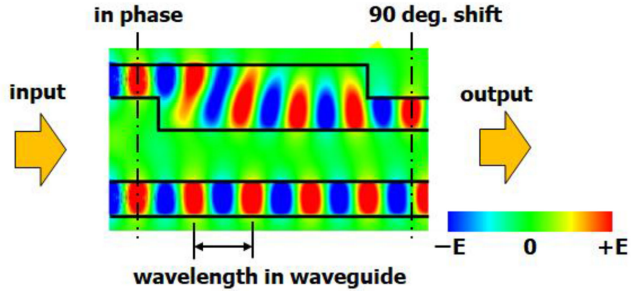

Fig. 3. Electric field distribution in the designed plasmonic phase adjuster (90 deg shift) and a single-mode waveguide.

3.2.2 Phase Adjuster (1 × 1 MMI): This component was comprised of an MMI that included the 0th- and 1st-order modes and an input and an output single-mode waveguide (Fig. 2(a)). The phase of the input signal could be adjusted to an arbitrary phase at the distance where the 0th- and 1st-order mode interfered each other with an antiphase by controlling the MMI size [24]. The size was designed using the equation for the MMI [24], [27], given as

$$L_{pa}(W_{MMI}) = \pi/[\beta_0(W_{MMI}) - \beta_1(W_{MMI})], \tag{3}$$

where W_{MMI} is the MMI width; and L_{pa} is the length generating the mirror image of 0th- and 1st-order modes; and $\beta_0(W_{MMI})$ and $\beta_1(W_{MMI})$ are the propagation constants of 0th- and 1st-order modes, respectively. Two types of phase adjusters were employed in the circuit; namely, a phase adjuster 800 nm (width) × 2220 nm (length) generating a 75 deg phase shift to the output of 400 nm-wide single-mode waveguide (equivalent phase change of component: 113 deg) and a phase adjuster 1200 nm (width) × 3710 nm (length) generating a 90 deg phase shift to the output of 600 nm-wide single-mode waveguide (equivalent phase change of component: 2 deg). For the 90-deg phase adjuster, the electric field distribution is shown in Fig. 3 in comparison to the case of a single-mode waveguide. The single mode in the input waveguide was changed to the multimode in the MMI and was then returned to the single mode in the output waveguide with a phase difference of 90 deg.

3.2.3 Arithmetic Unit (2 × 2 MMI): This component was comprised of an MMI including from 0th- to 3rd-order mode and two input and two output single-mode waveguides (Fig. 2(b)) [24]. Two input ports were set at the distance of 1/4 of the width of unit on the both side from the center. Two

input signals were outputted with the phase difference of ±90 deg and interfered with the phase difference of 0 or 180 deg by combining with the phase adjuster and then outputted. The size was designed using the equation for the MMI,

$$L_{au}(W_{MMI}) = (1/4)\,LCM\{2\pi/[\beta_0(W_{MMI}) - \beta_m(W_{MMI})]\}, \tag{4}$$

where L_{au} is the shortest length generating self-imaging for all modes; $\beta_m(W_{MMI})$ is the propagation constant of the mth-order mode; and LCM is the function calculating the least common multiple. The size of this unit was designed to 2630 nm (width) × 6060 nm (length), and the phase of the output signal was designed to 90 deg between the input port A (B) and output port A (B). The equivalent phase change of component was 215 deg between the input port A (B) and the output port A (B) and 305 deg between the input port A (B) and the output port B (A).

3.2.4 Distributor (1 × 2 MMI): This was comprised of a MMI including from 0th- to 3rd-order mode and an input and two output single-mode waveguides. The signals inputted were divided into two output ports including from 0th- to 3rd-order mode (Fig. 2(c)). The size was designed using the following equation,

$$L_d(W_{MMI}) = (3/4)\,LCM\{2\pi/[\beta_0(W_{MMI}) - \beta_m(W_{MMI})]\}, \tag{5}$$

where L_d is the shortest length generating the self-imaging for all modes. An input port was set at the distance of 815 nm from the center to excite the 3rd-order mode. The size of this unit was designed to 2630 nm (width) × 10280 nm (length), in which length the interfered modes were clear and eliminated the influence of Fresnel reflections. The equivalent phase change of the component was 100 deg between the input port and the output port A and 305 deg between the input port and the output port B.

3.2.5 Equalizer (1 × 1 MMI): Through the equalizer, the intensities of two plasmonic signals outputted from an arithmetic unit were equalized. The design of the equalizer was similar to that of phase adjuster. The size of the unit was designed as 1200 nm (width) × 6200 nm (length) (Fig. 2(d)). The equalizer performance was obtained by changing its attachment position to the arithmetic unit (2 × 2 MMI) so that the intensity of the output signal S1 (i.e., a 400 nm-wide single-mode waveguide) was controlled such that the difference in output intensity from the two ports was equalized to 0.3 dB from 3.6 dB and the on/off signal ratio was maximized to 5 dB. The phase was not designed because the output of the equalizer was connected to the output port S1 and outputted to an electronic circuit.

3.2.6 Multiplexer (2 × 1 MMI): The multiplexer comprised an MMI including the 0th- to 3rd-order modes, and the two plasmonic signals inputted from the different ports were outputted to the same port. The modes excited in the MMI were mainly 0th- and 2nd-order modes, and the size was designed using the equation for the MMI, given as

$$L_m(W_{MMI}) = \pi/[\beta_0(W_{MMI}) - \beta_2(W_{MMI})]. \tag{6}$$

The size of this unit was designed to 2000 nm (width) × 3000 nm (length) (Fig. 2(e)). The phase was not designed because the output of this unit was connected to the output port S2 and outputted to an electronic circuit.

3.2.7 Radiation Port of Redundant SPPs: This component, which has already been reported in [24], eliminated the redundant SPPs through crossing waveguides [28] from the circuit of the full adder. Therefore, this is a key component for suppressing the noise caused by the interference between the redundant SPPs and the signal SPPs.

3.2.8 Metal Bump: A portion of the SPPs, including redundant ones, were emitted from the waveguides. If this propagating lightwave coupled again with the waveguides, it would interfere with the intensity distribution of SPPs and result in noise. To suppress this coupling, wedge-type Au bumps were set at the points where 3D-FDTD simulations indicated that the intensity of the emission was high. These bumps reflected the emitted light to the upper directions of the circuits.

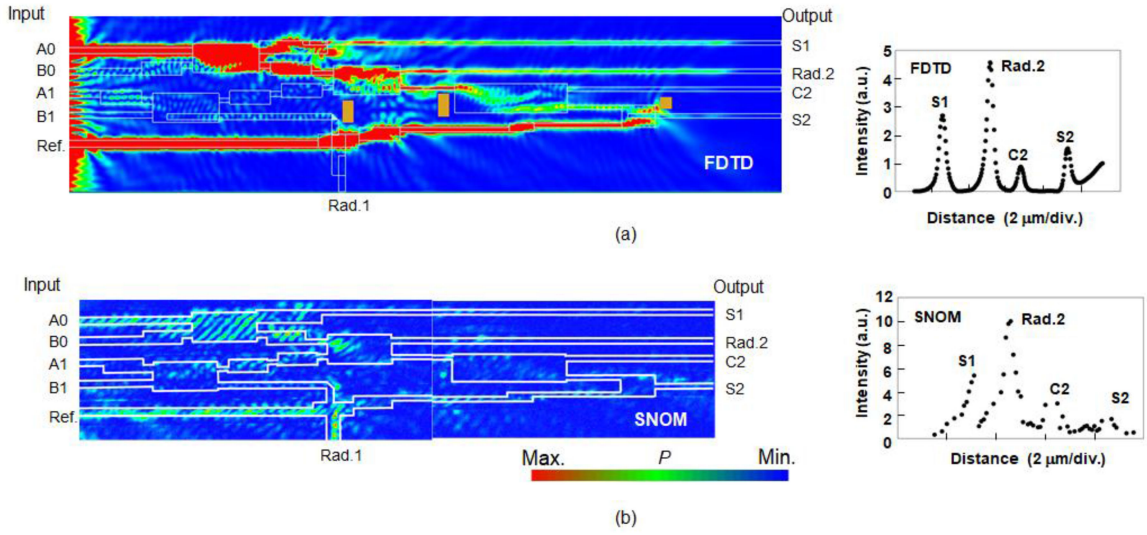

Fig. 4. Intensity distribution of plasmonic signals and output intensity pattern under input signal pattern (B1 A1 B0 A0) = (0001). (a) simulated with FDTD method and (b) monitored with SNOM.

4. Fabrication and Evaluation of Plasmonic Full Adder

4.1 Design and Simulation of Circuit Performances

The performance of the full adder shown in Fig. 1 were numerically examined using the 3D-FDTD method. The full adder comprised the components discussed in Section 3.2, and the phases of the plasmonic signals at the C2 port were adjusted to be equal to that of each input signal at A0, B0, A1, and B1 by taking the equivalent phase change of each component into consideration. In addition, each input intensity was controlled to ensure that the output intensity at the C2 (S1 and S2) port was equal, because each path length between the input and output port was different and thus the transmission loss for each path was also different. The intensity ratio of each input port was roughly set to B1:A1:B0:A0:Ref. = 10:10:1:1:1 and the input power was set to approximately 10 and 1 mW to obtain the ratio at the input ports. This intensity control was obtained by changing the length and width of the grating set at the input waveguides (grating for SPP generation) [29].

Some numerical results (i.e., intensity distribution of SPPs) are shown in Figs. 4–7. For all signal input patterns, the intensity distribution at the output port was calculated by integrating the intensity distribution for a distance corresponding to the one wavelength of SPPs. The diagram of the output intensity normalized with that of the (B1 A1 B0 A0) = (0 0 0 1) input pattern are shown in Fig. 8. The minimum ratio of level "0" and "1" was calculated to be 1.5 dB for C2, 1.5 dB for S1, and 2.0 dB.

4.2 Fabrication and Evaluation

The full adder designed in Section 4.1 was fabricated using a CMOS-compatible process excepting the metal material. In this adder, Au film was selected because of its chemical stability in a laboratory atmosphere. In practice, an Al film can be used instead of Au film, and the performances as a waveguide metal is nearly the same for Al and Au [23].

Fig. 9 summarizes the fabrication procedure of the full adder. A thick Au film was deposited on a silica wafer and Au bumps were cut down to pyramid shapes at the required positions using focused ion beam (FIB) etching (SII Nanotechnology Inc., SMI3200, acceleration voltage: 10 kV, beam current $<$20 nA). After the etching, a 500-nm-thick SiO_2 film was formed on the Au surface, and the SiO_2 film was simultaneously patterned to the circuit by FIB etching. A scanning electron microscope image of a fabricated full adder for the case of (B1 A1 B0 A0) = (0 1 1 0) input pattern is shown in Fig. 10. The fabricated length of the full adder was approximately 50 μm, which was

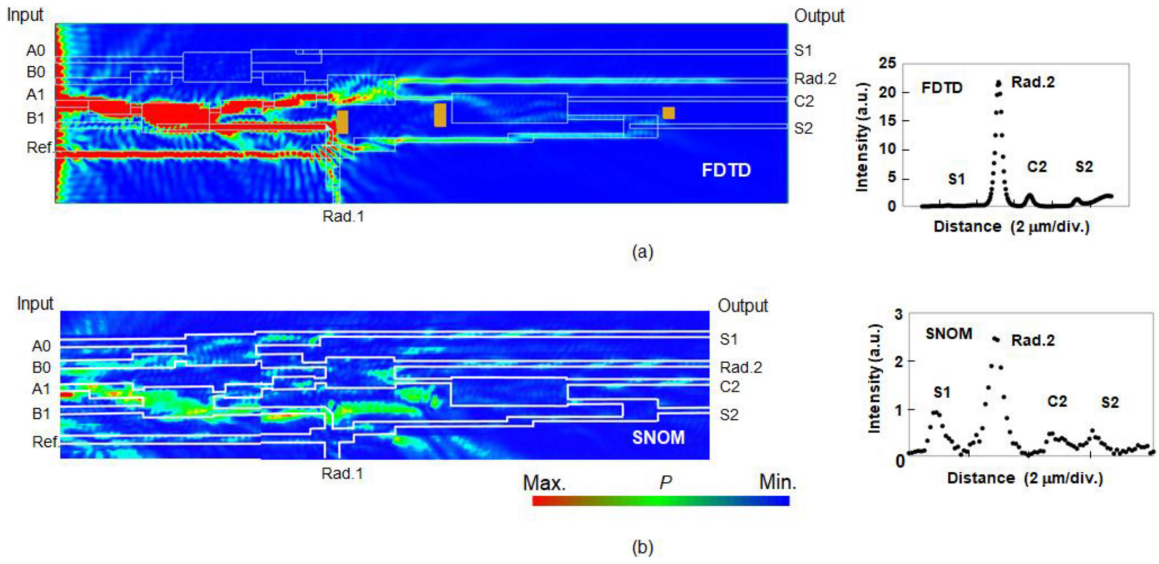

Fig. 5. Intensity distribution of plasmonic signals and output intensity pattern under input signal pattern. (B1 A1 B0 A0) = (0100). (a) simulated with FDTD method and (b) monitored with SNOM.

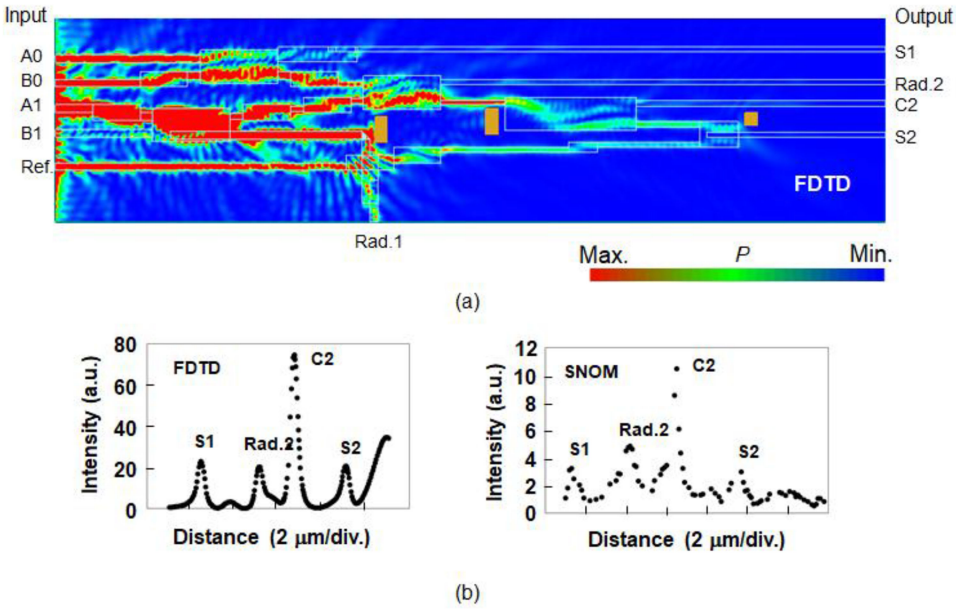

Fig. 6. Intensity distribution of plasmonic signals under the input signal pattern (B1 A1 B0 A0) = (0111): (a) simulated with FDTD method, (b) numerical and experimental intensity distribution at output port.

needed to synchronize the phase at C2 with the input signals and to ensure that each input intensity was almost equal at the output port.

The evaluation of the fabricated circuits was performed using a scanning near-field optical microscope (SNOM, Japan Spectroscopic Company (JASCO), NFX-520) and the monitoring system is shown in Fig. 11. The back side of a silica substrate was illuminated with collimated incident light, which was modulated at a frequency of 270 Hz. A tunable laser (Koshin Kogaku Co., Ltd., LS-601A)

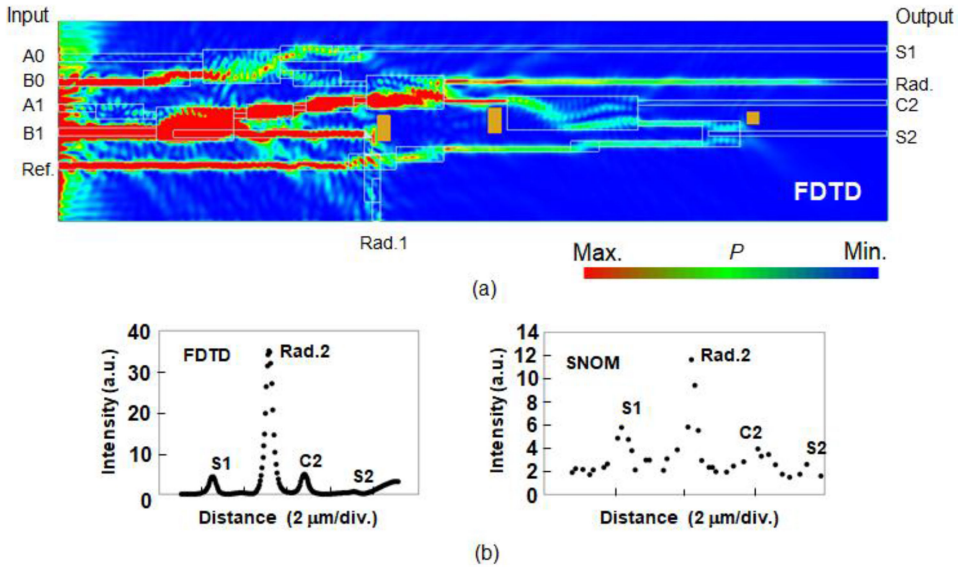

Fig. 7. Intensity distribution of plasmonic signals under the input signal pattern. (B1 A1 B0 A0) = (1010). (a) simulated with FDTD method, (b) numerical and experimental intensity distribution at output ports.

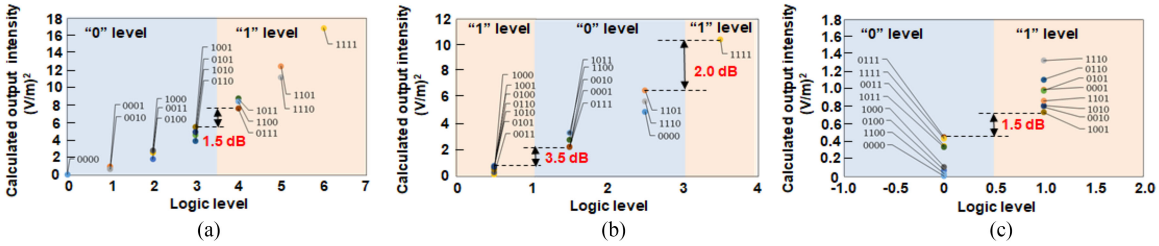

Fig. 8. Diagrams of the output intensity normalized with that of the input pattern (B1 A1 B0 A0) = (0 0 0 1) corresponding to each logic level: (a) output at C2, (b) output port at S2, and (c) output port S1. The horizontal axes also indicate the magnitude of the root of the defined intensity in Table 1.

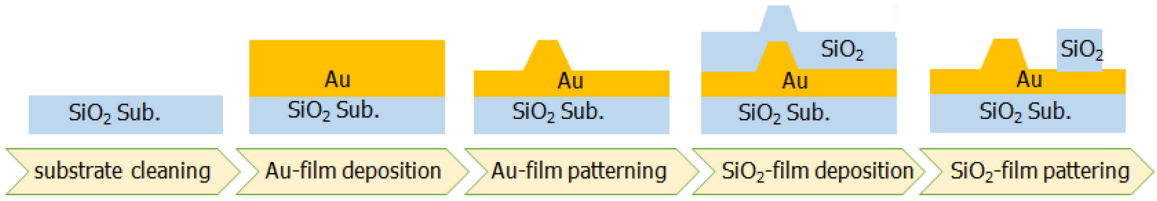

Fig. 9. Fabrication procedure of the full adder.

was used as an optical source (the output power: a few mW). Here, the gratings to convert the incident light to SPPs were set at the input ports corresponding to the input signal patterns (Fig. 10).

The diameter of the incident light beam was set at a few tens of micrometers in diameter to maintain constant optical input power with no optical axis deviation during monitoring, and its electric field was set in the direction perpendicular to the gratings to excite SPPs. For this structure, plasmonic signals were only coupled to the input port corresponding to each input pattern. The near field optical probe (JASCO) was covered with Au, and an aperture of approximately 100 nm in diameter was set at the top. Scattered and stray light from the circuit were accepted through

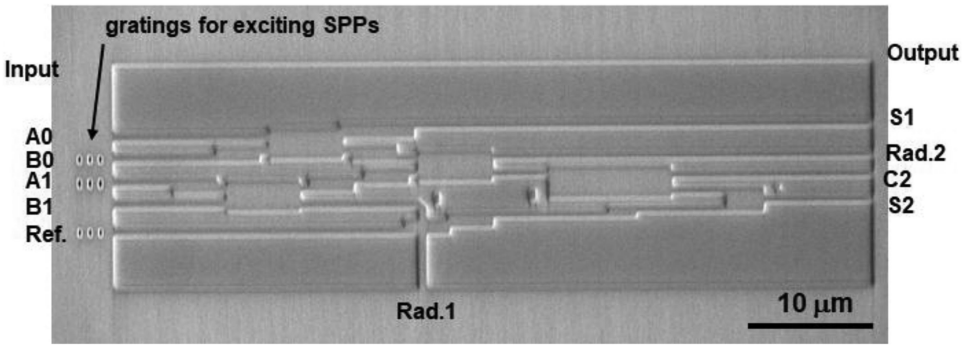

Fig. 10. Scanning electron microscope image of a fabricated full adder for the case of (B1 A1 B0 A0) = (0 1 1 0) input pattern.

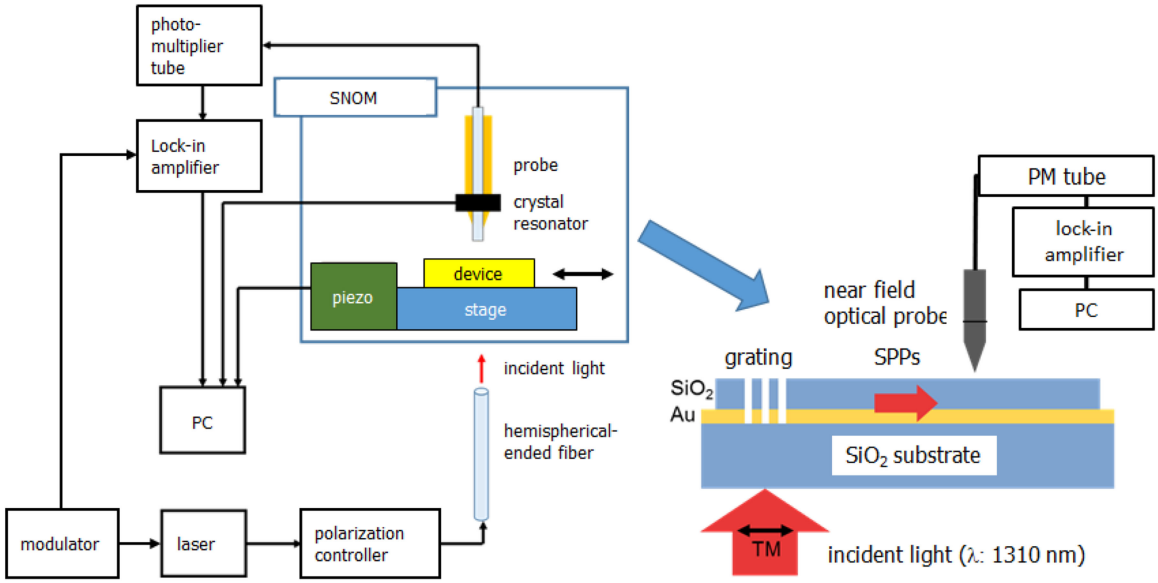

Fig. 11. Schematic diagram of evaluation system for scanning near field optical microscopy.

the aperture in addition to the near field signals. The plasmonic signal intensity distributions of several input patterns were monitored at 100-nm steps under continuous light incidence, where some monitoring results are shown in Figs. 4 and 5. Here, the SNOM intensity monitoring was divided into two areas because the entire area of the full adder was too wide for monitoring as one area.

In Fig. 4(b), most plasmonic signals in the input port Ref. passed to the port Rad. 1 via the cross point of the single- and multi-mode waveguide at just before the port Rad. 1. This resulted in the weak output signal S2 in Fig. 4(b) when compared with that of simulated in Fig. 4(a). In Fig. 5(b), the Au bump in the vicinity of port Rad. 1 seemed not to work well, where most plasmonic signals inputted in port A1 was emitted from the waveguide to air over the bump, as recognized in the figure. These were caused by errors in etching processes and solved by fabricating them in accordance with the designs. These fabrication factors and the characteristics of the SNOM probe influenced the intensity distribution monitored with the SNOM, and the monitoring patterns became vague and deviated from the simulated patterns at some sections. However, the generation and propagation of SPPs along the waveguides defined were recognized in the monitored patterns. The intensity distribution at the output ports was exact because no scattering part was located at these

sections. These output intensity distributions were also inserted in Figs. 4–7, where the intensity distribution at the output port was calculated by integrating the intensity distribution for a distance corresponding to the one wavelength of SPPs along the single-mode waveguides (output ports). The output patterns relatively corresponded to the results simulated by the 3D-FDTD method and supported the simulation results.

The propagation loss roughly estimated by 3D-FDTD method was approximately 20 dB between the input ports and the output port, C2, of the full adder, although an exact estimation was difficult because of the complicated paths corresponding to the input patterns. The propagation loss of a 50-μm-long single-mode waveguide was calculated to be approximately 6 dB in the 1310-nm-wavelength band [30], and the loss increased in the complex waveguide structure of the full adder. Approximately half of the estimated propagation loss of 20 dB resulted from the plasmonic loss (ohmic loss). The remaining half was caused by the distribution loss at the arithmetic unit, distributor, and equalizer, where the plasmonic signals were divided into multiple waveguides connected to the output ports, S1 and S2, or emitted through the radiation ports, Rad. 1 and 2, as redundant SPPs (emission loss).

Our design and fabrication methods were easily applied to the circuits composed of silicon-based ridge-type waveguides. In such circuits without ohmic loss of SPPs, the distribution loss and emission loss govern the total loss of the full adder (about 10 dB), and thus, such a full adder will operate at light speed without heat generation.

The simulation and experimental data herein are primitive results, and thus the difference in the plasmonic power level between “0” and “1” is relatively small because the configuration of each component and the accuracy of fabrication processes were not optimized. However, the feasibility of the proposed plasmonic logic circuit was numerically and experimentally demonstrated as a cascadable full adder comprising only single- and multimode-waveguides and fabricated using a CMOS-compatible process.

5. Conclusion

A cascadable plasmonic full adder was proposed, whose performance was demonstrated. The phase of the carry-out signal was synchronized with those of the input signals to ensure the cascade connection, and a few novel waveguide components such as divider and equalizer were developed to construct the circuit. The 3D simulations of the full adder performance calculated that the difference between “0” and “1” logic level as more than 1.5 dB. For some signal input patterns, the simulation results were experimentally confirmed for the full adder fabricated using CMOS-compatible process excepting the metal material. The intensity distribution of plasmonic signals were monitored with a scanning near-field optical microscope and coincided with those of simulated. These results were primitive but indicated feasibility of the cascadable plasmonic full adder.

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