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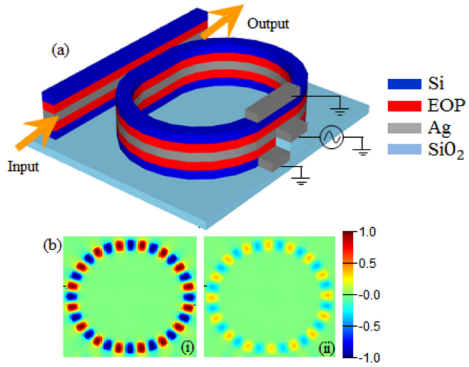

(a) Modulator Design, (b) Electric field confinement in the racetrack resonator for (i) no applied voltage, (ii) applied voltage of 1 V.

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Sub-Femtojoule Hybrid Plasmonic Optical Modulator

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Abstract: A highly compact optical modulator is proposed and analyzed. The modulator is based on the hybrid plasmonic waveguide platform. The structure of the modulator is built from silicon, silver, and electro-optical polymer layers. Hybrid plasmonic modes of symmetric and asymmetric natures excited in the structure were investigated. The symmetric mode is characterized by its lower propagation loss, so it was selected for the excitation of the device. The modulator's operation mechanism is based on the racetrack resonator configuration. Full three-dimensional electromagnetic analysis was performed around the 1.55-μm telecommunication wavelength. Different parameters such as the power coupling to the bus waveguide, the bend loss, the propagation loss, and the Q-factor of the resonances were studied in order to optimize the racetrack resonator design. The modulator is characterized by its extremely low energy consumption of 0.5 fJ/bit, high modulation depth of 10.5 dB, while the insertion losses were limited to 0.5 dB.

Index Terms: Plasmonics, racetrack resonator, electro-optic polymers, optical modulators.

1. Introduction

Silicon photonics has demonstrated success in a wide variety of components and devices such as couplers, splitters, and sensors. However, the silicon photonic modulator is still encountering challenges related to silicon's lack of strong electro-optic (EO) effects [1], [2], while the free carrier plasma dispersion effect is the commonly used method for modulation in silicon [2], [3]. The silicon organic hybrid platform [4] which combines silicon with materials possessing strong EO properties such as electro-optic polymers (EOPs) may form a suitable base for developing optical modulators [5], [6]. However, there is an increasing demand for the miniaturization of the photonic components and their integration with electronic components on the same chip. The attempt of downsizing silicon components faces the classical diffraction limit [7]. This limit prohibits nano-sized silicon components, it only allows for micro-sized components.

Plasmonic effects [8], [9] can be utilized for solving both challenges of the weak EO effect and the downsizing of optical components. Firstly, EOPs can be combined with plasmonic components in order to develop highly compact plasmonic modulators. The incorporation of EOPs with plasmonic components forms the hybrid plasmonic platform [4]. In this platform, the plasmonic waveguide

remains responsible for confining the electromagnetic field, while the EOP is responsible for the desired electro-optic effects.

Secondly, surface plasmon polaritons (SPPs) excited at metal/dielectric interfaces can be confined in nano-sized gaps, which breaks the classical diffraction limit [7]. This property enables the miniaturization of plasmonic components to nano-sizes that were not achieved in the realm of silicon photonics. Moreover, plasmonic structures are characterized by the enhanced electromagnetic fields at the metal interfaces.

Different configurations utilizing the plasmonic and hybrid plasmonic platforms have shown high potential for achieving fast, compact, and low power consumption modulators. These configurations include but are not limited to directional couplers [10], microdisk resonators [11], ring resonators [12]–[14], Mach-Zender interferometers [15], [16], asymmetric hybrid plasmonic waveguides [17], and plasmonic phase modulators [18]. However, the major challenge of such devices is the high insertion loss. This loss is mainly due to inherent intrinsic losses associated with plasmonic structures. Thus, it is important to reduce such losses while maintaining the compactness of the device. This will result in improving performance of plasmonic based modulators.

Previously reported modulators such as the plasmonic Mach-Zender modulator [19] showed an extinction ratio of 5.5 dB, and insertion loss of 5.8 dB, with a footprint of 15 μm^2. The electro-optical plasmonic ring resonator demonstrated in [20] showed an extinction ratio of 7 dB, resonator Q-factor of 190, and ring resonator radius of 5.48 μm. Electro-optical switches and modulators based upon ($Ge_2Sb_2Te_5$) GST-embedded SOI channel waveguides [21] showed low insertion loss, and low crosstalk at an operation wavelength of 2.1 μm, while the authors reported that at the operating wavelength of 1.55 μm, the performance is decreased, and the insertion loss was too large, in the range of 2.3−3.9 dB. Also, other structures based on five-layer silicon on nitride gap-slab and gap-strip plasmonic waveguides [22] showed an extinction ratio of 5 dB at an operation wavelength of 5 μm.

In this work, we demonstrate a low-loss highly compact modulator. The structure of the modulator is composed of a stack of layers arranged vertically bottom to top as silicon-EOP-metal-EOP-silicon, on a buried oxide. The modulator structure is optimized by minimizing insertion loss. This modulator is designed and analyzed using 3D Finite Difference Time Domain simulation (FDTD) tools. The demonstrated modulator is characterized by its low insertion loss, compactness, and high modulation depth. We introduced initial results of this device [23]. In this paper, more details of the proposed modulator are introduced including full study of: structure, waveguide properties, and optimization of the design. The excited plasmonic modes are discussed in detail. Moreover, the electromagnetic analysis of resonator and the performance of the modulator are completely investigated in this paper.

2. Methods

The proposed plasmonic modulator is based on the racetrack resonator operation to benefit from its sharp resonances and high Q-factors. Reducing insertion loss of our proposed modulator is expected to have a strong positive impact on the modulation depth and the resonator Q-factor. Thus, for the waveguide design, the asymmetric hybrid plasmonic waveguide (AHPW) [24] was used, which excites long-range surface plasmon polaritons, while the hybrid plasmonic symmetric mode was selected.

2.1. Device Structure

The proposed hybrid plasmonic modulator is shown in Fig. 1a. The device is composed of a straight (bus) waveguide which forms the input and output ports, and a racetrack resonator which resonates at distinct frequencies. The waveguide structure of the device consists of five layers: Silicon-EOP-Metal-EOP-Silicon layers, all on a SiO_2 substrate. The cross-section of the waveguide is shown in Fig. 1b. While this work focuses on the optimization of the modulator design and not fabrication, we are including suggested fabrication steps in supplementary material (fig. S1). The fabrication

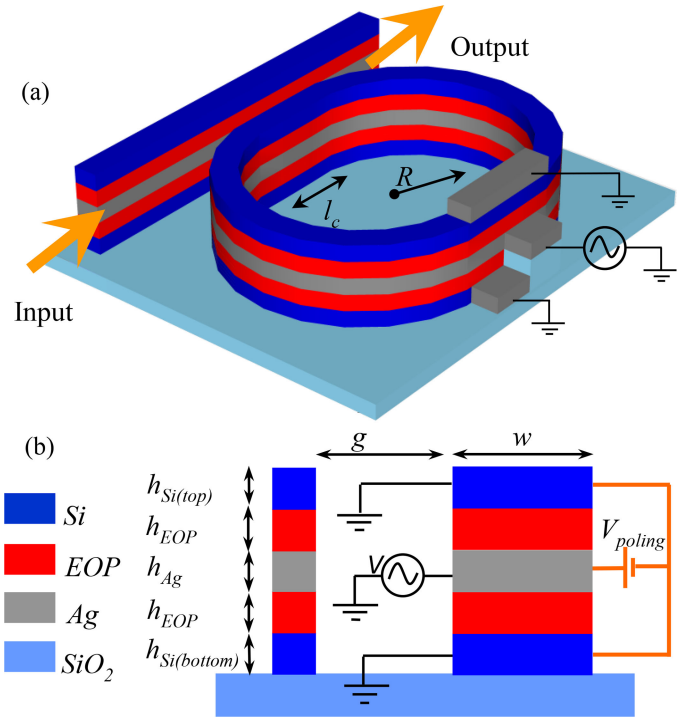

Fig. 1. Schematic layout of the modulator: (a) perspective view showing the racetrack resonator and the bus waveguide designs. R is the ring radius of the racetrack, $R = 2\ \mu$m, l_c is the length of the coupling region in the racetrack resonator, $l_c = 200$ nm (b) cross section view showing the poling of the EOP.

method is inspired by the MEMS and hybrid SOI / III-V platforms that are gaining popularity in silicon photonics. The novelty in this work is the 5-layer structure in developing a hybrid plasmonic racetrack resonator and its use as a compact modulator. We used silver because its plasmonic properties are very well understood, however, it is not CMOS compatible as silver in a contaminant in CMOS processes. This device can be integration in the same way that III-V devices are integrated on chips. For full CMOS compatibility, a different metal, such as tungsten, could be used. The same and modulation concept will apply, but the system has to be re-optimized for other metals.

2.2 Operational Principle and Modeling Methodology

Using intrinsic silicon would result in high resistivity and therefore the modulator speed will be substantially reduced, while using highly doped Si would result in high losses of the effective mode due to the high free carrier concentration. So, low doped Si of 10^{17} cm^{-3} carrier concentration has been used in our structure. The values of the Drude model parameters for the 10^{17}cm^{-3} phosphorous doped Si are: permittivity; $\varepsilon_{Si} = 11.7$, plasma frequency; $\omega_p = 3.56 \times 10^{13}\ rad/s$, and collision frequency; $\Gamma = 9.7 \times 10^{8}\ rad/s$,where these values were based on the doped Si models calculations given by [25].

The change in the EOP refractive index in response to an applied voltage is described by:

$$\Delta n_{EOP} = \frac{1}{2} n_{EOP}^3 r_{33} \frac{V}{h_{EOP}} \tag{1}$$

where $n_{EOP} = 1.6$ at no applied voltage, and the electro-optic coefficient $r_{33} = 300$ pm/V [11], [26], [27], V is the applied voltage in volts, h_{EOP} is the thickness of the EOP layer and across which the voltage is applied. The Ag layer material properties are described by Johnson and Christy [28], while $n_{SiO2} = 1.45$, around the1.55 μm wavelength.

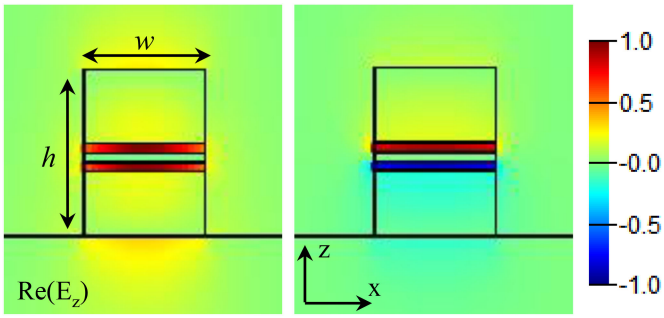

Fig. 2. Hybrid plasmonic modes supported by the structure: (a) symmetric mode, and (b) asymmetric mode. The color bar indicates the intensity of the real part of the E_z component, $w = 400$ nm, $h = 340$ nm.

3D simulations were performed by the means of a commercial grade simulator based on the FDTD method [29]. The smallest mesh sizes of the simulation region are $\Delta x = 20$ nm, and $\Delta y = 10$ nm, $\Delta z = 2$ nm. The simulations were made to run for a simulation time of 7000 fs, which is sufficient for allowing the fields in the racetrack resonator to decay to zero. Boundary conditions were 16 layers of uniaxial anisotropic perfectly matched layer (PML) and the device footprint is 22 μm^2.

2.3 Hybrid Plasmonic Mode

When the bus waveguide is excited by a modal source of wavelength range of 1.5 to 1.6 μm, SPPs are generated at the Ag/EOP interfaces, with the plasmonic mode strongly guided in the EOP layers. Thus, the interaction of the electromagnetic fields with the EOP is maximized, so the effective refractive index of the mode is highly dependent on the refractive index of the EOP, as will be discussed in greater depth later. This aids in reducing the applied voltage needed to induce a given change of the guided mode effective index. As will be shown, this enabled modulation at low voltages of only 1 V.

The hybrid plasmonic mode excited in the bus waveguide can be of symmetric or anti-symmetric nature as shown in Fig. 2. Theoretical discussion of the modes is based on treating the structure as the combination of two coupled hybrid waveguides [24], namely the bottom Si-EOP-Ag layers, and the top Ag-EOP-Si layers. However, the choice between symmetric and asymmetric modes for successful operation of the device is subject to losses considerations. The asymmetric hybrid plasmonic waveguide AHPW was previously addressed [24], where the discussion showed that in order to reach minimum propagation loss, only field components across the metal need to be symmetric, while the mode field components within the rest of the structure can remain non-identical [24]. It can be observed from Fig. 2 that the symmetric mode is identical across the metal layer which is not the case for the asymmetric mode which has opposite signs of its electric field components below and above the metal layer. The asymmetric mode complex effective index is $2.69 + 0.017i$, with modal loss of 0.61 dB/μm, while the symmetric mode effective index is $1.86 + 0.0003i$, and its modal loss is only 0.013 dB/μm, for the same device structure and same dimensions; $h_{Si(bottom)} = 140$ nm, $h_{Si(top)} = 160$ nm, $h_{EOP(bottom)} = h_{EOP(top)} = h_{Ag} = 20$ nm. Due to its significantly lower modal loss, the symmetric hybrid plasmonic mode was selected for the excitation of the input signal.

3. Results

3.1 Coupler Optimization

Coupling optical power to the hybrid plasmonic bus waveguide is carried by means of a conventional SOI strip waveguide of height 360 nm. The width w of the coupler waveguide must be wide

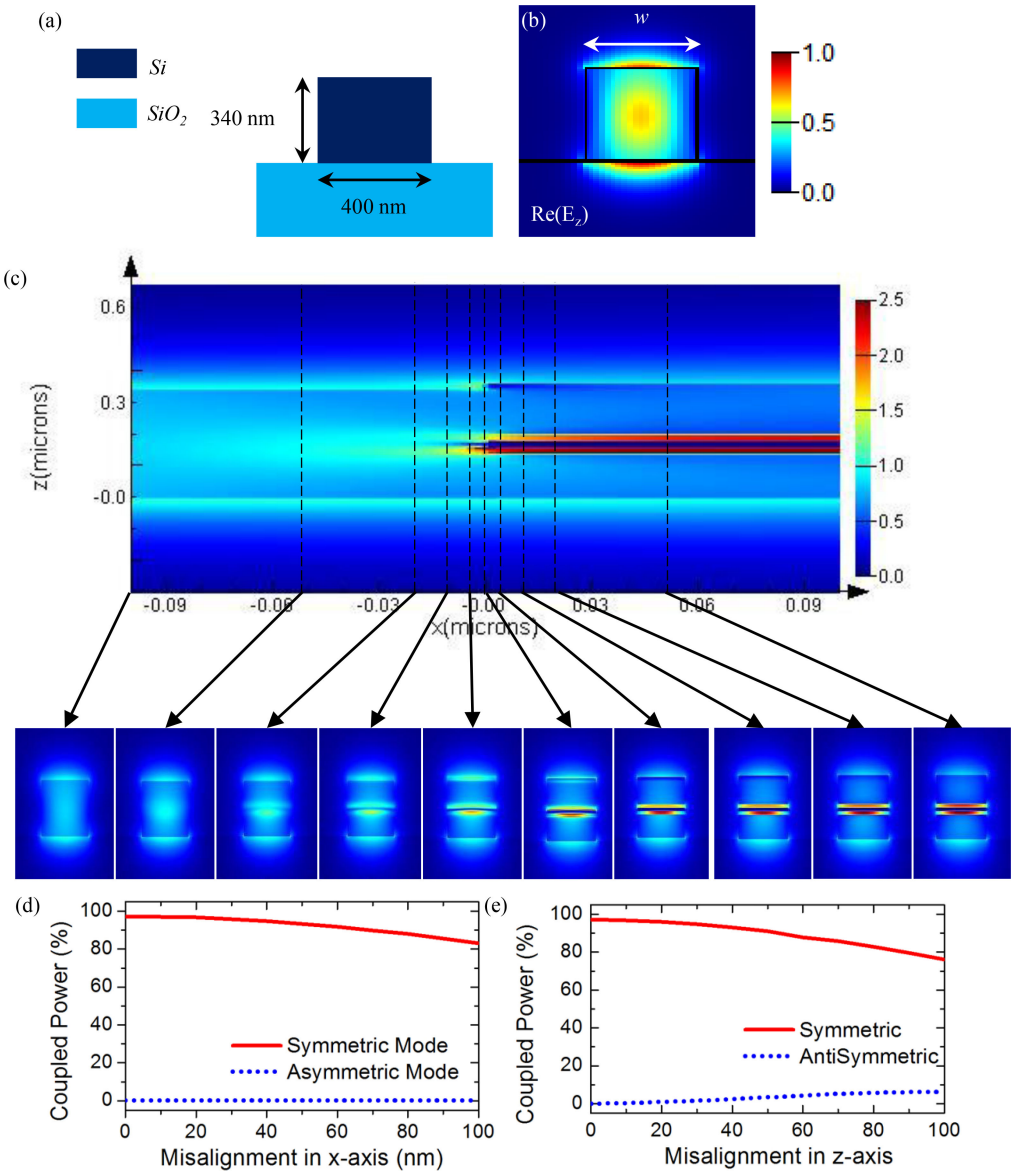

Fig. 3. (a) Schematic layout of the SOI strip coupler waveguide (cross-sectional view), (b) electric field distribution $\{\mathrm{Re}(E_z)\}$ of the TM mode. (c) (top) Electric field intensity at the coupler. The interface between the dielectric waveguide and the plasmonic waveguide is at x = 0. (bottom) Mode profiles at 100, 50, 20, 10, 5 nm before the interface and at the interface (x = 0) and at 5 nm, 10, 20, 50 nm after the interface. $h_{Si(bottom)} = 140$ nm, $h_{Si(top)} = 160$ nm, $h_{EOP(bottom)} = h_{EOP(top)} = h_{Ag} = 20$ nm, $w =$ 400 nm. Effect of misalignment on the coupled power between the coupler SOI waveguide and the bus waveguide; (d) misalignment in x-axis, and (e) misalignment in z-axis.

enough to allow as much optical power to be coupled to the bus waveguide as possible while avoiding generating higher order modes. Fig. 3(a) and (b) show the design and mode profile of the SOI coupler waveguide, respectively. Overlap analysis and power coupling efficiency between the coupler and bus waveguides were performed using a commercial simulator eigen-mode solver and propagator [30] at the 1.55 μm wavelength. The tolerance of the device was studied by introducing misalignment between the SOI coupler waveguide and the bus waveguide in x and z directions to the device while recording the percentage of power coupled from the SOI waveguide to the bus

TABLE 1
Effect of the SOI and Bus Waveguides Widths on the Power Coupling for Both the Symmetric and Asymmetric Modes

SOI and bus waveguides width (nm)	Asymmetric Mode Power Coupling (%)	Symmetric Mode Power Coupling (%)
200	0.08	80
250	0.001	92.2
300	0.004	95.4
350	0.01	0.96
400	0.05	97.4
450	0.08	97.8
500	0.07	98.2

waveguide using [30]. The SOI waveguide starts to experience higher order modes for widths larger than 400 nm, while at that width, the coupling efficiency to the hybrid plasmonic symmetric mode reaches 97%, so we chose a waveguide width of 400 nm for the design of the racetrack resonator modulator.

Power coupled between the coupler SOI waveguide and the hybrid plasmonic bus waveguide increases with increasing width as shown in Table 1. Excitation of the SOI coupler waveguide by the TM mode excites the low loss symmetric hybrid plasmonic mode in the bus waveguide, while the anti-symmetric mode is largely suppressed for two reasons. Firstly, the anti-symmetric mode has significantly higher losses than the symmetric mode. Secondly, the anti-symmetric mode power coupling efficiency is considerably lower than that of the symmetric mode as shown in Table 1. Fig. 4(c) visualizes this coupling.

Alignment tolerance was measured by shifting the centers of the SOI coupler waveguide and the bus waveguide with respect to each other in both the x and z axes, while recording the coupled power to both symmetric and asymmetric modes. Fig. 3(d) and (e) show that the fraction of power coupled to the asymmetric mode is extremely small compared to that of the symmetric modes, which minimizes the effect of the lossy asymmetric mode to the insertion loss of the device. Also, it can be observed that for a misalignment of 50 nm (for both x and z shifts); the power coupled remains above 90% (only 0.45 dB loss) for the symmetric mode of the 400 nm wide structure. So, ultra-fine alignment is not required for our device.

3.2 Si-EOP-Ag-EOP-Si Waveguide Optimization

In this section, the design of the bus waveguide and the racetrack resonator is investigated. The main goal is to achieve optimized dimensions for the waveguide structure in terms of modal effective index, propagation losses, bend losses, and power confinement. Fig. 4 shows a parametric study of the effect of the dimensions of the top and bottom Si layers on the non-biased symmetric hybrid plasmonic mode properties, namely the: (a) modal effective index, (b) modal loss in dB/μm.

Fig. 4(b) shows that both bottom and top Si layers of height 140 nm to 180 nm experience lower propagation losses, this result can be considered as the “coarse” adjustment of the Si layers heights. The top Si is surrounded by air cladding and the bottom Si is surrounded by SiO_2 cladding. To compensate for the index asymmetry along the vertical z-axis, the top Si layer should be slightly larger than the bottom Si layer. Regarding EOP layer thickness, symmetric mode propagation losses are minimized when the effective index of the structure is symmetric about the metal layer [24], therefore both the EOP layers should be the same thickness. Additionally, EOP thickness is inversely related to voltage as shown in eq. (1), so EOP thickness should be minimized in order to minimize the voltage requirements.

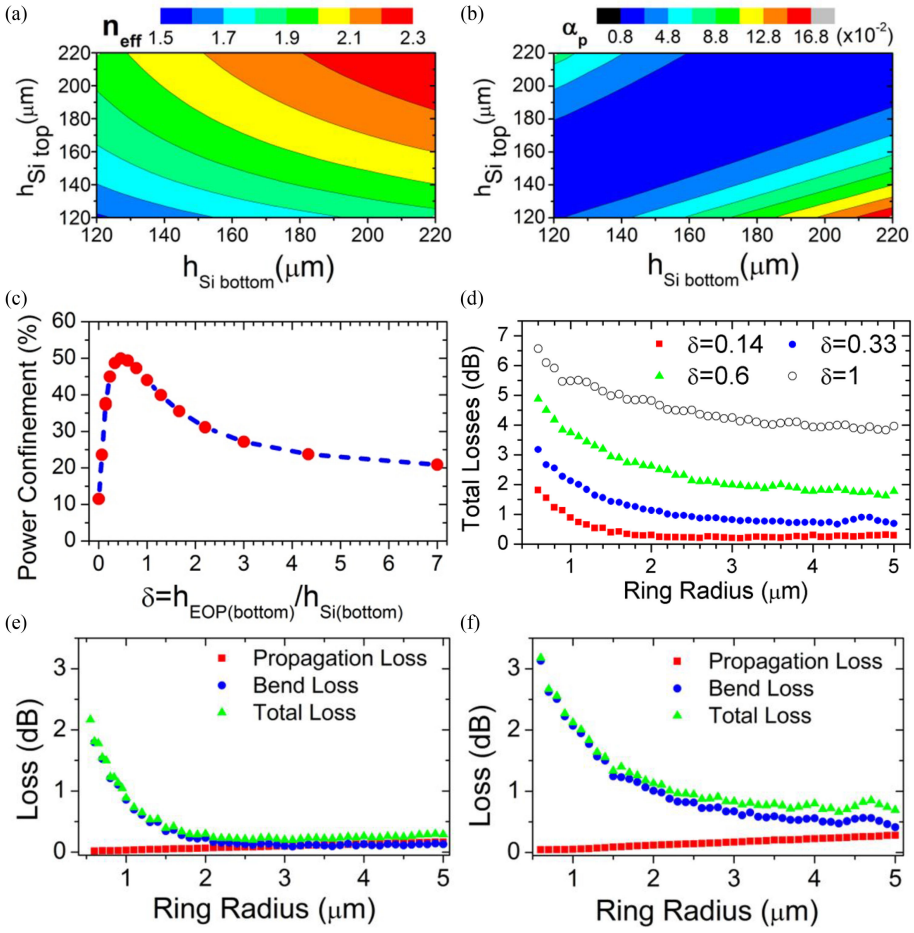

Fig. 4. Parametric study of the effect of the Si layers dimensions on the non-biased symmetric hybrid plasmonic mode properties: (a) mode effective index, (b) propagation loss in dB/μm, $w = 400$ nm, $h_{EOP(bottom)} = h_{EOP(top)} = h_{Ag} = 20$ nm. (c) Power confinement of the symmetric hybrid plasmonic mode as a function of $\delta = h_{EOP}/h_{Si}$, the red dots are the measured points, while the blue line is the overall behavior. (d) Total losses of the resonator's ring section as a function of its radius for four different designs defined by the parameter δ. Study of the propagation, bend, and total losses for: (e) $\delta = 0.14$, (f) $\delta = 0.33$.

TABLE 2
Design Variations

Design	h_{EOP}	h_{Si}	$\delta=h_{EOP}/h_{Si}$	Total Losses at R=2μm (dB)
1	20	140	0.14	0.3
2	40	120	0.33	1.1
3	60	100	0.6	2.6
4	80	80	1	4.8

Power confinement in the waveguide at different combinations of heights of the EOP and Si layers are studied in Fig. 4(c). The effect of the resonator radius R on total losses (propagation loss + bend loss) is shown in Fig. 4(d). Defining the ratio between the EOP and Si layers as $\delta = h_{EOP}/h_{Si}$, we investigated the power confinement and the total losses of four different designs having the same width $w = 400$ nm, denoted as shown in Table 2. It should be noted that in Table 2, the Si layers of the device were defined by the undoped Si model in order to save computational power and time, while

the performance of the modulator (Section 3.4) was investigated using the doped Si model in order to reduce the resistivity of the Si layers to achieve higher speed operation.

Fig. 4(c) shows that the power confinement reaches a maximum with Design 1, while Fig. 4(d) shows that Design 1 also has the lowest total losses. Fig. 4(e) and (f) show that bend loss is the dominant loss mechanism and that Design 1 has lowest bend losses. This can be explained by how much *plasmonic* is the hybrid mode. The plasmonic nature of the mode resides in the EOP due to the neighboring Ag. In comparison to other designs, in Design 1, the field is most strongly confined in the EOP layers, thus the plasmonic nature of the mode is highest. It is known that plasmonic waveguides can have much smaller bend radii than regular photonic waveguides, including 90° bends [31]. The higher plasmonic nature of design 1 reduces the loss at the bend of the structure, this results in considerably lower bend loss compared to the other designs, where their bend losses are higher as can be observed from fig. 4(e) and (f). For small ring radii, the total losses associated with the $\delta = 0.14$ design show a decrease with increasing ring radius, but for radii equal to or larger than 2 μm, the total losses are almost constant. The total losses are the sum of the FDTD simulated bend loss and the propagation loss. The propagation loss L_p in dB is calculated by:

$$L_p = \alpha_m \times 2(\pi R + l_c) \tag{2}$$

where α_m is the modal loss coefficient in dB/m, R is the ring radius, and l_c is the coupling length shown in Fig. 1(a), $l_c = 200$ nm. The coupling length optimization is detailed in the supplementary material file (fig. S2). The EOP material loss is only 2 dB/cm [26], this is 65 times smaller than the symmetric hybrid plasmonic modal loss ($\alpha_m = 130$ dB/cm), and so the EOP loss is neglected in the calculations.

The propagation, bend, and total losses of designs 1 and 2 were calculated using 3D FDTD simulations, they are depicted in Fig. 4(e), and (f), respectively. At very small radii, the bend loss is large and dominates the total loss while propagation loss is significantly low. As the radius increases, the bend loss decreases as expected, while the propagation loss is still low owing to the low loss symmetric hybrid plasmonic mode in use ($\alpha_m = 0.013$ dB/μm). Even when the radius reaches 5 μm, the propagation loss still does not exceed the bend loss.

Thus, the "fine" adjustment of the design dimensions can be finally achieved: $h_{Si(bottom)} = 140$ nm, $h_{Si(top)} = 160$ nm, $h_{EOP(bottom)} = h_{EOP(top)} = h_{Ag} = 20$ nm, and $w = 400$ nm. It should be noted that such dimensions allow the middle of the Ag layer (170 nm above the SiO_2 substrate) of the waveguide structure to match the middle of the 360 nm height SOI strip waveguide coupler, and the width of the SOI coupler is 400 nm. Also, R does not need to be larger than 2 μm, as the bend loss is already minimized at that radius, which helps in minimizing the footprint of the device.

3.3 Racetrack Resonator Design Optimization

Coupling between the bus waveguide and racetrack resonator is investigated in order to achieve maximum coupling. Fig. 5 studies the effect of gap spacing between the bus waveguide and the racetrack resonator on coupling extinction ratio (ER) and Q-factor of the 1.55 μm resonance. The extinction ratio is defined by:

$$ER = 10 \times \log(1/P_{out}) \tag{3}$$

where P_{out} is the power coupled to the resonator. Q-factor is calculated by $Q = \lambda/\Delta\lambda$, where $\Delta\lambda$ is the full-width at half maximum (FWHM) of the resonance line. As observed from Fig. 5(a), the extinction ratio is minimum for a gap spacing of 200 nm. So, the gap spacing of the racetrack resonator modulator is set to 200 nm to maximize the fraction of power coupled to the resonator, while at this gap, $Q = 770$.

3.4 Performance

Performance of the proposed modulator is analyzed by studying different properties such as output spectrum, modulation depth, insertion loss, and modulation speed.

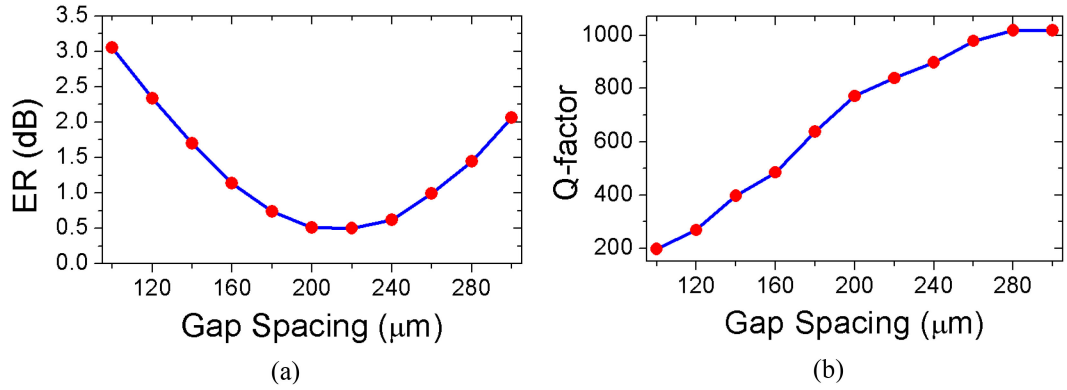

Fig. 5. Study of the effect of the coupling gap distance on the: (a) extinction ratio, (b) Q-factor of the resonance at the wavelength of 1.55 μm.

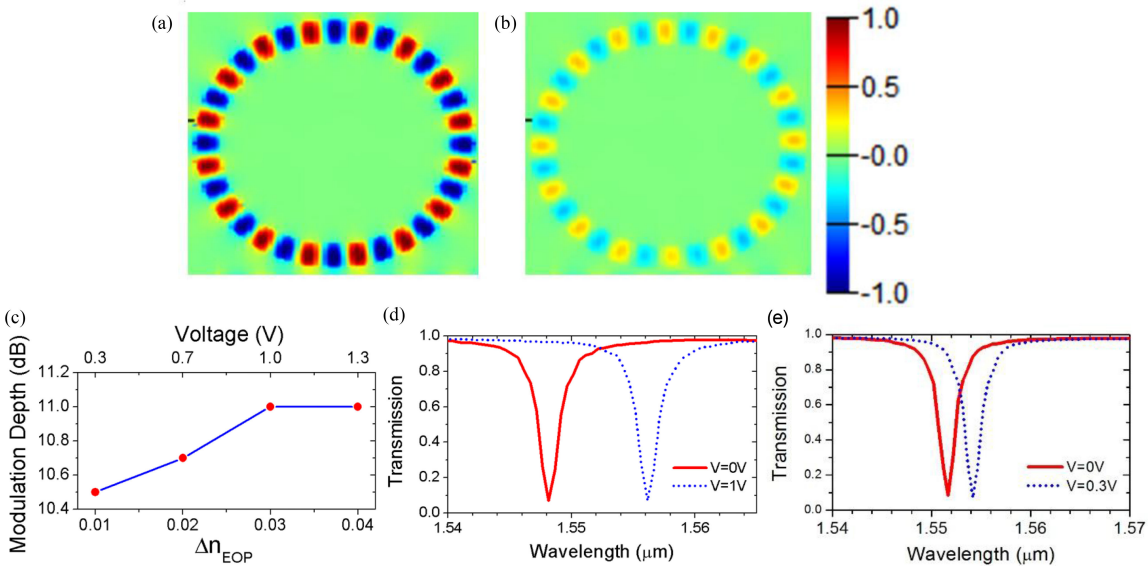

Fig. 6. Electric field component Re(E_z) in the racetrack resonator at $\lambda = 1.55$ μm for: (a) no applied voltage, (b) 1 V applied voltage. The field is monitored at the middle of the upper EOP layer. (c) Modulation depth as a function of Δn_{EOP} and applied voltage, $\lambda = 1.55$ μm. Transmission spectrum of the racetrack resonator showing the resonance shift in response to (d) 1 V, (e) 0.3 V applied voltage.

3.4.1 Modulation Depth: When there is no voltage applied across the EOP layers; the EOP refractive index keeps its initial value of $n_{EOP} = 1.6$, and the symmetric hybrid plasmonic mode effective index is $n_{eff} = 1.86 + 0.0003i$. The racetrack resonator has its resonances at distinct wavelength positions given by:

$$\lambda_m = \frac{2(\pi R + l_c)n_{eff}}{m} \tag{4}$$

where m is the resonance order. Upon applying a small voltage across the EOP layers, n_{EOP} changes according to (1), and consequently n_{eff} also experiences a change in its value. So, the racetrack resonator experiences resonance shifts. Fig. 6(a) and (b) visualizes the electric field distribution inside the racetrack resonator at $\lambda = 1.55$ μm. When there is no voltage applied across the EOP, the resonator is resonant and the field is strongly confined in the resonator, Fig. 6(a).

TABLE 3
Comparison of Our Results to State of the Art Hybrid Plasmonic Modulator

	Operational Voltage (V)	Energy Consumption (fJ/bit)	Modulation Depth (dB)	Insertion Loss (dB)	Footprint (μm^2)	Speed (Tbit/s)
State of the art hybrid plasmonic modulator [34]	3	3.6	8	2.3	11	1
Our symmetric mode based hybrid plasmonic modulator	1	6	11	0.5	22	1.7
	0.3	0.5	10.5	0.5	22	1.7

However, when 1 V is applied, the resonance wavelength red-shifts and the field is weakly confined in the resonator, Fig. 6(b).

This resonance wavelength shift can be depicted as a change in the level of power transmitted at the output port at the telecom wavelength of 1.55 μm due to the applied signal/voltage. The modulation depth shows an increase with the applied voltage as observed in Fig. 6(c). The output spectrum of the modulator measured at the output of the bus waveguide is shown in Fig. 6(d), where applying a small voltage of 1 V results in red-shifting of the 1.55 μm wavelength, and results in a modulation depth of 11 dB, while $\Delta\lambda_{3dB} = 2$ nm, and Q = 770. Fig. 6(e) shows the output spectrum when 0.3 V is applied, the modulation depth is 10.5 dB. The total insertion loss of the device is limited to 0.5 dB. The low insertion loss despite using doped Si model can be due to two reasons; firstly heavy doped Si was avoided and doping of 10^{17} cm^{-3} was used, secondly, the symmetric mode is mostly confined in the EOP layers, not the doped Si layers.

3.4.2 Modulation Speed: The EOP response is in the range of tens of femtoseconds [22], thus it has no pronounced effect on the modulation speed. However, the RC time constant of the electrical circuit needs to be investigated to estimate the speed of the modulator. The small thickness of the EOP layer ($h_{EOP} = 20$ nm) may result in high capacitance, but it should be noted that the surface area of the capacitor is also small, as calculated in supplementary information file (fig. S3), A = 5 μm^2. The capacitance of the modulator is found by:

$$C = \varepsilon_0 \varepsilon_{EOP} \frac{A}{h_{EOP}} \tag{5}$$

where C is the capacitance of one EOP layer which is equal to 5.6 fF. The two EOP layers are equivalent to two capacitors in parallel, so their capacitances add, so the total capacitance is C_t = 11.2 fF. More details about calculating the capacitance is in the supplementary information file. However, due to the parasitic capacitance, this value may increase to a maximum of 100 fF [32]. The used n-doped Si with doping concentration of 10^{17} cm^{-3} experiences a resistivity of 0.087 Ω.cm [33]. The resistance of the Si layers can be calculated by:

$$R = \rho \frac{l}{A} \tag{6}$$

where R is the resistance, ρ is the resistivity, l is the total height of the Si layers and is equal to 300 nm. Thereby, the total resistance of the Si layers is only 50 Ω, while the total resistance of the circuit may vary from 50 to 100 Ω depending on the quality of wiring.

$$\tau = RC \tag{7}$$

$$speed = \frac{1}{\tau} \tag{8}$$

where τ is the RC time constant. This allows a maximum speed that ranges from 100 to 200 Gbit/s. One should note that improved fabrication and connections can further reduce the parasitic capacitance and hence, increase the speed of the modulator. For example, the theoretical limit of our device's capacitance of 11.2 fF can allow a speed of 1.7 Tbit/s for 50 Ω total resistance. The bandwidth of the modulator is 50 THz, and defined by the resonator's response spectral range. The power consumption for a non-return to zero random bit sequence at frequency of 100 GHz is given by: $P = 2C_tV^2f/4$ [11], for an applied voltage of 0.3 V, this equals to 0.05 mW, which corresponds to energy consumption of 0.5 fJ/bit. More details of the power consumption calculation are in the supplementary information file. A comparison of the performance of our proposed modulator with a state of the art hybrid plasmonic modulator [34] is given in Table 3.

4. Conclusion

A hybrid plasmonic racetrack resonator modulator has been proposed and investigated using 3D FDTD simulation tools. The waveguide structure has been extensively studied and optimized for achieving high performance of the modulator. The symmetric hybrid plasmonic mode was utilized to minimize the propagation and bend losses and to maximize the power confinement in the waveguide. Coupling the optical power from a conventional SOI strip waveguide to the modulator's bus waveguide considerations were also taken into account. The modulator performance has been investigated, while it showed a remarkably low energy consumption of 0.5 fJ/bit, modulation depth of 10.5 dB, and insertion loss of 0.5 dB.

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