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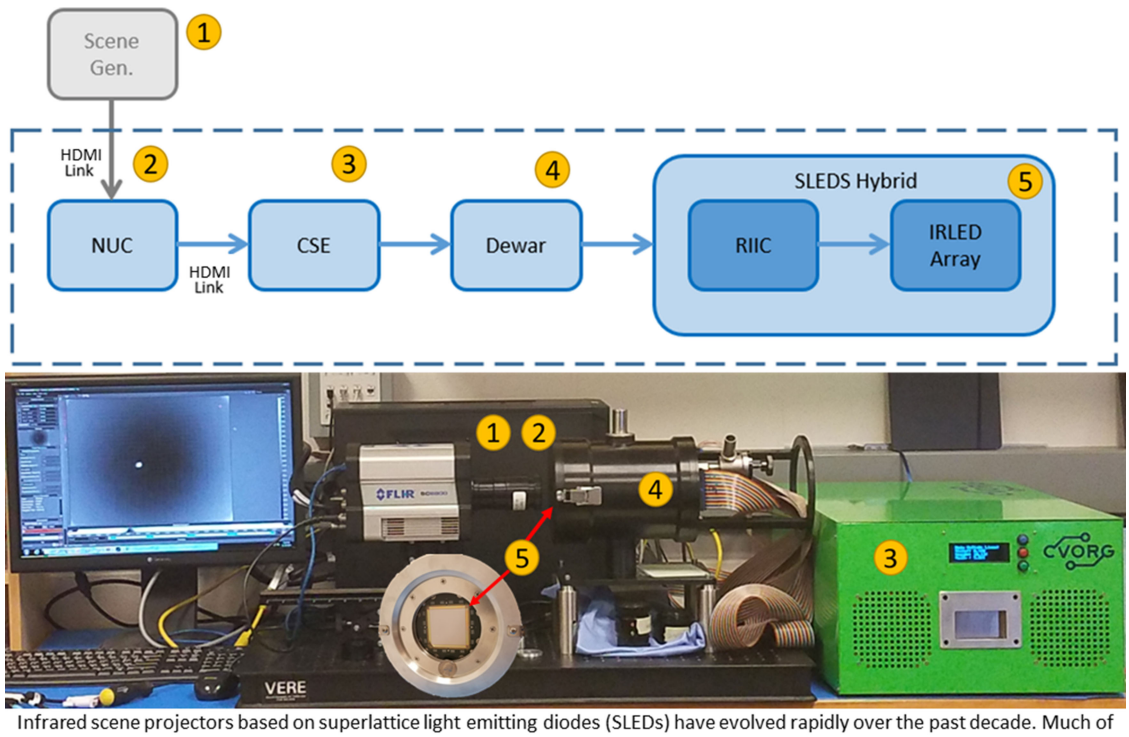

Infrared scene projectors based on superlattice light emitting diodes (SLEDs) have evolved rapidly over the past decade. Much of this development has been enabled by the design of a flexible support system for driving the SLEDs. A SLEDs projector consists of 5 main components: 1 - Scene generation computer, 2 - Non-uniformity correction (NUC)/control computer, 3 - Custom support electronics (CSE), 4 - Dewar, 5 - Hybrid.

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A Modular Platform for Rapid IRSP Development

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Abstract: Infrared scene projectors based on superlattice light emitting diodes (SLEDs) have evolved rapidly over the past decade. Much of this development has been enabled by the design of a flexible support system for driving the SLEDs. This paper describes the system and its benefits.

Index Terms: Infrared scene projector, superlattice light emitting diodes, firmware, MWIR.

1. Introduction

Infrared imaging devices play a key role in various larger systems, as noted in [1]–[3]. Testing and training these systems in real-world scenarios can be difficult, expensive, or impossible. Various forms of hardware-in-the-loop (HWIL) allow for realistic and repeatable testing which is critical to support system and device development. HWIL tests of infrared imagers have relied largely on infrared scene projectors (IRSPs) since the 1980s [1]. This reliance has largely driven the development of IRSP technology.

A complete IRSP is comprised of several components, including IR sources, scene producing optical or mechanical devices, and supporting elements to drive, control, and house these front-end components. The latter components play a significant role in furthering the development of IRSPs. To illustrate this importance, this paper presents a specific IRSP system and highlights several of the features that have enabled the rapid development of a set of projectors based on superlattice light emitting diodes (SLEDs). Section 2 reviews some history of IRSPs with an emphasis on the development of SLEDs IRSPs. Section 3 gives an overview of each component of the SLEDs IRSP system. Section 4 outlines the design approach for SLEDs firmware to achieve a modular and scalable design. Section 5 shows some of the results achieved thus far with each projector with example imagery.

2. Background

Over the past few decades, various IRSP technologies have been explored and some of these incorporated into HWIL testing facilities [3]. Resistive arrays have dominated this field since the

TABLE 1
SLEDs Projectors in Development

	SLEDS	TCSA	NSLED	HDILED TRL5	HDILED TRL6
Resolution	512x512	512x512	1024x1024	2048x2048	2048x2048
Spectral Range	1-color MWIR	2-color MWIR	1-color MWIR	1-color MWIR	1-color MWIR
Pixel Pitch	48um pixel	48um pixel	24um pixel	24um pixel	24um pixel
# CSEs	1	1	1	1	4
Max Frame Rate (Hz)	100	1000	500	125	500
Synchronization	COTS	COTS	COTS	COTS	Custom
IO (Pixels/sec)	25M	500M	500M	500M	2000M
Thermal Capacity (Watt)	20	20	20	20	200
Dewar	COTS	COTS	COTS	COTS	Custom
Year First Operated	2014	2016	2016	2018	TBD
Status	Delivered	In Progress	In Progress	In Progress	Proposed

1980s and have undergone significant development. Researchers at British Aerospace presented one of the first 256 $\times$ 256 (pixel), long-wave infrared (LWIR) projectors in 1991 [4]. Three resistor types have been explored: thin-film, bridge and suspended membrane [7]. Suspended membrane proved to have superior performance in various areas, including simulated temperature range and spectral range, and the ability to decouple power consumption from frame rate [1], [7]. Development of suspended membrane resistive technology began in the early 1990s. Researches at Honeywell presented multiple 512 $\times$ 512 systems and a 128 $\times$ 128 system (all wideband) in 1996 using suspended membrane technology [7]. One of the next major developments was the development of larger arrays sizes. In 2003 Santa Barbara Infrared (which had acquired the license for Honeywell's IRSP technology in 2001) presented 1024 $\times$ 1024 suspended membrane resistor arrays, both LWIR and mid-wave infrared (MWIR) [8], [9].

Historically, resistive arrays have been limited to simulating temperatures of around 700 K, and too low frame rates due to the device rise-time [10], [11]. Current research by Santa Barbara Infrared aims to overcome these barriers and reach frame rates up to 500 Hz and apparent temperatures over 1500 K. Results reported thus far are promising [12]. While resistive technologies continue to advance, researchers have explored alternative technologies, including those based on infrared light emitting diodes (IRLEDs). Early experiments with IRLED arrays suggested they are capable of achieving apparent temperatures over 1000 K, faster transition times than resistive elements, and high dynamic range [10], [13], [14].

The University of Delaware CMOS VLSI Optimization Research Group (CVORG) and a team at the University of Iowa have been working together to develop IRLED-based IRSPs for ten years. In 2008, members from these two groups and researchers from the Army Research Laboratories (ARL) presented the results of testing a 64 $\times$ 64 array of MWIR superlattice IRLEDs mounted to a driver ASIC device using flip-chip bonding [15]. In 2009, the same groups published the results of flip-chip bonding 68 $\times$ 68 MWIR LED array [16]. The results of these tests led to the fabrication of larger arrays, and in 2011, researchers from CVORG presented the design of the system to drive a 512 $\times$ 512 array, including a read-in integrated circuit (RIIC) and a customized dewar [17]. In 2013, researchers from the University of Iowa and CVORG demonstrated characteristics of the fabricated 512 $\times$ 512 SLEDs array, hybridized with the RIIC [18]. In 2016, these groups presented the results of incorporating at 512 $\times$ 512 array bonded to a RIIC and integrated with the entire projector system [19].

Since the presentation of the first SLEDs IRSP system, CVORG and the team at the University of Iowa have completed several versions of the projectors, collectively referred to as the SLEDs projectors. These projectors possess varying characteristics including resolution, frame rate, and pixel pitch, as shown in Table 1. Measurements of a Nightglow SLEDs (NSLEDs) array being formally evaluated showed that the array can achieve temperatures near 1350 K. Table 1 gives an overview of projectors currently in development. Figure 1 provides an overview of each SLEDs

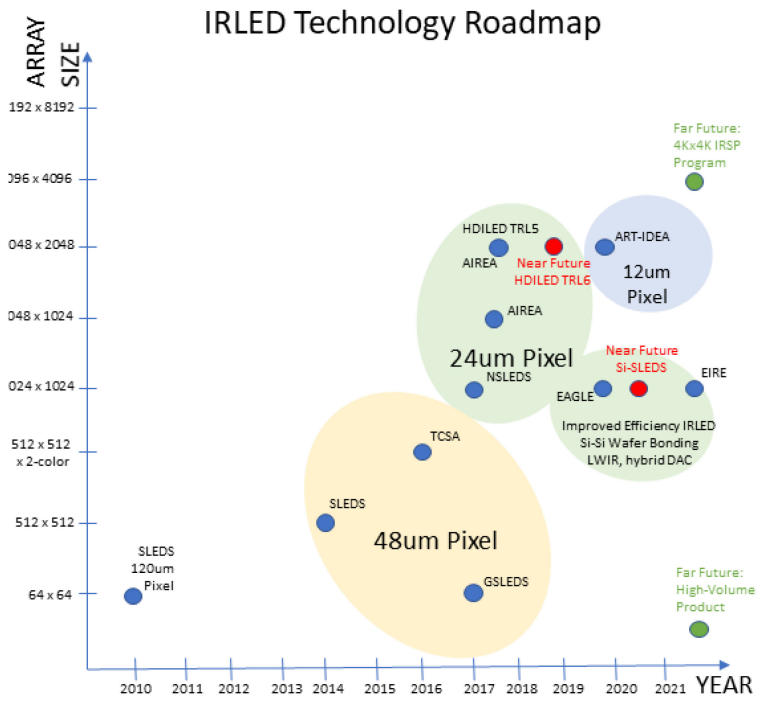

Fig. 1. IRLED technology roadmap including past and future projects.

projector from the first IRLED array all the way through proposed projects for the next two years. The rapid development of the SLEDs projectors has been enabled by the flexibility provided by various components of the entire projector system. These components and the features that provide this flexibility are the focus of the remainder of this paper.

Below, Fig. 2 shows how the SLEDs projectors are divided into five major components. All SLEDs projectors use the same basic structure and these components. Each component is explained in the following sections.

2.1 Hybrid

The hybrid comprises a RIIC and the IRLED array, bonded together. The University of Iowa grew the IRLED arrays (InAs/GaSb Type-II Superlattice arrays on n-Gas substrates) [18]–[20]. The RIICs are fabricated by ON Semiconductor using its C5 process. (This is a complimentary metal-oxide semiconductor, 0.5 μm, 3 metal process.) Hybridization is completed by Teledyne Scientific Co. using flip-chip bonding.

2.2 Dewar

The dewar houses the hybrid. As noted in [11], IRLEDs will generate waste heat which must be removed to maintain good performance, as electro-optical efficiency of the IRLEDs decreases as their temperature increases. For tests requiring cryogenic temperatures, the dewar is filled with liquid nitrogen to cool the array to 77 K [19].

2.3 Custom Support Electronics

The Custom support electronics (CSE) comprises several components, shown in Fig. 3. The CSE receives image data from the control PC, formats the data and generates appropriate analog signals

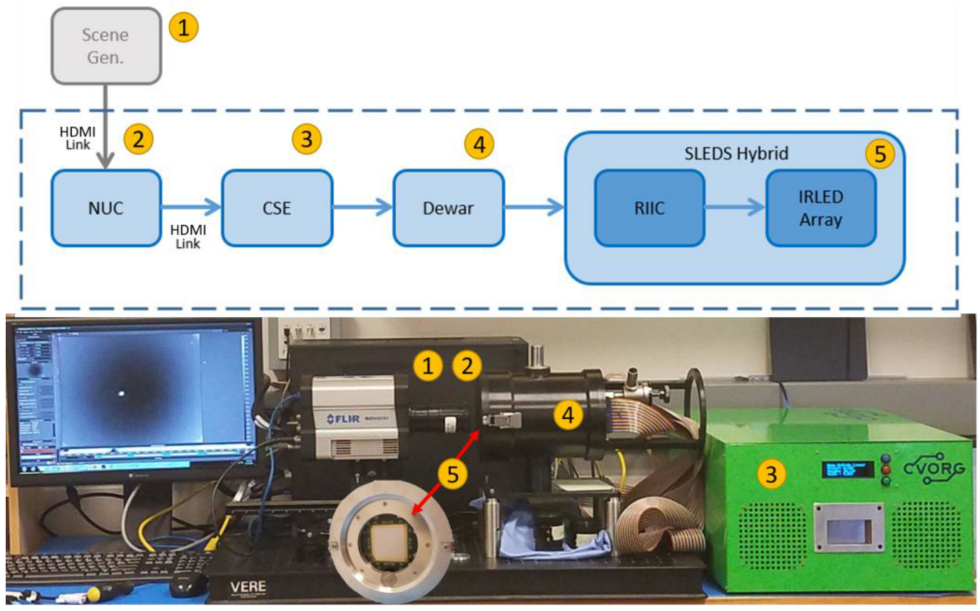

Fig. 2. SLEDs projector components. 1/2: Scene generation computer/NUC or control PC 3: Custom support electronics (CSE) 4: Dewar 5: Hybrid.

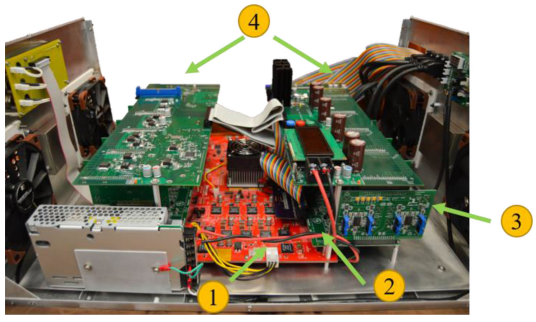

Fig. 3. Custom support electronics. 1: TB-6V-LX760-LSI board (main FPGA board) 2: Digital to analog converter cards 3. Amplifier board 4. Interface board. Not shown (at the back of the system) HDMI cards.

for driving the IRLEDs, as well as digital control signals for addressing and enabling pixels. Various controllers within the CSE also communicate with the user interface to provide system identification and configuration information and allow system settings to be changed easily.

2.3.1 HDMI Card: The data link between the control PC and the CSE is handled by two HDMI cables which split the control PC imagery in half as well as the bandwidth requirement on the link. In order to handle non-standard frame sizes and frame rates, a custom Zynq FPGA (Field-Programmable Gate Array) board was made to connect to the TB-6V-LX760-LSI inside the CSE. As depicted in Figure 4, this FMCL-ZYNQ-HDMI board is driven by a ZYNQ-7020 SoC, which in turn consists of a dual-core ARM Cortex-A9 processor core and a Xilinx Artix-7 FPGA. The firmware running on this ZYNQ SoC processes the data incoming from the control PC through the HDMI port, then sends this data out through the low pin-count FMC connector to the TB-6V-LX760-LSI. The ZYNQ firmware is fully configurable, capable of treating the HDMI ports as either inputs or outputs and handling different image resolutions and clock rates.

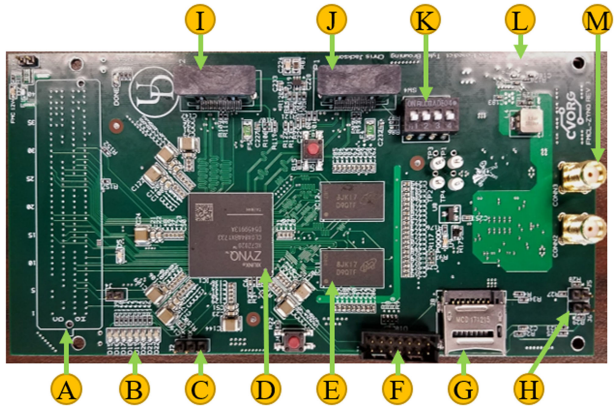

Fig. 4. FMC-ZYNQ-HDMI features: A. FMC B. LEDs C. UART D. Zynq7020 E. DDR F. JTAG G. SD H. Selectable boot mode jumpers I. HDMI J. HDMI K. Switches L. Flash M. SMA.

2.3.2 DAC Card: The DAC board is responsible for converting the digital value of the pixel into an analog current. Each CSE can support up to 8 DAC cards installed in 8 FMC slots of the TB-6V-LX760-LSI board. Each DAC card contains 2 × 16-bit AD9747 DAC chips which each support 2× DAC channels for a total of 4× channels per board and 32× channels per CSE.

2.3.3 Amplifier Board: The amplifier board is responsible for converting the analog current provided by the DAC card to an analog voltage from 0 V to 5 V and contains 4× transimpedance amplifiers per board. The CSE can support up to 8× amplifier boards per system. The voltage out of the amplifier board controls the LED brightness of the IRLED array in the dewar.

2.3.4 Interface Board: The interface board is responsible for providing a connection between all the CSEs DAC and amplifier boards to the RIIC in the dewar. There are 2× interface boards per CSE for the 2 sides of the TB-6V-LX760-LSI. The primary function of the interface board is to provide power to the DAC and amplifier boards as well as power monitoring via a microcontroller that monitors each voltage rail connected to the RIIC. This information is sent to a CPLD for display on the front of the CSE.

2.4 Control PC

The control PC used in the system provides test imagery for the array emitter. Output imagery is synchronized through a pulse sent by the IR camera. In the setup, scenes are preprocessed (non-real-time) for display in order to format output for the array emitter. The processing allows for modification of brightness and contrast through user input. Additionally, user-designed scenes can be generated to test specific array inputs such as grids, or other simple geometric figures and test patterns. All operations are done through a provided graphical user interface.

In terms of implementation, the UI is a layered implementation. At the top layer, the user interface is implemented using a combination of HTML, JavaScript, and Python. Below this, a service layer provides basic array functionality as shown in Figure 5. For example, camera control functionality and display driving functionality.

3. SLEDs System Design Approach

The design approach of the SLEDs system emphasizes flexibility. As with other computer systems, the speed of operation achieved through customization must be balanced against the need for rapid development. In the SLEDs system, the balance is achieved through modular hardware and scalable firmware. Components may be customized to achieve high performance and can be used for various projector systems with minimal modifications. The firmware can be configured at

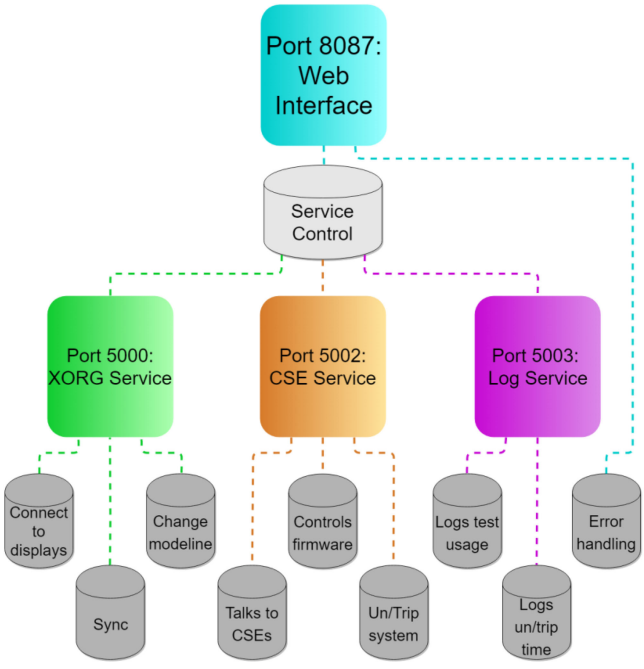

Fig. 5. Control PC service architecture.

TABLE 2
Projectors Interfaces and Compatibility

	TCSA	NSLED	HDILED
SLEDs Array	2-Color pixel 512x512 48um	1Kx1K 24um	2Kx2K 24um
# Analog Lines	128	128	128
# Digital Lines	64	64	64
# Address bit per quadrant	16	16	18
Load signal used	No	Yes	Yes
Serial Interface	Yes	Yes	Yes
# Configurable Registers	64	64	64
CSE Hardware	Compatible	Compatible	Compatible
CSE Firmware	Compatible	Compatible	Compatible
Cryo Package	Compatible	Compatible	Compatible
Synchronization	Compatible	Compatible	Compatible
CSE-to-RIIC Interface	Compatible	Compatible	Compatible
Scene Gen Interface	Compatible	Compatible	Compatible
Test Program GUI	Compatible	Compatible	Compatible
NUC	2-Color*	Compatible	Compatible
RIIC Chip	Custom	Custom	Custom

run-time to target a specific SLEDs system. Section 3.1 highlights the similarities and difference between different SLEDs projectors. Section 3.2 reviews the data-path and bandwidth requirements for the projector systems. Section 3.3 provides a design discussion of the firmware to run all SLEDs projector systems.

3.1 SLEDs Compatibility

The scalability of the system derives largely from the design of the RIIC itself. The interface of the RIICs for the TCSA, NSLED and HDILED systems are very similar, as illustrated in Table 2.

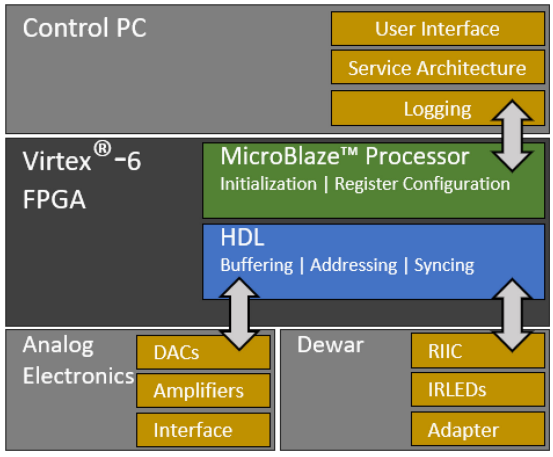

Fig. 6. The SNAP firmware runs on the Virtex-6 FPGA and interacts with the user interface, the analog electronics, and the RIIC.

This similarity facilitates the design of hardware and firmware to drive the arrays. The RIIC also supports modularity, through a set of configurations that allow up to sixteen analog channels to simultaneously drive adjacent pixels. The modularity of the RIIC is reflected in the design of the CSE analog hardware. A set of eight custom digital-to-analog (DAC) and amplifier boards drive the RIIC channels. These boards are interchangeable within and between systems and can be added or removed to support user requirements with the ability to drive 1 to 32 DAC channels. Finally, the flexibility of the RIIC and analog hardware is reflected in the design of the firmware that controls these components. Due to this similarity, a general purpose CSE can drive all the IRLED arrays. The minor differences between architectures are compensated for in the firmware design.

3.2 Projector Data-Path

The projector data-path consist of the link between the control PC and CSE. Currently, this link is handled by two HDMI cables which split the control PC imagery in half and transmit in column major order. To handle the custom frame sizes and frame rates a Zynq FPGA board was made with HDMI input and FMC output to connect to the TB-6V-LX760-LSI inside the CSE (refer to Section 2.3.1). For an HDILED array operating at 100 Hz, the bandwidth requirement per link becomes roughly 2.52Gb/s. Each HDMI port on the Zynq FPGA board can support a maximum rate of 4.95Gb/s for a total of 9.9Gb/s of available bandwidth per card and 19.8Gb/s per CSE. Supporting faster frame rates and larger resolution would require a multiple CSE solution where each CSE would be responsible for driving a single quadrant of the array.

3.3 Firmware Design

Based on requirements derived from the prior two sections, a firmware architecture called Snap was derived. At the hub of the CSE is a TB-6V-LX760-LSI board which is driven by a Xilinx Virtex-6 FPGA. The Snap architecture consists of two layers with various functions, as shown in Fig. 6.

HDL Layer: The foundation of the architecture comprises a set of modules defined with a Hardware-Description Language (HDL) which perform the essential functions of buffering, formatting and addressing. Figure 7 depicts the core of this architecture as follows:

Snap receives 2$\times$ high-definition multimedia interface (HDMI) data streams. These streams are buffered by 4 HDMI modules containing BRAMs for writing the data in on the HDMI clock and synchronizing reads out on the FPGA system clock. Each HDMI module holds 16 pixels at a time, but only 2 modules are written to at a time (alternating reads and writes). The HDMI module that

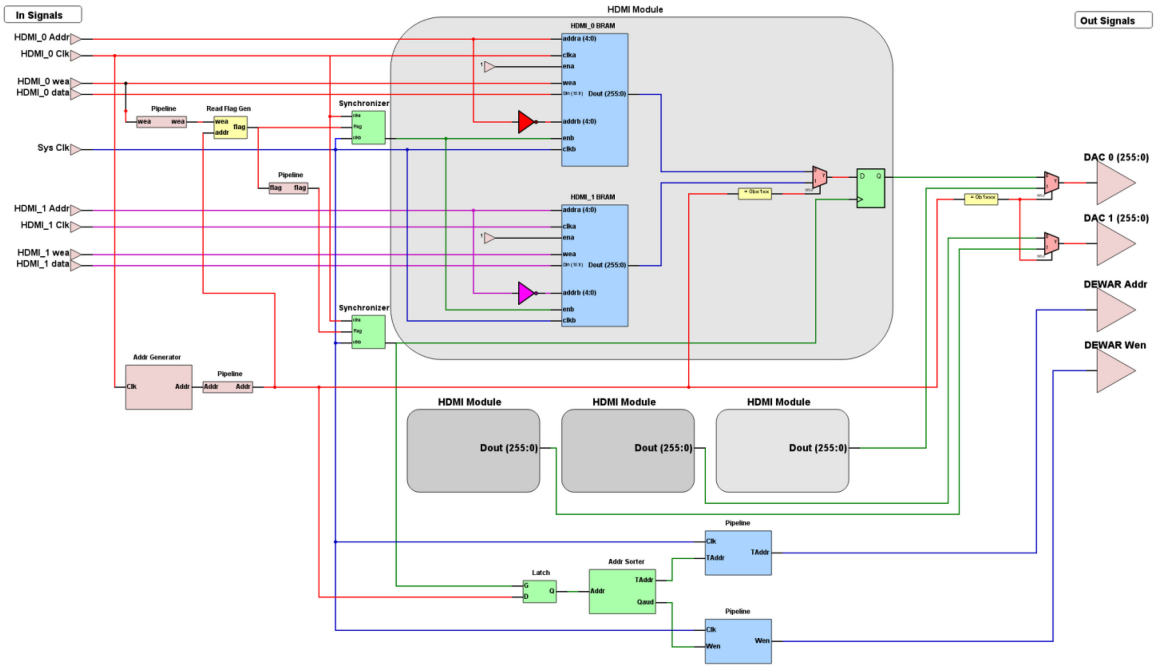

Fig. 7. The basic modules of the SNAP architecture for buffering pixel data. The incoming HDMI stream is split to 4 HDMI modules which handle buffering data from the HDMI clock domain to the FPGA system clock domain.

is written to is determined by the 4th bit of the incoming address. Internally, the HDMI module determines which BRAM buffer to read based on the 3rd bit of the address. The data read out of the BRAM buffer to the FPGA clock domain is then sent to a module for formatting.

After receiving data from the HDMI module, it is converted a 16-bit value and routed to the correct FMC slot depending on the address. The DAC signals are sent over the FMC to the DAC cards

The RIIC interface also expects relevant control signals and addressing values to be sent along with the data from the DAC cards. An addressing module is responsible for correctly delaying these signals to match the propagation delay of the data signals and changing address modes based on system parameters read in from the MicroBlaze layer.

MicroBlaze Layer: To support dynamic control and reconfiguration of various system parameters, the lower layer interacts with programs running on the Virtex-6 MicroBlaze: a soft-core processor. The portion of the system on the MicroBlaze largely acts as a bridge between the user interface and the hardware level.

The modules comprising the hardware-level design can be easily added, removed, or modified. The major blocks of the system are shown in Fig. 7. The design's modularity supports the rapid development of the projector system. Each of the modules is independently simulated and verified, reducing the amount of time necessary to debug the system as a whole. Individual modules can also be updated or altered for specific tests without necessarily requiring adjustments to other modules.

The SNAP architecture is also highly scalable, as additional functionality can be achieved simply by adding more modules to the system. SNAP can support various resolutions frame rates with minimal reconfiguration. The difference between various arrays is largely in addressing and buffering. Because of the way the RIIC handles addressing, NSLEDs and HDILEDs require twice as much buffering. To avoid exhausting the FPGA BRAMs, buffering is kept to a minimum, and data is read from buffers as soon as the next set of pixels to be written becomes available. The variations in addressing schemes are supported through parameters set at compile time. Scripts to set the

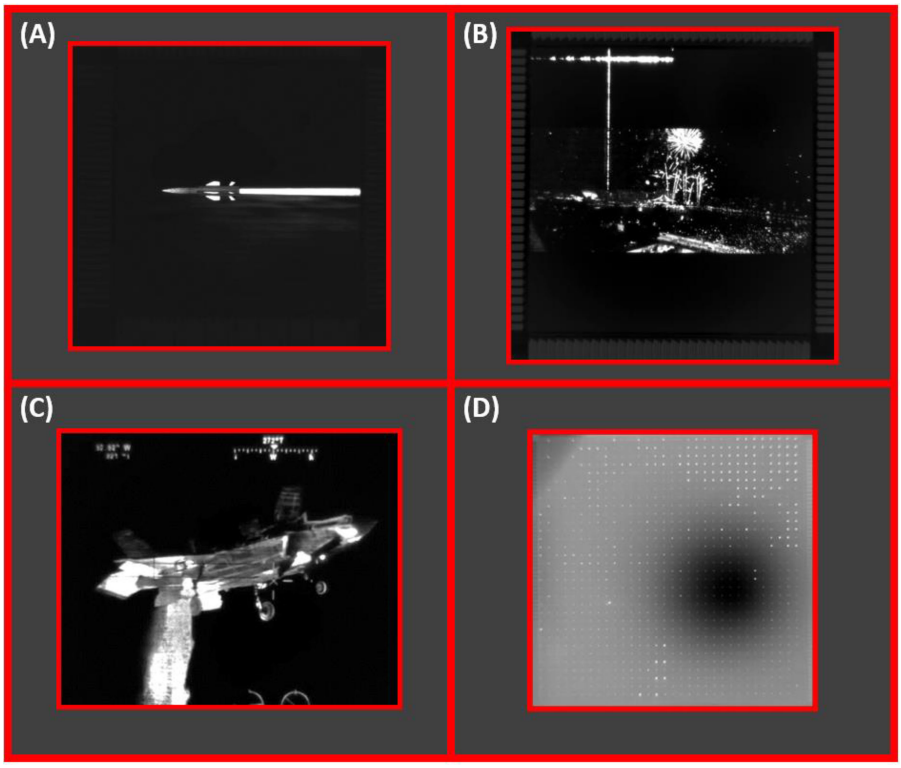

Fig. 8. Projector results. (a) Simulated rocket on NSLEDs (b) Fireworks on NSLEDs (c) F35 on NSLEDs (d) Grid on HDILEDs.

parameters and the system identification information are invoked by a custom make file in order to reduce the time and the possibility of error when creating new builds.

4. Projector Results

To date, this modular architecture has been used to drive a variety of SLEDs arrays from the size of 512 $\times$ 512 to 2048 $\times$ 2048 with plans to scale further in the near future. Figure 7 demonstrates some of the test imagery run on these systems. Figure 8(a) shows the apparent heat signature of a simulated missile from a scene projector displayed on an NSLEDs 1024 $\times$ 1024 array operating at room temperature at 100 Hz. Figure 8(b) shows fireworks displayed on an NSLEDs array operating at cryogenic temperature ($\sim$77 K) at 100 Hz with non-uniformity correction applied. Figure 8(c) displays an F35 jet on an NSLEDs array operating at 100 Hz and at 77 K. Figure 8(d) depicts a 64 $\times$ 64 marching grid on an HDILED array operating at room temperature. Grid patterns are used to measure the operability of an array's pixels for use in the NUC process.

5. Conclusion

The SLEDs projectors have developed rapidly, and in a little over ten years have reached array sizes, simulated temperature ranges, and frame rates that compete with those of resistive arrays. While this rate of progress reflects the demand that is also driving new achievements for resistive arrays, it has only been possible due to the flexibility of the supporting systems. The modular and scalable design approach of the SLEDs projectors has allowed devices and techniques developed for earlier projectors to be used for newer ones. This approach will continue to drive the progress of IRLED-based IRSPs and support HWIL testing of thermal imaging systems.

Aside from iterating on the current design, future SLEDs based projector systems will investigate driving IRLEDs via multiple CSEs. A new firmware architecture is also under development which will leverage a custom data transport protocol called PDP (Packetized Display Protocol) to eliminate the need for traditional fixed frame rate video standards such as DVI and HDMI and enable dynamic frame rates for subregions of the arrays [21].

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