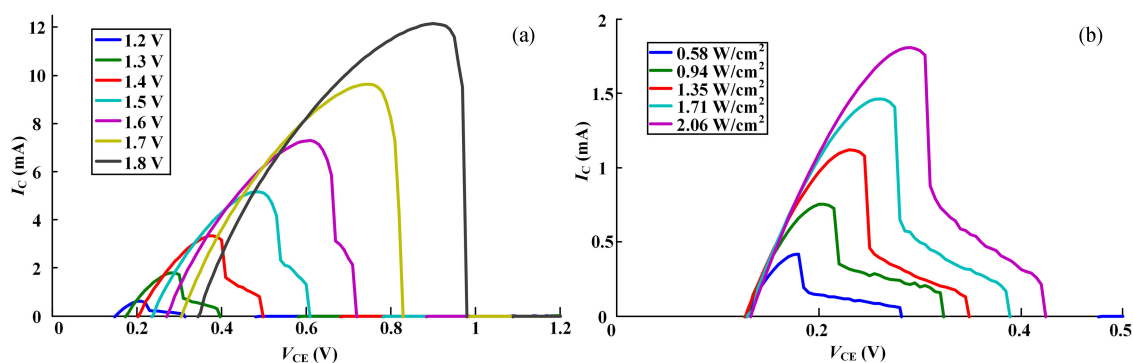


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Abstract: To prepare a desired negative differential resistance (NDR) device by standard complementary-metal-oxide-semiconductor (CMOS) process, a photoelectric dual control NDR device with a PNP bipolar-junction-transistor (BJT) and an NPN BJT was designed and fabricated by using the Si-base standard 0.18 μm CMOS process without any process modification and a special substrate. In order to reduce the valley current under optical control, a metal mask was added to the NDR device. The results show that the device exhibits good NDR characteristics under either voltage-control or photo-control. Under voltage-control, a low valley current (0.23 pA) and a high peak-to-valley current ratio (1.4×10^{10}) are obtained at less than 1 V. Under photo-control, the two parameters obtained at less than 0.5 V, are 37 nA and 4827, respectively. Also, the device displays fine S-type NDR characteristics and nice maintaining response function under photo-control. These superior photoelectric NDR characteristics endow the device with greatly potential application in the photoelectric logic circuits.

Index Terms: CMOS, negative differential resistance (NDR), peak-to-valley current ratio (PVCR), photoelectric devices, and optical switch.

1. Introduction

Negative differential resistance (NDR) devices have been applied in many analog and digital circuits owing to their unique folded current-voltage (I - V) characteristic which can greatly reduce the circuit complexity and largely enhance the circuit functionality [1]–[5]. However, for these NDR devices, there are two primary problems that have hindered their practical applications since the NDR characteristic was discovered by Esaki in 1958 [6]. One is that the NDR devices made by III-V materials are not compatible with standard complementary-metal-oxide-semiconductor (CMOS) process though the high peak-to-valley current ratio (PVCR) values usually appear in them. The other is that those silicon-compatible devices usually have PVCR values less than 10, which is not high enough for them in the practical applications [7].

To overcome the two problems, a great of effort has been made to improve the functions of NDR devices. For example, the enhanced surface generation method was exploited in SiGe-based

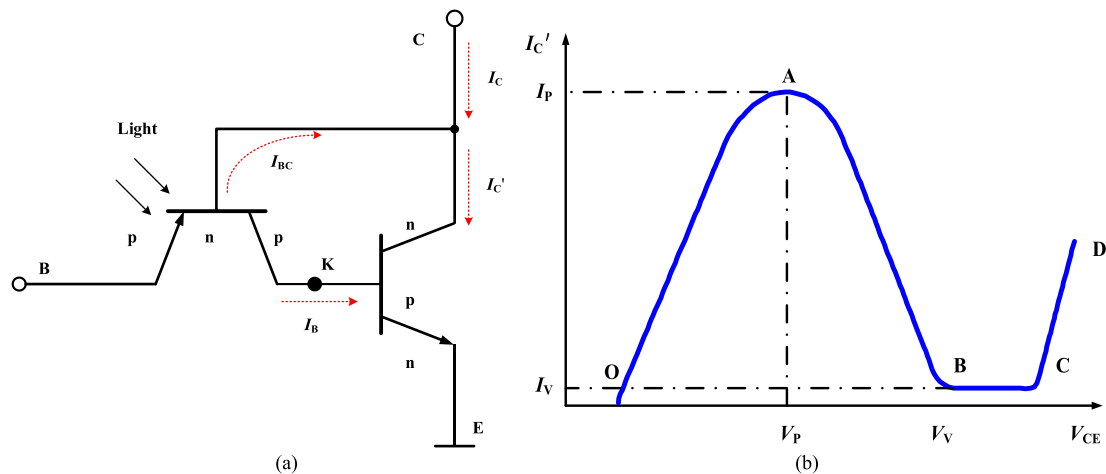


Fig. 1. (a) Equivalent circuit of NDR device. (b) $I_{C'}$ - V_{CE} characteristic of NDR device at a set V_{BE} .

gated diode and the PVCR was improved to 300 at 3 V [8], [9]. The breakdown mechanism of gated bipolar device in MOSFET structure was employed to cause PVCR increased to 1000 at 2.5 V [10], [11]. And the enhancement and depletion modes of MOSFET were used to prepare NDR device to increase PVCR to 10^7 at 1.6 V [12]. In these works, though the PVCR values are greatly increased, the operation voltages of them all are over 1.5 V, which will inevitably lead to great power consumption [8]–[12]. And then, some researches have been carried out to obtain high PVCR at relatively low operation voltage. Ever, a novel multiple-NDR device was obtained by combining tunnel diode with a conventional MOSFET, which caused PVCR exceed 10^6 at 1.0 V [7]. Moreover, when a simple PN diode was combined with silicon (Si) nanowire (NW) structure, then PVCR reached 10^4 at 1.0 V [13]. If the threshold voltage of conventional MOSFET was given a reasonable adjust, the ultra-high 1st and 2nd PVCR of multiple NDR device could be over 10^7 at less than 1.0 V [14].

In the aforesaid researches, the performance of NDR devices have been improved, and some of which achieve high PVCR at less than 1 V but are not compatible with standard CMOS processes. The main stream of ultra-large-scale integration (ULSI) still is standard Si-based CMOS or SiGe-based BiCMOS process. Therefore, NDR devices are expected to have an ultra-high PVCR at low voltages and be compatible with standard integrated circuit processes. Then an idea is conceived to prepare the desired NDR devices by combining standard CMOS process with photoelectric technology, based on our previous research work [15]. As a result, a photoelectric dual control NDR device is prepared by using the UMC 0.18 μm standard CMOS process. To the best of our knowledge, up to now, no photoelectron NDR device compatible with standard CMOS process has been developed.

Interestingly, the obtained NDR device not only has high PVCR at less than 1 V under voltage-control, but also shows good NDR characteristics at less than 0.5 V under photo-control. And the peak current voltage (V_P), peak current (I_P), PVCR and negative resistance (R_N , resistance in negative current region) can be conveniently modulated by adjusting the third-terminal bias voltage or light intensity. Moreover, the device can be developed into an irreversible optical switching with fine S-type NDR characteristics and nice maintaining response function.

2. The Device Structure and Operation Principle

2.1 Device Structure

The equivalent circuit of device is shown in Fig. 1(a) in which a PNP Bipolar-Junction-Transistor (BJT) works as the feedback transistor and an NPN BJT works as a master transistor. The three terminals of device are marked as base (B), collector (C) and emitter (E), respectively. And the

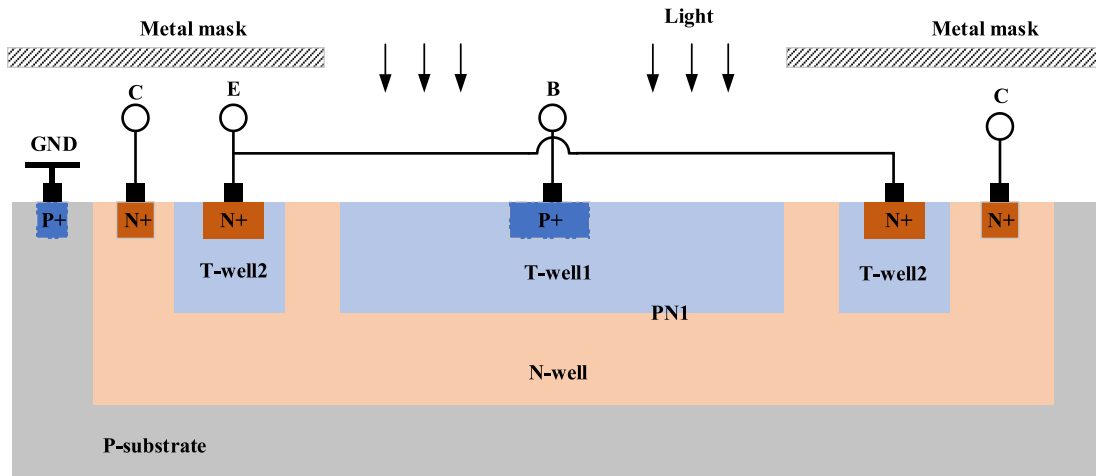


Fig. 2. Basic structure of NDR device.

emitter of PNP BJT is used as B, the collector of NPN BJT connected to the base of the PNP BJT is used as C, and the emitter of NPN BJT is used as E.

The basic structure of NDR device is shown in Fig. 2 in which the lateral PNP BJT is constituted of T-well1/N-well/T-well2 and the vertical NPN BJT is constituted of N+/T-well2/N-well. T-well is a p-type doped shallow well in UMC 0.18 μm process. The T-well2 works both as the collector of PNP BJT and as the base of NPN BJT for further saving the device area. The T-well1 has a relatively large area to absorb enough light energy. And the metal mask was added over T-well2 to reduce the valley current under photo-control.

2.2 Operation Principle

When the device works under voltage-control, no light illuminates on the surface of device. The B-E inter-voltage (V_{BE}) of the NDR device is fixed at a positive bias voltage that enables the PN1 junction (PN junction formed by T-well1 and N-well) to be turned on, the E point is grounding and the C-E inter-voltage (V_{CE}) is set at a changing positive bias voltage increased from 0 V. When V_{BE} is given, holes inject from the emitter junction of PNP into N-well region. Some of holes in N-well region are collected by C electrode due to $V_{BE} > V_{CE}$, and the others are diffused to the depletion region of PNP BJT collector junction to produce I_B . When V_{CE} is very small, the emitter junction voltage of PNP BJT V_{BC} ($V_{BE} - V_{CE}$) is large and then the collector current also is large. Thus, NPN BJT works in saturation region because of a small V_{CE} and a large base current (I_B , being equal to the collector current of PNP BJT). As V_{CE} increases, the electrons collected by C increases, that is, I_C' increases, as shown in OA section of Fig. 1(b). With the further increase of V_{CE} , I_B decreases for the decreases of V_{BC} , which will result in NPN BJT working in active region. At this point, $I_C' = \beta I_B$ in which β is the magnification coefficient of NPN BJT far greater than 1. Then I_C' decreases with the decrease of I_B , which makes the $I_C - V_{CE}$ curve appear NDR region, as shown in AB section of Fig. 1(b). As V_{CE} continues to increase, NDR device will work in cut-off region, because of PNP BJT being cut-off (V_{BC} is not enough to turn the PN junction on), as shown in BC section of the Fig. 1(b). When V_{CE} is larger than the breakdown voltage of NPN BJT, the device will work in a breakdown region, e.g., CD section.

When the device works under photo-control, T-well1 region is illuminated by light and the base of the NDR device is open. Light injection, instead of current injection, results in a photo-generated voltage appearing between B and E, which can turn on NPN BJT. Then the photocurrent of NPN BJT will cause a positive feedback to the base of PNP BJT. When V_{CE} is set as a changing positive

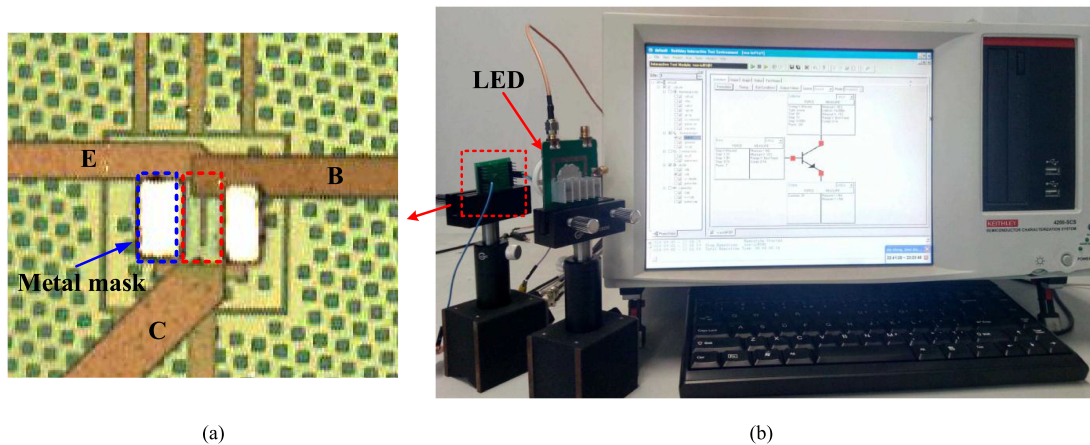


Fig. 3. (a) Microphotograph of the NDR device. (b) Test system of I_C - V_{CE} characteristic.

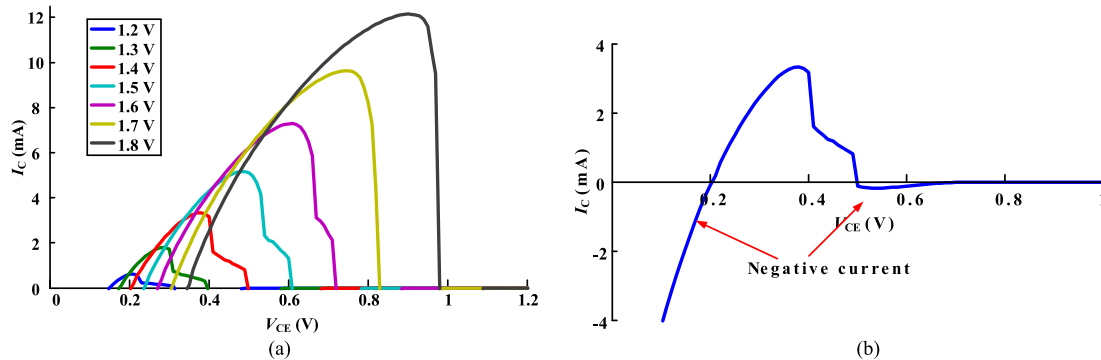


Fig. 4. (a) I_C - V_{CE} curve of NDR device when V_{BE} altered from 1.2 to 1.8 V 0.1 V per step. (b) I_C - V_{CE} characteristic of NDR device measured when V_{BE} set at 1.4 V.

bias voltage increased from 0 V as mentioned above, the change regulation of I_C - V_{CE} curve is similar to the one under voltage-control in Fig. 1(b).

3. Experimental Results and Analysis

The photomicrograph of device ($25 \mu\text{m} \times 16 \mu\text{m}$) is shown in Fig. 3(a) in which the areas framed by red and blue dotted lines are the light-absorbed region T-well1 ($12.7 \mu\text{m} \times 9 \mu\text{m}$) and the metal mask over T-well2 ($12.7 \mu\text{m} \times 3 \mu\text{m}$), respectively. And the typical I_C - V_{CE} characteristic curves of NDR device under either voltage-control or photo-control are measured by a Keithley 4200-SCS parameter analyzer [see Fig. 3(b)], at room temperature.

3.1 Characteristics of Device Under Voltage-Control

Under voltage-control, it was found that no NDR characteristics appear when V_{BE} is less than 1.2 V. This is because that the voltage drops on PN1 cannot turn it on when V_{BE} is less than 1.2 V. Once $V_{BE} > 1.2$ V, as V_{CE} increases from 0 V, I_C increases firstly to a peak value and then decreases, which just is a fine NDR characteristic of the device, and also the I_P , PVCR and R_N values all are changed, once V_{BE} altered [see Fig. 4(a)]. Moreover, for each I_C - V_{CE} curve, there are two negative currents appeared in two corresponding voltage regions. Here the curve gotten at $V_{BE} = 1.4$ V is taken as a representative to show the current changing characteristics [see Fig. 4(b)]. It is obvious that a negative current value gradually decreases and then change to a positive current before

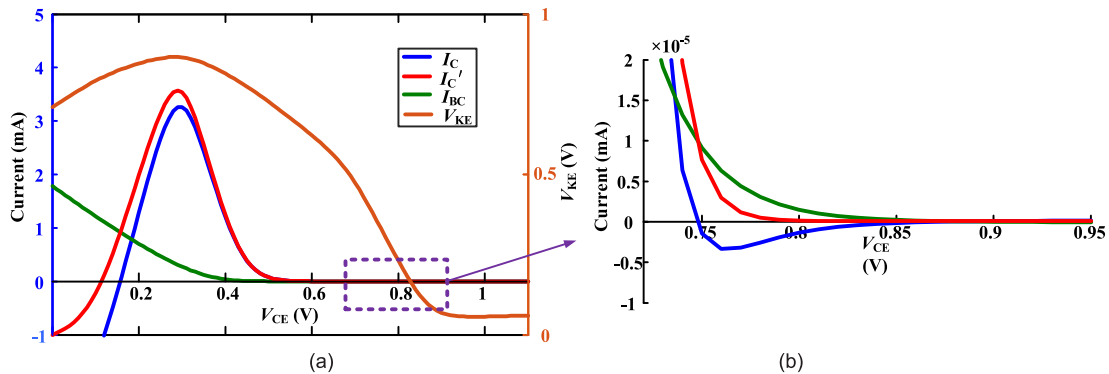


Fig. 5. (a) Curves of I_{BC} , I_C , I_C' and V_{KE} changed with V_{CE} when V_{BE} is set at 1.4 V. (b) Curves of I_{BC} , I_C , I_C' changed with V_{CE} when the second negative current existed.

$V_{CE} = 0.2$ V, and another negative current value increases firstly and then decreases after $V_{CE} = 0.5$ V. A similar phenomenon has been reported in the literature [16], but the detail explanation was not given.

For better understanding the mechanism of current changing with voltage, the equivalent circuit in Fig. 1(a) was simulated by Spectre. When V_{BE} is set at 1.4 V, the curves of I_{BC} , I_C , I_C' and V_{KE} (the voltage value of K point) changes with V_{CE} is shown in Fig. 5(a)]. All curves are slightly different from the measured curves, because of process differences. It is found that V_{KE} increases firstly and then decreases until V_{KE} is finally stable at a lower voltage value, along with the increase of V_{CE} . And its highest point and the peak of I_C (I_P) appear at the same time (when $V_{CE} = V_P$). This is because that, before V_{CE} over V_P , NPN BJT works in the saturation region because of the small V_{CE} and the large I_B , which makes V_{KE} increase. And differently, once V_{CE} over V_P , NPN BJT works in the active region and the base carriers are released, which causes V_{KE} decrease. In addition, V_{KE} is always higher than V_{CE} before I_C drops to nearly 0 A, which makes PNP BJT always work in saturated region.

The current direction shown in Fig. 1(a) is considered to be the positive direction. Based on the analysis above, the reason for generation of negative current can be understood as follow. The first negative current I_C is measured when V_{CE} is no more than 0.2 V [see Fig. 4(b)]. At this time, I_C' is a negative current because $V_{KE} > V_{CE}$, and I_{BC} is a positive current because $V_{BE} > V_{CE}$. I_C can be written as $I_C = I_C' - I_{BC}$. So, the first negative I_C is detected. Nevertheless, with the increase of V_{CE} , I_C' gradually changes from negative to positive value and subsequently further increases, and contrarily I_{BC} decreases for decrease of V_{BC} . Therefore, the detected negative I_C value continuously decreases down to 0 A and then changes into positive value [see Fig. 5(a)].

The second negative I_C is recorded when $V_{CE} > 0.50$ V. As mentioned above, when $V_{CE} > V_P$, NPN BJT work in active region and PNP BJT still work in saturation region. Under this circumstance, both I_B and I_{BC} decrease as V_{CE} increases and I_B is not controlled by I_{BC} . On the other hand, I_C' descends faster for that there is an equivalence relationship $I_C' = \beta I_B$. Also, when the second negative current appear, the relationship among I_C , I_C' , and I_{BC} can be intuitively seen in Fig. 5(b), in which I_C' drops faster than I_{BC} and then both of their downward trends slow down. This is because with the increase of V_{CE} , PNP BJT gradually enters the cut-off region. It also can be seen that the curves of I_{BC} and I_C' have two intersections. This leads to the appearance of negative current I_C and the value of negative current I_C increases first and then decreases. Therefore, 0 A I_C appeared twice [see Fig. 4(b)]. And the measured I_C - V_{CE} curve surely passes through the X axis for two times [see Fig. 4(b)]. In summary, according to the analysis above, the value of I_C can be equal to 0 A, because $I_C = I_C' - I_{BC}$. That is, theoretically, the NDR device has a low valley current of 0 A and a high PVCR of infinity. Valley current appears when the NDR device just enters the cut-off region. At this point, the value of V_{CE} is valley current voltage (V_V), $V_{BC}' = V_{BE} - V_V$, in which V_{BC}' (about

TABLE 1
NDR Characteristics of Device at Different Base Voltages

$V_{BE}(V)$	$I_p(mA)$	$I_V(\mu A)$	PVCR
1.2	0.62	0.06	1.0×10^{10}
1.4	3.33	0.23	1.4×10^{10}
1.6	7.29	0.92	7.9×10^9
1.8	12.1	18.06	6.7×10^8

0.65 V in simulation) is positive voltage but not enough to turn PN1 on. That is to say, if the V_{BE} is small, V_V will be smaller, thus the NDR characteristics can be obtained at a lower voltage.

However, the 0 A I_C is not directly gotten in practical test due to the rapid change from positive current to negative current and the accuracy of instrument. For all that, there is a large PVCR revealed by the measured data. For example, when V_{BE} is 1.4 V, there are $I_p = 3.33$ mA, $I_V = 0.23$ μ A, and PVCR = 1.4×10^{10} . The PVCR is higher than those previously reported results [7], [12]–[14]. The ultra-low I_V and the ultra-high PVCR still exist under other V_{BE} values (see Table 1), which is greatly significant for NDR devices in improvement of logic circuits [17].

3.2 Characteristics of Device Under Photo-Control

The photoelectronic NDR devices can sensitively convert optical signals into electrical signals and output NDR characteristics, which can be used as photoelectric switches [18], optical frequency modulation [16], optical oscillation [19], and optical bistability [20], [21]. So, instead of electro-injection, visible light was injected into the base of NDR device to produce NDR characteristics. The employed light source is white light-emitting diode (LED), which is mainly used for visible light communication (VLC). And the VLC technology is an emerging technology applied in high-speed and short-range wireless communication, in virtue of the advantages such as high security, immunity to radio frequency interference, worldwide availability and unlicensed bandwidth [22]–[24]. However, the NDR phenomenon did not appear while only light illuminated on the device. It was speculated that the light intensity (I) of LED was not high enough, and the chip was too small to receive enough light energy, thus, a large photo-generated voltage was not formed at the base. Therefore, a small voltage V_{BE} was biased to assist light to generate an enough high voltage.

It was found that, if V_{BE} less than 1 V, illumination could not cause NDR to generate. However, when V_{BE} was bigger than 1 V and smaller than the NDR turn-on voltage (1.2 V), a fine NDR phenomenon could be induced by external LED light. The I_C - V_{CE} characteristic curves of NDR device, when V_{BE} at a value of 1–1.1 V and light intensity at $2 \text{ W}\cdot\text{cm}^{-2}$, could be observed [see Fig. 6(a)]. It was obvious that these curves exhibited desired NDR characteristics. For example, when V_{BE} was set at 1.08 V, there were $I_p = 1.81$ mA, $I_V = 37$ nA and PVCR = 4827, which is better than other reported photoelectric NDR devices [19]–[21], [25], [26]. If the base was biased at a voltage between 1 V to 1.1 V and no illumination was given, the I_C - V_{CE} curve had not NDR characteristics [see Fig. 6(b)], which meant that it was critical for light illumination on the device to generate the aforesaid NDR characteristics.

In addition to V_{BE} , the light intensity also effects the characteristic of NDR device. The obtained I_C - V_{CE} characteristic curves of NDR device show that both of I_p and V_P increase with the increase of light intensity at $V_{BE} = 1.08$ V, which is similar to the impact of V_{BE} on them (see Fig. 7). In terms of the effect of V_{BE} and light intensity on I_C - V_{CE} curves, the NDR characteristics of device appear when V_{CE} is less than 0.5 V (see Figs. 6(a) and 7).

Here the I_V values are lower than those behaved by reported photoelectric NDR devices [16], [19]–[21], which is benefited from the metal mask above T-well2. The metal mask can effectively shield light illumination on the base of NPN BJT to avoid photocurrent generation, so as to reduce the valley current. More precisely, if there is no metal mask, external light will illuminate on T-well2

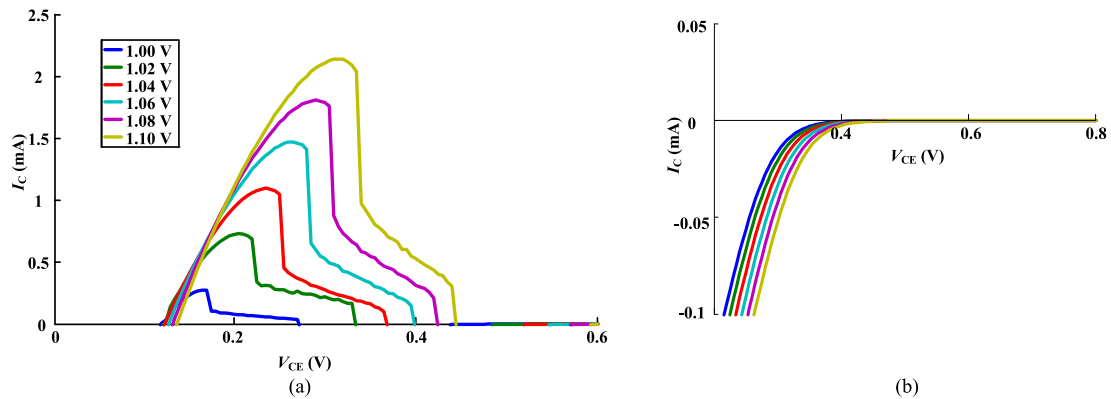


Fig. 6. (a) I_C - V_{CE} curves of NDR device when V_{BE} is set at a value of 1–1.1 V and light intensity at $2 \text{ W}\cdot\text{cm}^{-2}$. (b) I_C - V_{CE} curves of NDR device when V_{BE} is set at a value of 1–1.1 V and no illumination was given.

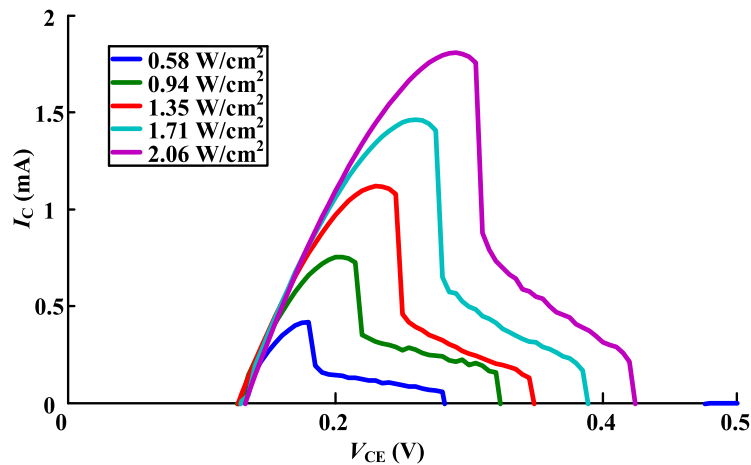


Fig. 7. I_C - V_{CE} curves of NDR device under different light intensities when V_{BE} is set at 1.08 V.

region and excite an optical-generated voltage, which always exists in the device. That is to say, even though the V_{CE} is biased at the V_V , still there is a photo-generated voltage existed in NPN BJT base, resulting in that NPN BJT can't be completely turned off and a larger valley current exists for that NPN BJT can't be completely turned off. Obviously, the metal mask can effectively reduce I_V of NDR device.

Table 2 shows performance summary of the proposed NDR device and comparison with other voltage-control or photo-control NDR devices recently reported. Whether under voltage-control or photo-control, the proposed NDR device shows higher PVCR and lower I_V than the other NDR devices.

3.3 S-Type NDR Characteristics of Device Under Photo-Control

Further, the device also has S-type NDR characteristics of I_{BE} - V_{BE} curves under photo-control. The diagram of test circuit is shown in Fig. 8(a) in which the B pole is connected to the power supply V_B through a resistance R_B and an ammeter, and the C pole is connected to the power supply V_C via a resistance R_C . The initial test conditions were set as R_C at $1 \text{ K}\Omega$, R_B at 150Ω , and V_{CE} at 1.8 V . Then V_{BE} was altered from 0 V to the critical voltage 2.6 V at which, instead of V_{BE} continually increased, the intensity of light illuminated on T-well2 was increased from 0 to $110 \text{ mW}\cdot\text{cm}^{-2}$. When the light

TABLE 2
Performance Summary and Comparison With Other NDR Devices

		[7]	[12]	[14]	[20]	[21]	[26]	This work
Process		CMOS	0.09- μm Standard CMOS	CMOS	GaAs-Base	InP-base	a	0.18- μm Standard CMOS
voltage-control	V_V	<1 V	>1.5 V	<1 V	N.A.			<1 V
	$I_V(\text{A})$	1.4×10^{-12}	N.A.	3.71×10^{-13}	N.A.			2.3×10^{-13}
	PVCR	1.3×10^6	4×10^7	1.16×10^8	N.A.			1.4×10^{10}
photo-control	V_V	N.A.			1.13	<0.5 V	3 V	<0.5 V
	$I_V(\text{A})$	N.A.			8.39×10^{-2}	7.2×10^{-3}	N.A.	3.7×10^{-8}
	$I_P(\text{A})$	N.A.			1.69×10^{-1}	2.44×10^{-2}	N.A.	1.81×10^{-3}
	PVCR	N.A.			2.01	3.39	1.85	4827

*a: MEH-PPV decorated electro spun TiO_2 mat.

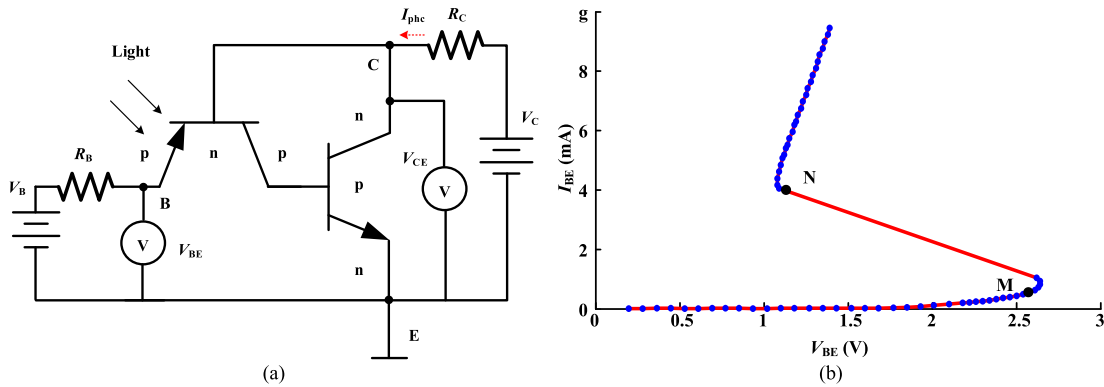


Fig. 8. (a) Equivalent circuit for testing the S-type NDR characteristic of NDR device. (b) I_{BE} - V_{BE} curve obtained under the conditions of $R_C = 1 \text{ K}\Omega$, $R_B = 150 \Omega$, and $V_C = 1.8 \text{ V}$.

intensity was less than $51.5 \text{ mW}\cdot\text{cm}^{-2}$, the NDR device was in a high resistance state, i.e., M point of I_{BE} - V_{BE} curve in Fig. 8(b). Once the light intensity reached at $51.5 \text{ mW}\cdot\text{cm}^{-2}$, Instantaneously I_{BE} increased to 4 mA and V_{BE} downed to 1.2 V, i.e., N point of I_{BE} - V_{BE} curve in Fig. 8(b). The suddenly changed MN section in I_{BE} - V_{BE} curve can be comprehended as follow. Under the set conditions of V_{CE} at a certain value V_{CE0} , e.g., 1.8 V, and V_{BE} at a critical voltage V_{BE0} , e.g., 2.6 V, the NDR device is in a high resistance state if there is not illumination. While the NDR device is illuminated, an additional photo-generated voltage appears in PN1 junction, which leads to holes accumulated in T-well2 region and correspondingly reduces the barrier of electron injection into T-well2 region. Therefore, an additional photo-generated current I_{phc} generates, which passes through R_C and brings V_{CE} with a voltage drop. V_{CE} will change from V_{CE0} to V_{CE1} , which can be expressed as (1).

$$V_{CE1} = V_{CE0} - I_{phc}R_C \quad (1)$$

It can be seen that, the stronger an illumination is given, the larger I_{phc} becomes, and also the smaller V_{CE1} becomes. When the light intensity exceeds a critical value, e.g., $51.5 \text{ mW}\cdot\text{cm}^{-2}$, V_{CE1} is small enough to result in $V_{BE0} > V_{BE1}$, and then the device jumps to a low resistance state. V_{BE1} can be expressed by V_{CE1} and V_f , written as (2) [27], in which V_f is a positive PN junction voltage drop.

$$V_{BE1} = V_{CE1} - V_f \quad (2)$$

After the device jumps to a low resistance state, the state always remains (V_{CE} and V_{BE} change slightly), no matter how the light intensity is changed unless the light intensity drops to $0 \text{ mW}\cdot\text{cm}^{-2}$.

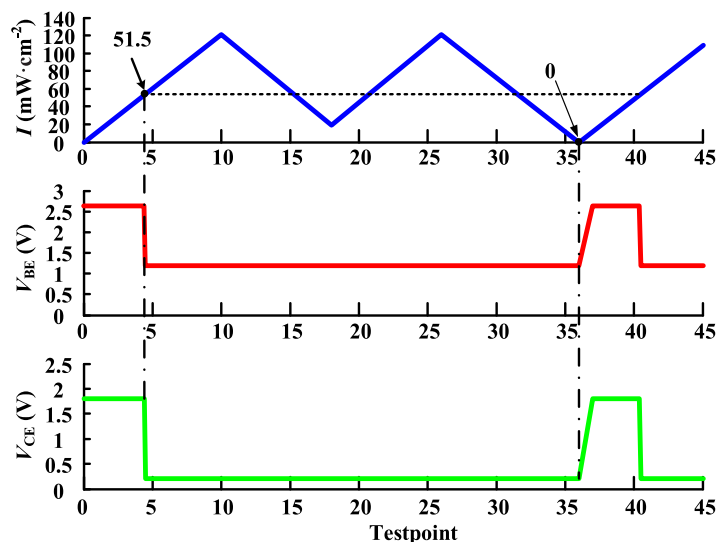


Fig. 9. Change of V_{CE} and V_{BE} with light intensity (I).

From Fig. 9, it is observed that V_{BE} does not change with light intensity after light intensity firstly exceeds $51.5 \text{ mW}\cdot\text{cm}^{-2}$, until the light intensity reaches $0 \text{ mW}\cdot\text{cm}^{-2}$. Once the light intensity drops to $0 \text{ mW}\cdot\text{cm}^{-2}$, the device restores to the high resistance state. That is to say, the NDR device has the function of maintaining response, which is very significant for the design of irreversible photo-controlled current switching.

4. Conclusion

To develop a standard CMOS-compatible NDR device with high PVCR at low voltage, an NDR device was designed and fabricated in $0.18 \mu\text{m}$ standard CMOS process. In the device, the number of transistors in typical logic circuits is reduced to two, which dramatically decreases the area occupied by circuits. It is tested and found that the device exhibits fine NDR characteristics under either voltage-control or photo-control. Under voltage-control, an I_V of 0 A and a PVCR of infinity can be obtained theoretically, and an ultra-low I_V (0.23 pA) and an ultra-high PVCR (1.4×10^{10}) was measured below 1 V . Under photo-control, a low valley current (37 nA) and a higher PVCR (4827) are obtained at less than 0.5 V . The I_P , V_P and R_N can be effectively controlled by voltage V_{BE} or external light intensity. For application, an irreversible optical switch is designed and studied, which display fine S-type NDR characteristics and nice maintaining response function. In sum, the device is well compatible with standard CMOS technology, for which it will have greatly potential in logic circuits. In addition, the device also has fine photoelectric characteristics, which will make it have broad application prospect in the integration process of VLC systems.

References

- [1] P. Sharma, L. Syavoch Bernard, A. Bazigos, A. Magrez, and A. M. Ionescu, "Graphene negative differential resistance circuit with voltage-tunable high performance at room temperature," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 865–867, Aug. 2015.
- [2] H. Agarwal *et al.*, "Engineering negative differential resistance in NCFETs for analog applications," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 2033–2039, May 2018.
- [3] J. Núñez, M. J. Avedillo, and J. M. Quintana, "Novel pipeline architectures based on negative differential resistance devices," *Microelectron. J.*, vol. 44, no. 9, pp. 807–813, 2013.
- [4] K. Maezawa and M. Mori, "Possibilities of large voltage swing hard-type oscillators based on series-connected resonant tunneling diodes," *IEICE Trans. Electron.*, vol. E101.C, no. 5, pp. 305–310, 2018.

- [5] K.-J. Gan, C.-H. Huang, W.-K. Yeh, C.-Y. Guo, and J.-J. Lu, "Design of multi-threshold threshold gate using MOS-NDR circuits suitable for CMOS process," *Analog Integr. Circuits Signal Process.*, vol. 96, no. 3, pp. 409–416, 2018.
- [6] L. Esaki, "New phenomenon in narrow germanium-p-n junctions," *Phys. Rev.*, vol. 109, no. 2, pp. 603–604, 1958.
- [7] S. Shin and K. R. Kim, "Multiple negative differential resistance devices with ultra-high peak-to-valley current ratio for practical multi-valued logic and memory applications," *Jpn. J. Appl. Phys.*, vol. 54, no. 6S1, 2015, Art. no. 06FG07.
- [8] B. M. Wilamowski and F. M. Long, "Negative resistance element for a static memory cell based on enhanced surface generation (MOS devices)," *IEEE Electron Device Lett.*, vol. 11, no. 10, pp. 451–453, Oct. 1990.
- [9] Y. Liang, K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "From DRAM to SRAM with a novel sign-based negative differential resistance (NDR) device," in *Proc. Int. Conf. IEEE Electron Devices*, 2005, pp. 959–962.
- [10] R. Duane, A. Mathewson, and A. Concannon, "Bistable gated bipolar device," *IEEE Electron Device Lett.*, vol. 24, no. 10, pp. 661–663, Oct. 2003.
- [11] C. Xu and R. Duan, "A comprehensive study of bistable gated bipolar device," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2589–2597, Oct. 2006.
- [12] S.-L. Chen, P. B. Griffin, and J. D. Plummer, "Negative differential resistance circuit design and memory applications," *IEEE Trans. Electron Devices*, vol. 56, no. 4, pp. 634–640, Apr. 2009.
- [13] S. Shin, W. R. Min, and K. R. Kim, "Negative differential resistance devices with ultra-high peak-to-valley current ratio based on silicon nanowire structure," in *Proc. Int. Conf. IEEE Silicon Nanoelectron.*, 2012, pp. 1–2.
- [14] J. W. Jeong, E. S. Jang, S. Shin, and K. R. Kim, "Multiple negative differential resistance device by using the ambipolar behavior of tunneling field effect transistor with fast switching characteristics," *J. Nanosci. Nanotechnol.*, vol. 16, no. 5, pp. 4753–4757, 2016.
- [15] K. Xia, S. Li, L. Dan, Y. Zheng, L. Mao, and W. Guo, "Principle of photoelectric dual base transistor," *Chin. J. Semicond.*, vol. 24, no. 8, pp. 850–855, 2003.
- [16] W. Guo *et al.*, "An InGaP/GaAs negative differential resistance heterojunction bipolar transistor with a new structure," *Chin. J. Semicond.*, vol. 26, no. 9, pp. 1783–1788, 2005.
- [17] R. Duschl, O. G. Schmidt, G. Reitemann, and E. Kasper, "High room temperature peak-to-valley current ratio in Si based Esaki diodes," *Electron. Lett.*, vol. 35, no. 13, pp. 1111–1112, 1999.
- [18] E. R. Cardozo de Oliveira *et al.*, "Electroluminescence on-off ratio control of n-i-n GaAs/AlGaAs-based resonant tunneling structures," *Phys. Rev. B*, vol. 98, no. 7, 2018, Art. no. 075302.
- [19] B. Romeira, J. Javaloyes, J. M. L. Figueiredo, C. N. Ironside, H. I. Cantu, and A. E. Kelly, "Delayed feedback dynamics of Liénard-type resonant tunneling-photo-detector optoelectronic oscillators," *IEEE J. Quantum Electron.*, vol. 49, no. 1, pp. 31–42, Jan. 2013.
- [20] J. Mi *et al.*, "A GaAs-based hybrid integration of a tunneling diode and a 1060-nm semiconductor laser," *IEEE Photon. Technol. Lett.*, vol. 27, no. 2, pp. 169–172, Jan. 2015.
- [21] Y.-J. Li *et al.*, "Electrically and optically bistable operation in an integration of a 1310 nm DFB laser and a tunneling diode," *Chin. Phys. Lett.*, vol. 35, no. 4, 2018, Art. no. 044202.
- [22] Y. Wang, L. Tao, X. Huang, J. Shi, and N. Chi, "8-Gb/s RGBY LED-based WDM VLC system employing high-order CAP modulation and hybrid post equalizer," *IEEE Photon. J.*, vol. 7, no. 6, Dec. 2015, Art. no. 7904507.
- [23] Y. Wang, J. Yu, and N. Chi, "Demonstration of 4×128 -Gb/s DFT-S OFDM signal transmission over 320-km SMF with IM/DD," *IEEE Photon. J.*, vol. 8, no. 2, Apr. 2016, Art. no. 7903209.
- [24] X. Huang *et al.*, "2.0-Gb/s visible light link based on adaptive bit allocation OFDM of a single phosphorescent white LED," *IEEE Photon. J.*, vol. 7, no. 5, Oct. 2017, Art. no. 7904008.
- [25] K. W. Lee *et al.*, "Light-induced negative differential resistance in graphene/Si-quantum-dot tunneling diodes," *Sci. Rep.*, vol. 6, Jul. 2016, Art. no. 30669.
- [26] K. Mohanta, M. Karthega, and S. K. Batabyal, "Light-dependent negative differential resistance in MEH-PPV decorated electrospun TiO₂ mat," *Appl. Phys. A*, vol. 124, no. 4, 2018, Art. no. 349.
- [27] W. L. Guo, S. L. Zhang, P. N. Zhang, and J. Zhou, "Non-linear photo isolator and its response maintaining function," *Semicond. Optoelectron.*, vol. 23, no. 3, pp. 167–166, 2002.