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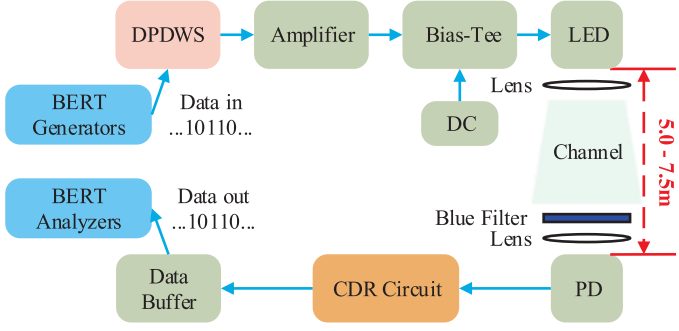

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Real-Time 262-Mb/s Visible Light Communication With Digital Predistortion Waveform Shaping

Weishu Xu,[1] **Min Zhang**,[1] **Dahai Han**,[1] **Zabih Ghassemlooy**,[2] **Pengfei Luo**,[3] **and Yongjian Zhang**[4]

[1]State Key Laboratory of Information Photonics and Optical Communications, Beijing University of Posts and Telecommunications, Beijing 100876, China
[2]Optical Communications Research Group, Faculty of Engineering and Environment, Northumbria University Newcastle, Newcastle upon Tyne NE1 8ST, U.K.
[3]Research Department of HiSilicon, Huawei Technologies Co., Ltd., Beijing 100085, China
[4]School of Information Science and Technology, University of International Relations, Beijing 100091, China

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Abstract: A digital predistortion waveform shaping scheme combined with a blue filter is proposed to optimize both the rise and fall times of a light-emitting diode (LED) and the optical receiver current of the signal of the real-time visible light communication (VLC) system. The proposed scheme is implemented on a field-programmable gate array (FPGA) and a digital-to-analog converter based test bed, which is flexible and reconfigurable by programming the FPGA to match different LED characteristics and varied data rates. A 262-Mb/s non-return-to-zero on-off keying modulation based real-time VLC link with a bit error rate of less than 1.0×10^{-6} is achieved over a transmission distance of 5.0 m, which uses a single white phosphorous LED with a limited power of 0.1 W.

Index Terms: Digital pre-distortion waveform shaping (DPDWS), real-time visible light communication (VLC), rise and fall times, white phosphorous LED.

1. Introduction

Light-emitting diode (LED)-based lighting systems are replacing conventional systems due to their unique features which include low energy consumption, low cost, longer lifespan, and environmental friendliness for both indoor and outdoor usage. The applications of LEDs including illumination and visible light communication (VLC) (i.e., data communication, indoor positioning, and environmental sensing). VLC systems offer a number of interesting features including: (i) an unlicensed and wide spectrum band; (ii) free from radio frequency (RF)-based electromagnetic interference (i.e., ideal for applications where RF signals are not allowed to be used) [1]; (iii) enhanced communication security, which is highly desirable in banking, manufacturing, financial transactions, etc. [2]; and (iv) very high accuracy when used for indoor positioning [3]. VLC systems are used in a number of applications, such as, underwater communications, medicine, manufacturing, aircraft, intelligent transportation systems, and others [1], [4]–[6].

However, in high bandwidth-link applications, VLC systems face significant challenges due to the low modulation bandwidth of white phosphorous LEDs (i.e., in the range of a few MHz). The modulation bandwidth of LEDs is greatly limited by the recombination lifetime and the time constant associated with depletion capacitance [7]. Most commercially available LEDs used in VLCs have a large current-injected p-n junction area, and therefore a large capacitance. The time constant due to the space-charge capacitance of the diode can be reduced by using a small-area p-n junction for the electron-emitting layer [8]. For high-speed LEDs, a shorter recombination lifetime is needed, which is achieved by high active-layer doping, but at the cost of reduced efficiency and a broadened spectrum [9]. In addition, the modulation bandwidth of an LED is proportional to the square root of the current density [10]. In order to increase the modulation bandwidth of an LED, it is necessary to reduce the junction capacitance and the recombination lifetime.

To overcome the inherent limitation of the -3 dB bandwidth f_{-3dB} of commercial LEDs and to increase the transmission data rate R_b, several schemes have been adopted including: current shaping (i.e., an RC network with a time constant equal to or less than the spontaneous recombination lifetime) [11], peaking and carrier sweep-out effects [12], optical blue filtering [13], and pre-and post-equalization [14]. In [15], the f_{-3dB} of a VLC-link was extended to 220 MHz using pre-emphasis and post-equalization circuits, which allowed an R_b of 553 Mbps with non-return-to-zero on-off keying (NRZ-OOK) modulation. Analog pre-emphasis and post-equalization circuits were used to enhance the f_{-3dB} of the VLC-link from 3 MHz to 233 MHz using NRZ-OOK modulation with an R_b of 550 Mbps [14]. The most effective approach is to develop higher bandwidth LEDs, such as, resonant-cavity LEDs and μLEDs that have f_{-3dB} of approximately 100 MHz and 150 MHz, respectively [11], [16]. Furthermore, several spectrally efficient modulation techniques can be utilized to greatly increase the R_b, such as, red-green-blue (RGB) LED-based wavelength division multiplexing, multi-level and multi-carrier transmission (i.e., orthogonal frequency division multiplexing), and others [17], [18].

In this paper, we proposed a field-programmable gate array (FPGA) and a digital-to-analog converter (DAC)-based digital pre-distortion waveform shaping (DPDWS) scheme to increase the transmission R_b by reducing both the rise time t_r and fall time t_f of the LED, as well as the optical receiver (Rx) current in the low-speed area of the modulating signal. We experimentally demonstrate a 262-Mbps real-time VLC-link, employing the proposed DPDWS scheme and a single white phosphorous LED with NRZ-OOK modulation. The experimental results show that a transmission R_b of 262 Mbps over a transmission distance L of 5.0 m is achieved with a bit error rate (BER) of less than 1.0×10^{-6}. This is well below the forward error correction (FEC) threshold of 3.8×10^{-3}. Compared with conventional schemes (e.g., the reported pre-emphasis and post-equalization schemes in [14] and [15], which are analog signal processing techniques), the proposed DPDWS scheme can be reprogrammed via FPGA to optimize the parameters for different VLC-links, instead of changing the resistors, the capacitors, or other components of circuits. The function of the DPDWS scheme is to change the voltage of the signal in the low-speed area without using any complicated digital signal processing algorithms. The code is simple to implement, and therefore only a few logical elements of an FPGA are required. However, for a higher transmission R_b, a faster FPGA and a DAC with a higher sampling rate are required (e.g., for a transmission R_b of 300 Mbps, the maximum operating clock frequency of the FPGA and the maximum sampling rate of the DAC should be higher than 300 MHz and 300 MSPS, respectively), resulting in higher cost. Therefore, there is a trade-off between the transmission R_b and the cost associated with the FPGA and the DAC. In addition, the vertical resolution requirement of the DAC is not very demanding due to the low-order modulation (i.e., OOK modulation) and the DAC output signal processing by the DPDWS module is only a fourth-order signal.

2. Proposed System

A schematic block diagram of the proposed system is shown in Fig. 1. At the transmitter (Tx), a pseudorandom binary sequence (PRBS) in the NRZ-OOK pattern is applied to a DPDWS module, which is based on an FPGA board and a DAC. The reshaped signal is amplified and then applied to

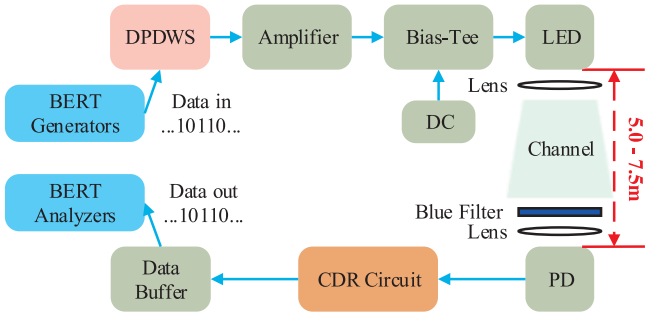

Fig. 1. System block diagram.

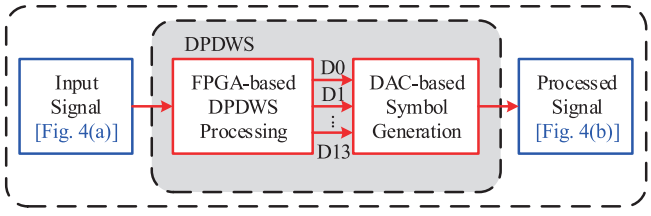

Fig. 2. Structure of the proposed DPDWS scheme.

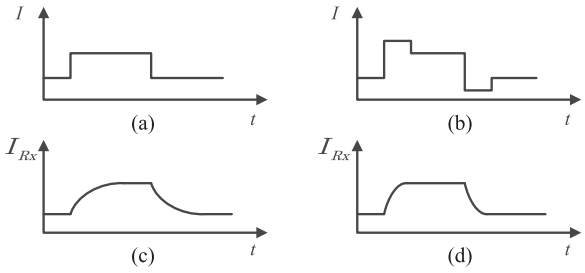

Fig. 3. Current waveforms at (i) the Tx (i.e., LED) (a) without excess current, and (b) with excess current; and (ii) the optical Rx (c) without excess current, and (d) with excess current.

a bias-tee prior to modulate a white phosphorous LED. For a longer transmission L , a set of lenses are used to focus the LED light on both the Tx and Rx. A blue filter at the Rx is used to increase the LED's bandwidth. An optical Rx is positioned after the blue filter to regenerate a transmitted data stream. To recover the system clock and maintain synchronization, a clock and data recovery (CDR) module is used as in [19]. A bit error rate tester (BERT) is used to determine the link's BER.

The structure of the proposed DPDWS scheme illustrated in Fig. 2 is used to reduce both t_r and t_f, as well as the optical Rx current in the low-speed area by the combination of an FPGA board and a DAC-based symbol generation. The proposed DPDWS scheme is flexible and reconfigurable by simply re-programming the FPGA for different LED characteristics and R_b.

2.1 Reducing t_r and t_f of the LEDs

To increase the transmission R_b of the LEDs, it is necessary to reduce both t_r and t_f. For the input current signal applied to the LEDs, the DPDWS module creates an excess current when the LED is switched on or off, as shown in Fig. 3. During the switch-on transient, the excess current assists in achieving the steady-state carrier concentration in the active region within a t_r shorter than the spontaneous lifetime t_{sl}. During the switch-off transient, the reverse current assists in sweeping out carrier of the LED within a t_f shorter than t_{sl} [8], [12]. Note that t_{sl} defined in terms of an LED's f_{-3dB}

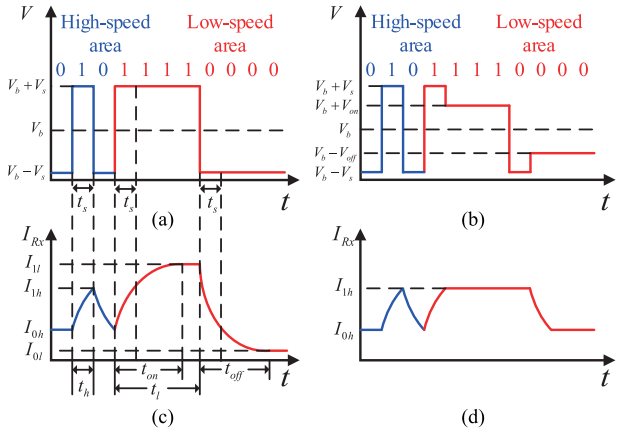

Fig. 4. Waveforms at the DPDWS module: (a) input, (b) output. The corresponding current waveforms at the Rx: (c) without DPDWS, and (d) with DPDWS.

is given as [20]:

$$t_{sl} = \frac{1}{2\pi f_{-3\text{dB}}}. \tag{1}$$

Considering a linear system, we have:

$$t_r = t_f = \ln(9) t_{sl} \approx 2.2 t_{sl}. \tag{2}$$

2.2 Reducing Optical Rx Current

Fig. 4(a) and (b) show the waveforms before and after the DPDWS module, where the continuous and fast-changing binary "0" or "1" sequences are defined as low- and high-speed area, respectively. The waveforms of the response of the LED are shown in Fig. 4(c) and (d), which indicate both t_{on} and t_{off} for the optical Rx current reaching the steady-state level. In general, the time t_{on} (or t_{off}) is lower and higher than the symbol period t_l and t_h for the low- and high-speed area, respectively. This reflects that the optical Rx current in the low-speed area is higher than that of the high-speed area, as seen in Fig. 4(c). In this case, the peak-to-peak voltage level adopted is $2V_s$, the bias voltage is V_b, and the signal bit period is t_s (which is $< t_{on}$ and t_{off}). Thus, the optical Rx current in the high-speed area never reaches the steady-state level, as shown in Fig. 4(a) and (c). Note that reducing the input signal level in the low-speed area is effective for reducing the optical Rx current in this region, as shown in Fig. 4(b) and (d).

For the input signal switched between the level "0" to "1", we can express the current at the optical Rx as:

$$I(V_s, t) = \begin{cases} I_{0\to1}(2V_s, t), & t \le t_{on} \\ I_{max1}(2V_s), & t > t_{on} \end{cases}, \tag{3}$$

where $I_{0\to1}(2V_s, t)$ and $I_{max1}(2V_s)$ are the currents at the optical Rx for $t \le t_{on}$ and $t > t_{on}$, respectively, and V_s is a constant. Fig. 5(a) illustrates the input signal applied to the LED, and its corresponding optical signal at the Rx is shown in Fig. 5(b).

For a high-level input signal of "1", the optical Rx current in the high-speed area never reaches the steady-state level of I_{max1} due to $t_h < t_{on}$ (or t_{off}). This is in contrast to the low-speed area. Thus, I_{1h} and I_{1l} are given as:

$$I_{1h} = I_{0\to1}(2V_s, t_s), \tag{4}$$

$$I_{1l} = I_{max1}(2V_s). \tag{5}$$

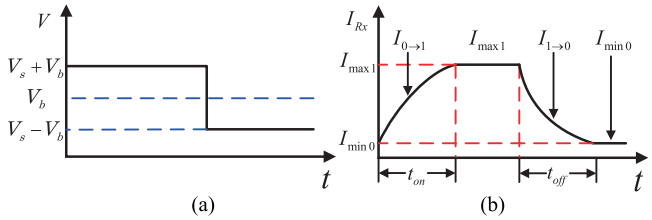

Fig. 5. Waveforms at the LED: (a) input voltage, and (b) current at the Rx.

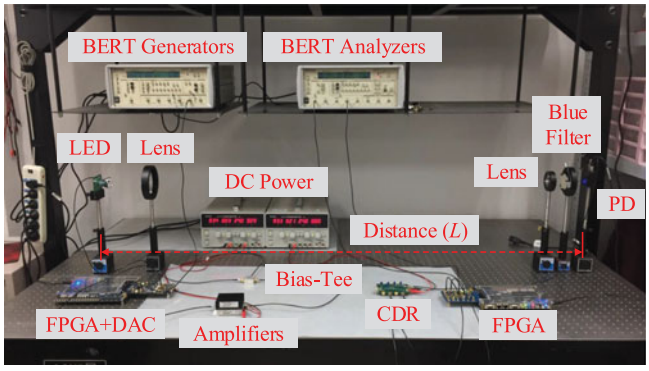

Fig. 6. Experimental testbed for the DPDWS scheme-based VLC-link.

Note that $I_{1l} = I_{1h}$ if the input signal voltage in the low-speed area is reduced to V_{on}, as seen in Fig. 4(b) and (d). Thus, V_{on} can be obtained from (4) and (5), which is given by:

$$I_{max1}(2V_{on}) = I_{0\to1}(2V_s, t_s). \tag{6}$$

For $I_{1l} = I_{1h}$ the input signal in the low-speed area reaches the voltage level of V_{on}, and the pre-distortion depth A_1 is expressed as:

$$A_1 = 20\lg\left(\frac{V_s}{V_{on}}\right)\ (\text{dB}). \tag{7}$$

Similarly, for the input signal of "0", $I_{0l} = I_{0h}$ provided that the input signal voltage in the low-speed area is increased to V_{off}, as seen in Fig. 4(b) and (d). Therefore, the pre-distortion depth A_0 is defined as:

$$A_0 = 20\lg\left(\frac{V_s}{V_{off}}\right)\ (\text{dB}). \tag{8}$$

In addition, we defined the DPDWS parameters of $[A_1,\ A_0]$ as the pre-distortion depth, which can be determined from (7) and (8) to match different LED characteristics and varied R_b.

3. Experiment and Results

3.1 Experimental Setup

Fig. 6 presents the experimental testbed for the proposed system. At the Tx, the input NRZ-PRBS-OOK bit stream with a pattern length of $2^{20} - 1$ is generated by the BERT (gigaBERT-1400), and it is first processed by the DPDWS module, which is implemented using an FPGA board (Cyclone IV EP4CE115) and a DAC (DAC5672). The signal is amplified by the amplifier (ZHL-6A-S+) to enhance the modulation depth and modulated to a white phosphorous LED that is driven by the bias-tee (ZFBT-4R2G+). A convex lens with a focal length of 15 cm is used for beam collimation. At

TABLE 1
System Parameters

	Parameter	Values
Tx:		
	Data rate R_b	262 Mbps
	Modulation	NRZ-OOK
	Patten length	$2^{20}-1$
FPGA	Type	Cyclone IV EP4CE115
DAC	Type	DAC 5672
	Maximum sampling rate	275 MSPS
Amplifier	Type	ZHL-6A-S+
	Bandwidth	500 MHz
	Gain	25 dB
Bias-Tee	Type	ZFBT-4R2G+
	Bandwidth	4200 MHz
LED	Type	General white phosphorous LED
	Bandwidth	4.2 MHz
	Transmit power	0.12 W
Convex lens	Diameter	10 cm
	Focal length	15 cm
Channel:	Length	5.0 m
Rx:		
Convex Lens	Diameter	5 cm
	Focal length	7 cm
Optical Rx (PDA10A)	Peak wavelength	730 nm
	Active area	$0.8\ mm^2$
	Bandwidth	150 MHz
	PD Responsivity (in 730 nm)	0.44 A/W
	NEP	$3.5 \times 10^{-11}\ W\sqrt{Hz}$
	Noise	1.5 mVrms
CDR	Type	ADN 2812
	Data rates	12.5-2700 Mbps

the Rx, we use a convex lens with a focal length of 7 cm, an optical blue filter (to enhance the LED's bandwidth), and a fixed gain optical Rx (PDA10A), which is composed of a silicon photo-diode and a trans-impedance amplifier. To recover both the clock and retimes of the data, the received signal is applied to the CDR (ADN2812) and the FPGA modules. Finally, the BER performance of the VLC-link is determined by using a BERT (gigaBERT-1400) in real time. The key system parameters are provided in Table 1.

The real-time VLC system is an asynchronous link, where bit synchronization timing needs to be directly acquired from the regenerated data sequence at the Rx. Since Tx and Rx FPGAs are running at different clock frequencies, then any frequency drift will contribute to a worsening of the BER. To overcome this, a CDR module is employed to recover both the clock and retimes of the data signal.

3.2 Results and Discussion

The measured plot of the luminous intensity versus the forward current for the LED is shown in Fig. 7(a). Note that the plot is not completely linear, showing two linear regions, A and B, which limits the maximum achievable peak-to-peak current at the optical Rx. In this work, we operate the LED

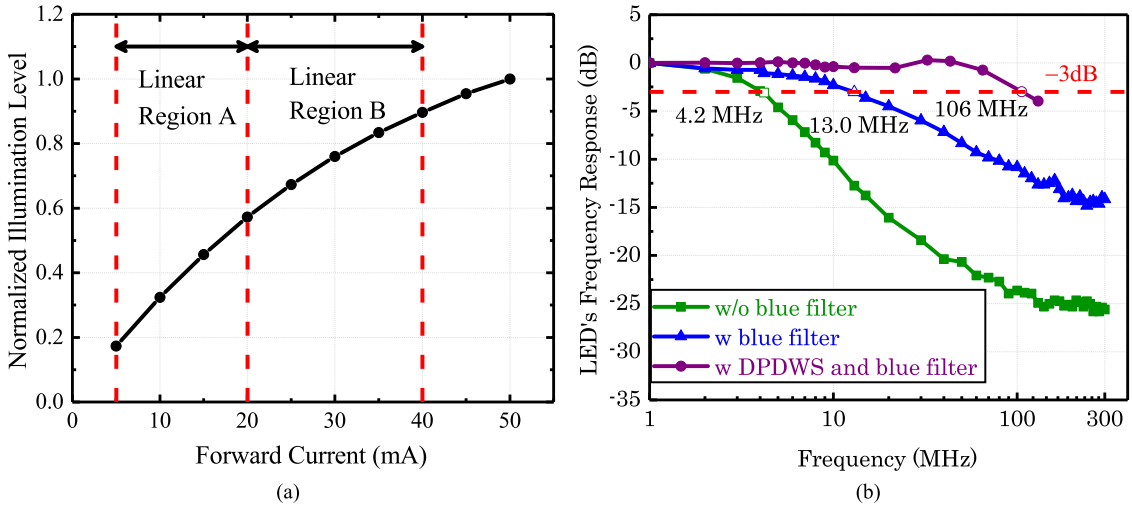

Fig. 7. Measured LED responses: (a) luminous intensity versus the forward current, and (b) the frequency response with (w) or without (w/o) a blue filter, and with a blue filter using the DPDWS scheme.

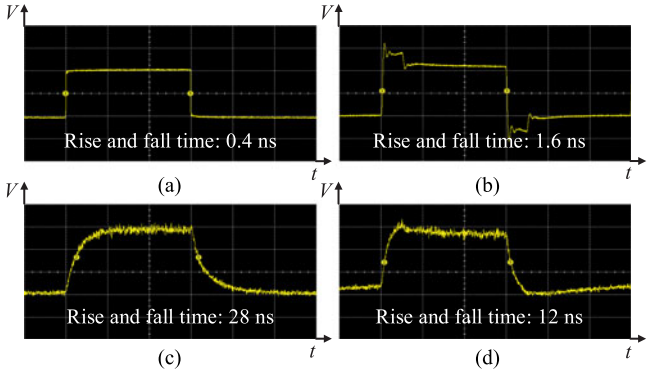

Fig. 8. Measured voltage waveforms at the: (a) input, (b) output of the DPDWS module, and output of the optical Rx (c) without DPDWS, and (d) with DPDWS. Horizontal scale: 55 ns/div.

in region B to achieve a higher illumination level. The measured small-signal frequency response of the white phosphorous LED at a bias current of 30 mA is shown in Fig. 7(b). The f_{-3dB} of the white phosphorous LED is extended from 4.2 MHz to 13.0 MHz with the blue filter. In addition, the proposed DPDWS scheme is used to enhance the f_{-3dB} of the VLC-link from 13.0 MHz to 106 MHz using the blue filter. Note that the bandwidth beyond −3 dB can also be used in applications with lower signal-to-noise ratio (SNR) requirements.

Fig. 8 shows the voltage waveforms at the Tx and the Rx, measured using a Keysight MSOS404A oscilloscope (4 GHz bandwidth). Note that the measured f_{-3dB} of the white phosphorous LED with the blue filter is 13.0 MHz (i.e., $t_{sl} = 12.2$ ns). Thus, the predicted LEDs t_r and t_f are 27 ns, which is almost the same as the measured value of 28 ns. However, both t_r and t_f are reduce to 12.0 ns when using the DPDWS scheme. Therefore, the measured results show that the excess current processed by the DPDWS module has a considerable impact on the performance of the white phosphorous LED. Fig. 9 shows the measured output voltage waveforms at the BERT generator, the DPDWS module, the PD, and the CDR circuit.

The measured spectra of the OOK signal before and after the DPDWS module is shown in Fig. 10. Note that the amplitude of the signal in the relative low-frequency region (e.g., for a transmission R_b of 100 Mbps, the frequency of signal spectrum less than approximately 45 MHz is defined as

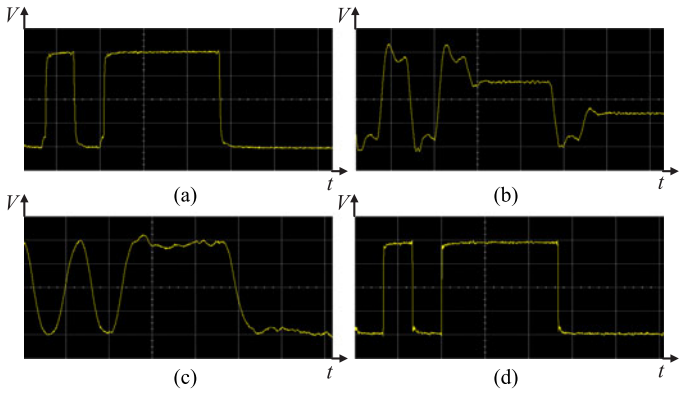

Fig. 9. Measured output voltage waveforms for (a) the BERT generator, (b) the DPDWS module, (c) the PD, and (d) the CDR circuit. Horizontal scale: 15 ns/div.

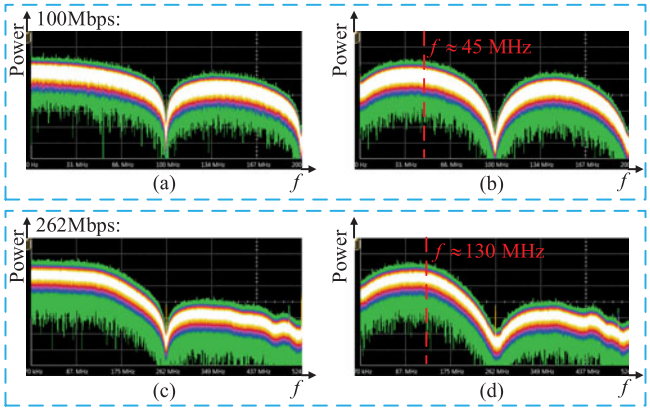

Fig. 10. Measured spectra of OOK signal: (i) (a) before, and (b) after the DPDWS module with R_b of 100 Mbps, and (ii) (c) before, and (d) after the DPDWS module with R_b of 262 Mbps.

the relative low-frequency region) is attenuated after the DPDWS module. The amplitude of the signal in the relative low-frequency region is closer to that of the relative high-frequency region, and therefore the acquired eye-diagram is open using the DPDWS scheme, as shown in Fig. 11. Thus, the proposed scheme has a considerable impact on enhancing the $f_{-3\text{dB}}$ of the VLC-link.

To evaluate the data transmission performance of the proposed real-time VLC-link with a transmission L of 5.0 m, we measured the eye-diagrams of the 262-Mbps VLC-link detected at the PD for various pre-distortion depths, as shown in Fig. 11. The eye-diagram is completely closed without DPDWS, and therefore the data cannot be directly recovered at the receiver. Using the optimum pre-distortion depth of [20.21, 13.17], the eye-diagram is clearly distinguishable, and the data can be recovered directly at the receiver. Furthermore, the transmission L has no effect on the optimum pre-distortion depth.

Meanwhile, we used the BERT to measure the BER performance as a function of the R_b for a range of pre-distortion depths, as shown in Fig. 12(a). Considering the FEC limit of 3.8×10^{-3}, the achievable R_b is only 34 Mbps without DPDWS. However, R_b increases to 262 Mbps with a BER of less than 1.0×10^{-6} when using the DPDWS scheme. Fig. 12(a) also shows the pre-distortion depth of [20.21, 13.17], which offers the best BER performance. Note that a CDR circuit is used for clock recovery and data retiming from the received data stream due to the asynchronous VLC-link. The reason for the rapid BER performance degradation is the CDR module abruptly loses lock (i.e., the error clock and data were recovered by the CDR module) as the data rate increases (e.g., R_b is

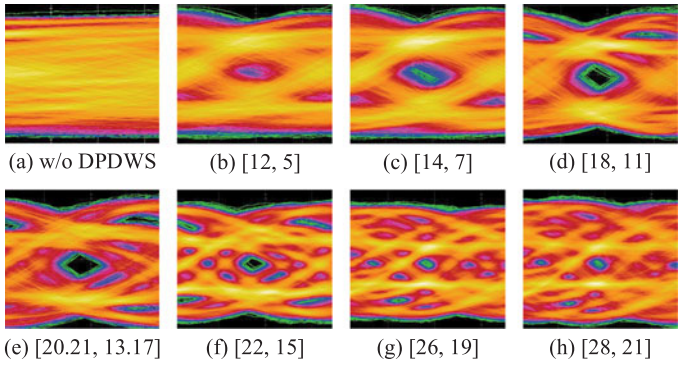

Fig. 11. Received NRZ-OOK eye-diagrams for the 262-Mbps VLC-link at 5.0 m: (a) without DPDWS, and with various pre-distortion depths of (b) [12, 5], (c) [14, 7], (d) [18, 11], (e) [20.21, 13.17], (f) [22, 15], (g) [26, 19], and (h) [28, 21].

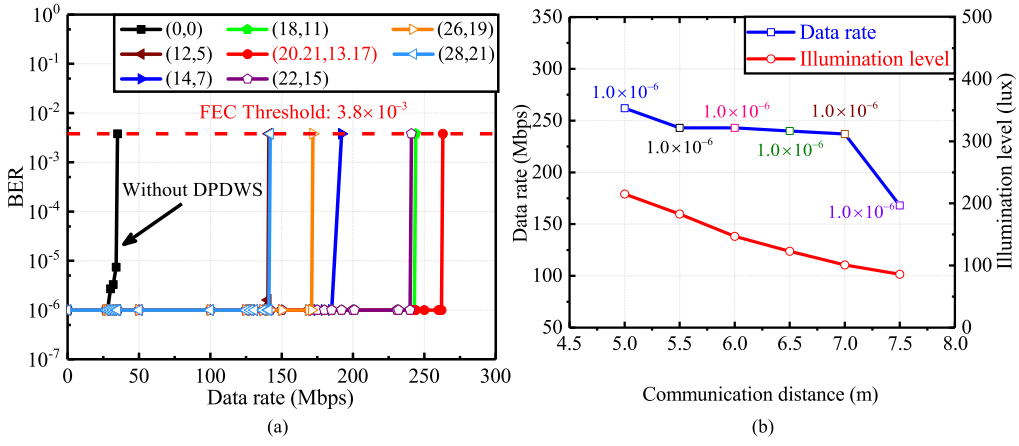

Fig. 12. Measured (a) BER performance versus the transmission R_b for a range of pre-distortion depth and L of 5.0 m, and (b) transmission R_b and the white light illumination level versus L.

higher than 262 Mbps with a pre-distortion depth of [20.21, 13.17]), resulting in a large number of bit errors. We defined the $BER > 3.8 \times 10^{-3}$ if the CDR module loses lock at the receiver. Although the pattern length of the PRBS is sufficient, the times of the experimental measurement is limited. We defined the $BER = 1.0 \times 10^{-6}$ if the $BER < 1.0 \times 10^{-6}$ or there is an error-free transmission at the receiver. In a real scenario, the optimum pre-distortion depth can be determined experimentally by applying a feedback signal based on the LED characteristics and R_b.

Finally, for the optimal pre-distortion depth value of [20.21, 13.17], the measured maximum transmission R_b and light illumination level as a function of L are presented in Fig. 12(b). The BER values for each measurement are well below the FEC limit of 3.8×10^{-3}. As expected, both the measured R_b and the illumination level decrease with L. The lowest R_b is 168 Mbps with a BER of less than 1.0×10^{-6} and the illumination level is 86 lux at L of 7.5 m. Note that for $L > 6$ m, the CDR module will lose lock without DPDWS, and therefore cannot recover the clock and data; and low luminance leads to a reduced SNR level, and thus an increased BER.

4. Conclusion

In this experimental work, we proposed an FPGA and a DAC-based DPDWS scheme to achieve a real-time high bit rate VLC-link using a commercial 0.1-W white phosphorous LED. We

demonstrated a 262-Mbps real-time VLC-link over a transmission L of 5.0 m with a BER of less than 1.0×10^{-6}, which is well below the FEC limit of 3.8×10^{-3} using the DPDWS scheme. Increasing the transmission link to 7.5 m resulted in a reduced R_b of 168 Mbps, but with a BER of less than 1.0×10^{-6}. The VLC-link with the DPDWS scheme implemented with the FPGA board and DAC is flexible and reconfigurable by simply modifying the pre-distortion depth of $[A_1, A_0]$.

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