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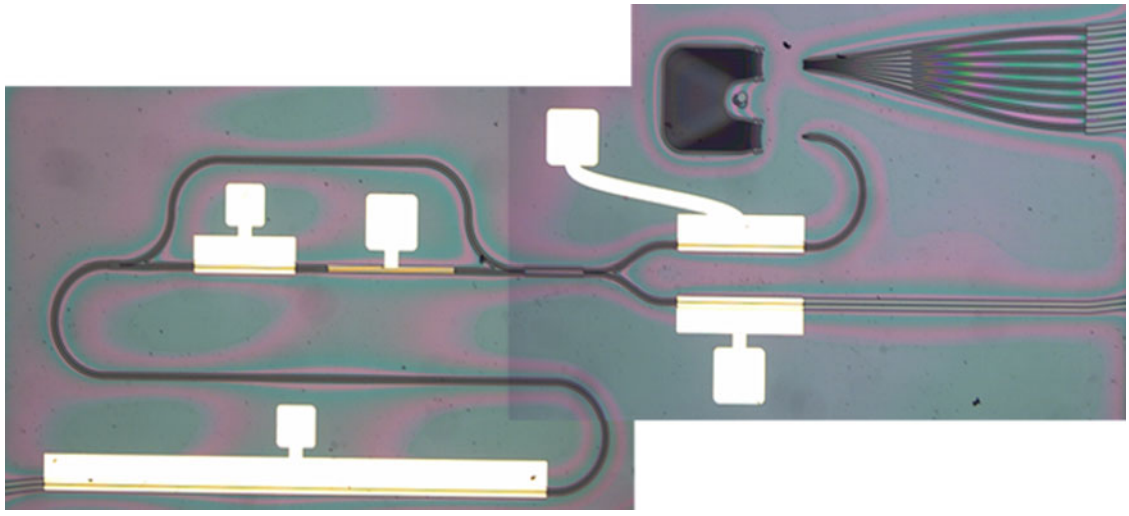

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Monolithic Integrated Chip With SOA and Tunable DI for Multichannel All-Optical Signal Processing

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Abstract: An indium phosphide-based monolithic integrated chip with semiconductor optical amplifiers and a tunable delay interferometer (DI) is developed. Because of the comb filtering characteristics of DI, this chip has the potential to be used for multichannel all-optical signal processing functions in dense wavelength-division-multiplexed networks. In this paper, four-channel all-optical format conversion simultaneously from nonreturn-to-zero to return-to-zero at 40 Gb/s with a power penalty of less than 0.5 dB is demonstrated as a validation based on this chip.

Index Terms: Photonic integrated circuits, optical data processing, all-optical signal processing, semiconductor optical amplifiers.

1. Introduction

Photonic integration has been a very hot research topic throughout the last ten years due to its small footprint, low power consumption, high reliability [1]–[5], and its widely potential applications in optical networks, data centers, high performance computing, lidar systems, etc. [4], [6], [7]. Indium phosphide (InP)–based and silicon-based integrated chips are two main research counterparts in this area, and InP-based integration chip has the potential to be monolithic integrated in which laser, detector, modulator, amplifier, waveguides could be developed with the same InP material system [4], [8], [9]. Widely tunable lasers [10], multichannel optical transceivers [11], [12], lidar systems [13], etc. have been demonstrated with InP-based monolithic integrated chips.

On the other hand, all-optical signal processing technologies have received widely attentions in the past two decades for avoiding optical-to-electrical and electrical-to-optical conversion processes and increasing the capacity of the optical networks [2], [14], [15]. For dense wavelength division multiplexing (DWDM) optical networks, multichannel optical signal processing technologies should be developed to handle multichannel optical signals. In our group, schemes for multichannel optical signal processing functions with semiconductor optical amplifiers (SOAs) and comb filters were

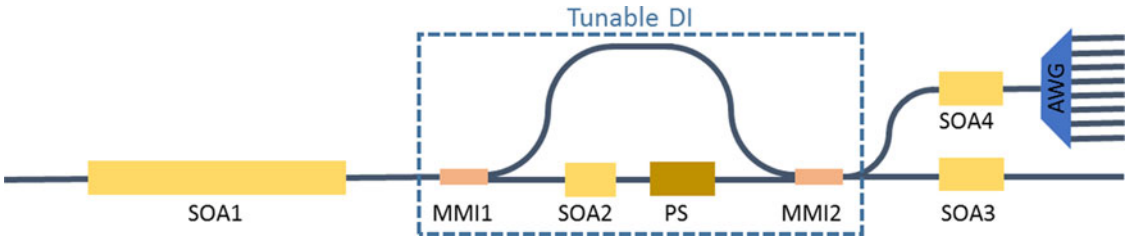

Fig. 1. Schematic diagram of the monolithic integrated chip.

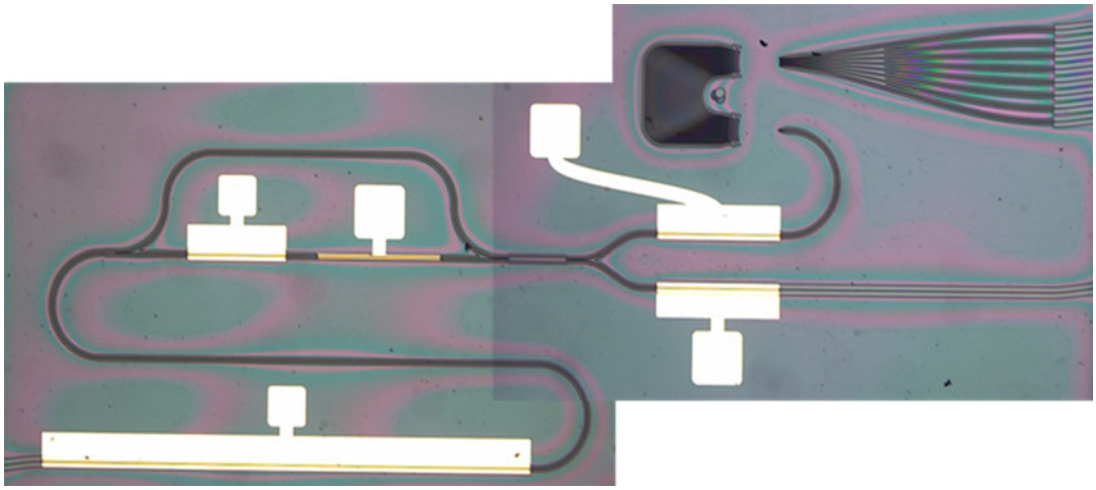

Fig. 2. Metallographic microscope picture of the fabricated monolithic integrated chip (footprint: 2.0 $\times$ 4.6 mm^2).

proposed and demonstrated for 16 $\times$ 10 Gb/s and 8 $\times$ 20 Gb/s multichannel signals [16]–[18]. However, all experimental results were demonstrated with discrete devices. Monolithic integrated chips based on this scheme are worthy of further investigation. Very recently, reconfigurable signal processor [2], wavelength router [19], unicast and multicast wavelength converter [20], etc. have been successfully demonstrated with InP-based monolithic integrated chips. But, one monolithic chip with only one nonlinear SOA for processing multichannel signals simultaneously has not been reported. In this work, we developed a monolithic integrated chip based on one nonlinear SOA and a tunable delay interferometer (DI) for processing multichannel signals simultaneously, and the proposed integrated chip has much simpler configuration and is more reliable.

All-optical format conversion is one of the most important functions for all-optical signal processing in optical networks, because there are different modulation formats exploited in different parts of the networks [21]. Although non-return-to-zero (NRZ) to return-to-zero (RZ) formats are not popular in current optical networks [21], they are basic modulation formats for generating advanced modulation formats most of which can be divided into NRZ-type and RZ-type. Those schemes for NRZ-RZ conversion can also be developed to realize NRZ-type to RZ-type advanced modulation format conversion [21], [22]. So, we use NRZ-RZ conversion as the example to demonstrate the function for multichannel signal processing. In this paper, based on this chip, four-channel format conversion from NRZ to RZ format at 40 Gb/s has been successfully realized.

2. Operation Principle, Chip Design and Device Characterization

Schematic diagram of the monolithic integrated chip is shown in Fig. 1. The chip consists of four sections, a long SOA1, a tunable DI, short SOA3 and SOA4, and an arrayed waveguide grating (AWG). The long SOA1 with a length of 2000 μm is used as a nonlinear device where nonlinear

TABLE 1
The Epitaxial Structure of the Device.

active layer stack				passive layer stack			
Layer	Material	Doping	*d* [nm]	Layer	Material	Doping	*d* [nm]
III-3	p-InGaAs	$1.5*10^{19}$	300	III-3	p-InGaAs	$1.5*10^{19}$	300
III-2	p-InP	$1.5*10^{20}$	1000	III-2	p-InP	$1.5*10^{20}$	1000
III-1	p-InP	low 10^{17}	300	III-1	p-InP	low 10^{17}	300
I-6	p-InP	low 10^{17}	200	II-2	n-InP	low 10^{17}	200
I-5	i-Q1.25		205	II-1	n-Q1.25	low 10^{16}	500
I-4	i-MQW(4)		90				
I-3	i-Q1.25		205				
I-2	n-InP	low 10^{17}	500	I-2	n-InP	low 10^{17}	500
I-1	n-InP	low 10^{18}	500	I-1	n-InP	low 10^{18}	500
I-0	n-InP	$1.4*10^{18}$	substrate	I-0	n-InP	$1.4*10^{18}$	substrate

The Roman Numerals Indicate the Different Epitaxial Growths. The Blue Color Indicates the Cladding Layer, Green is the Waveguiding Film and Red is the Active Layer.

effects such as cross phase modulation (XPM) and cross gain modulation (XGM) occur, and the relatively long length is helpful for enhancing the nonlinear effects. The tunable DI consists of two multi-mode interference (MMI) couplers, a 400-μm-long SOA2 and a 500-μm-long phase shifter (PS). The MMI1 is used to split the signal, and the MMI2 is used to combine the signals from the two arms with different phase shifting. The PS is used for detuning the center wavelength of the comb filter, and SOA2 is used for compensating the loss introduced by the PS. In the end, 500-μm-long SOA3 and SOA4 are used to amplify the output signals for further processing and analyzing. The AWG is designed for demultiplexing the multichannel signals. The metallographic microscope picture of the fabricated chip is shown in Fig. 2. Regarding the epitaxial structure of different elements in the chip, there are two main different structures, one is for active waveguide and the other is for passive waveguide which can be shown in Table 1 in detail. For the active waveguide, there is an additional multi-quantum well (MQW) structure with 4 periods. The fabrication process is carried out by Smart Photonics Co. Ltd. with the help of Joint European Platform for photonic integration of components and circuits, more details of the structure can be found in the design manual [23]. The SEM photos of the long SOA, 1 $\times$ 2 MMI and the tunable DI are also shown in Fig. 3(a), (b) and (c), respectively. It should be mentioned that there are two kinds of waveguide architectures in this chip, ridge waveguide and slab waveguide, as shown in Fig. 4(a) and (b), respectively. Compared with the slab waveguides, the ridge waveguides have lower loss but need larger bending radius. Therefore, in our chip, the SOAs, PS and the long straight waveguides are ridge waveguides for low loss, while the curve waveguide are slab waveguides for small bending radius.

First of all, the performance of the PIC is characterized. The amplified spontaneous emission (ASE) spectra of the integrated SOA1 at different bias currents are shown in Fig. 5(a). The gain peak wavelength is located around 1570 nm and in the format conversion experiment the pump light should be located close to the 1570 nm for better format conversion result. The output power as a function of input optical power at different wavelengths for 270 mA biased current are shown in Fig. 5(b), and it shows that the SOA would work in saturated state when the input signal power is higher than 0 dBm. The output power as a function of injected current at different input optical powers for 1560 nm wavelength are shown in Fig. 5(c), and the results show that the output power will not increase correspondingly while increasing the biased current to be higher than 300 mA. Finally, the tunability of the DI is shown in Fig. 5(d). The measured free spectral range (FSR) of the

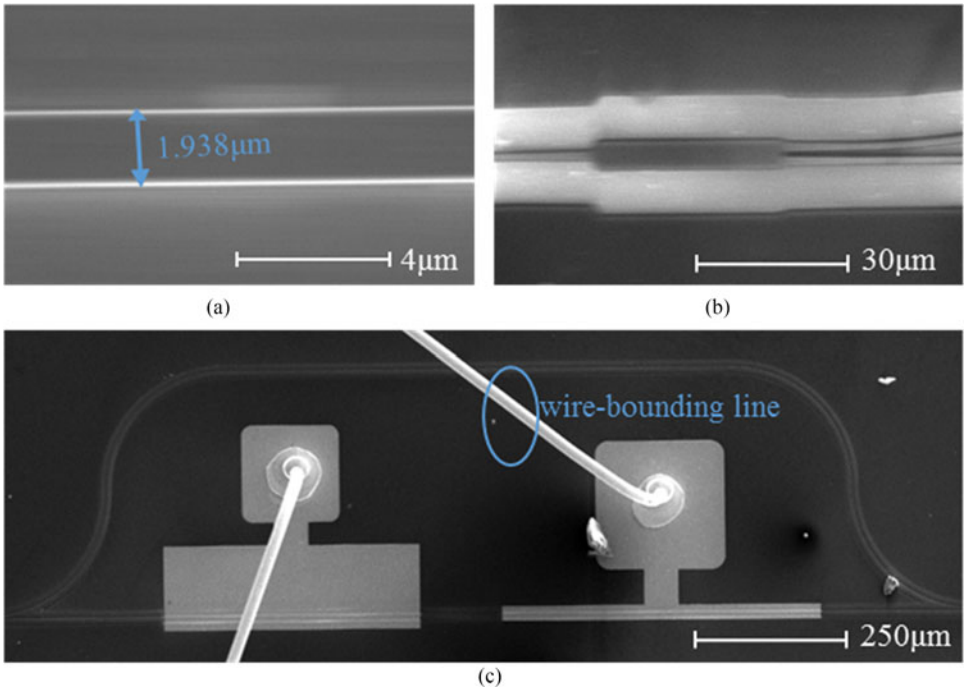

Fig. 3. SEM photos of the PIC. (a) SOA. (b) 1 × 2 MMI. (c) Tunable DI.

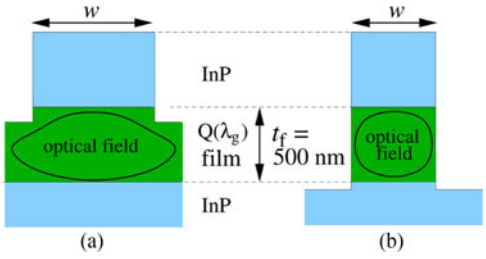

Fig. 4. The cross section of (a) ridge waveguide and (b) slab waveguide.

DI is around 1.5 nm, which is close to the international telecommunication union (ITU) wavelength space of 1.6 nm. Besides, the tunable efficiency of the PS is experimentally around 0.68 nm/mA. In other words, 1.1 mA injected current can tune the DI with half a FSR. With the good tunability of the DI, it is feasible to detune the multichannel filter and extract the specific desired spectra of the multichannel signals simultaneously.

This chip is designed for processing multi-channel optical signals, and as a proof-of-concept demonstration, we demonstrate this function by realizing four-channel format conversions simultaneously from NRZ to RZ at 40 Gb/s. The operation principle is illustrated with the help of spectrum evolutions as shown in Fig. 6. The multichannel NRZ signals worked as probe signals are launched into the integrated chip together with a strong RZ clock signal. Due to the XPM effect in the SOA1, the output multichannel signals carry strong periodic phase modulation information and the spectra are broadened widely. Then the DI filter, which has a comb-like spectral response, is used to extract the specific desired spectra from the broadened spectra of those four channels simultaneously. With proper detuning, the DI will only transmit frequency shifted components caused by the XPM. Lastly, the converted RZ signals are obtained. Although the scheme is proposed for multichannel format conversion, the operational principle for realizing NRZ-to-RZ conversion is the same as the

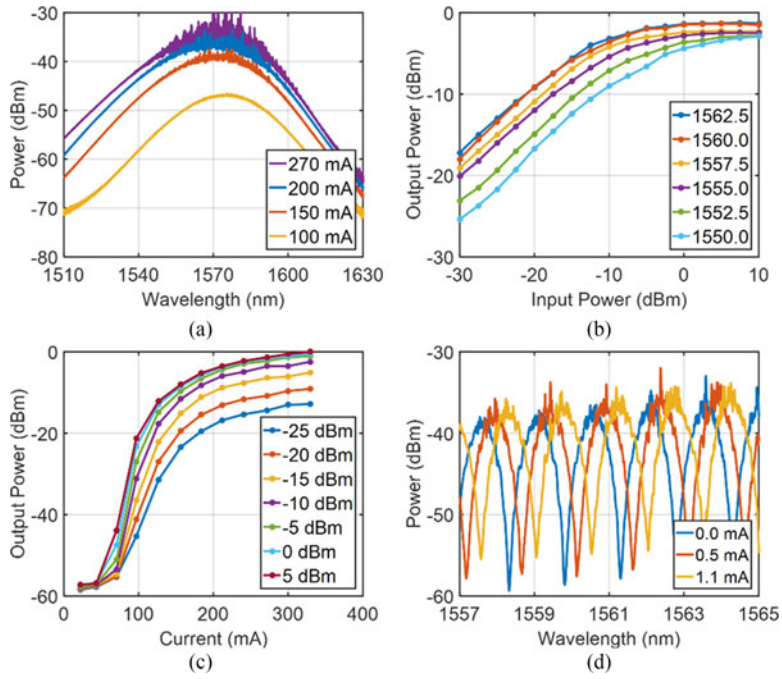

Fig. 5. (a) Measured ASE spectra of the SOA at different bias current. (b) Output power as a function of input optical power at different wavelengths (bias current: 270 mA). (c) Output power as a function of injected current at different input optical powers (wavelength: 1560 nm). (d) The spectrum of the integrated tunable DI at different phase shifter injected current.

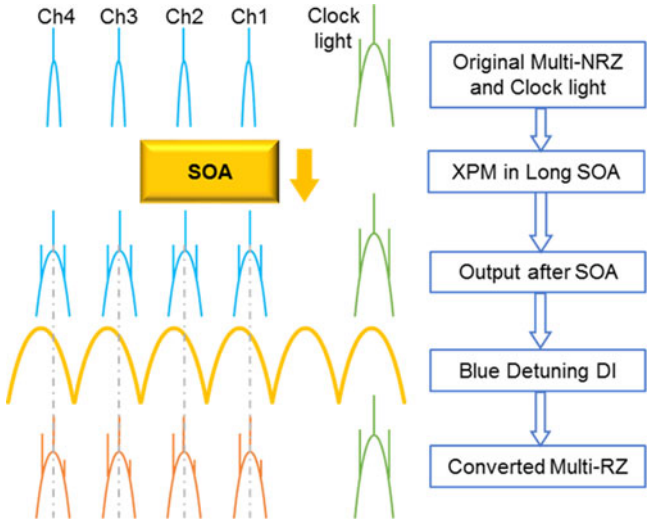

Fig. 6. Illustration of the spectrum evolution in the four-channel format conversion process.

scheme for single channel, related theoretical description and numerical simulation have been reported in our group [24]. For multichannel format conversion, crosstalk between different channels is a problem to be paid much attention. In our scheme, the RZ clock signal should be strong enough to suppress the inter-channel crosstalk, and probe signals should be weak enough and chosen to deviate from the peak wavelength of the SOA in order to alleviate the gain modulation and phase modulation induced by probe signals.

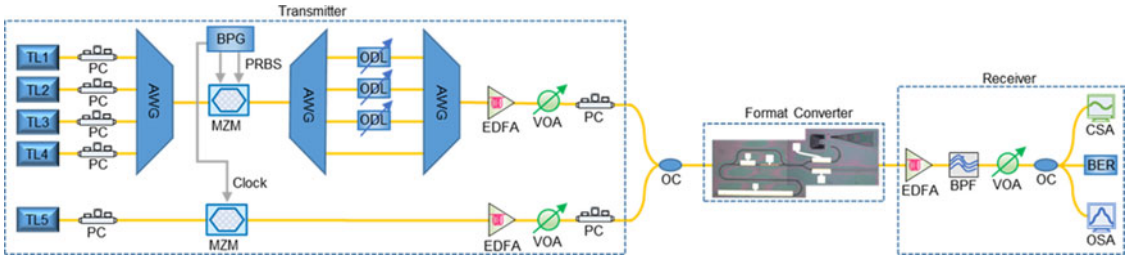

Fig. 7. The experimental setup. TL: tunable laser; PC: polarization controller; AWG: arrayed-waveguide grating; BPG: bit pattern generator; MZM: Mach-Zehnder Modulator; EDFA: erbium doped fiber amplifier; VOA: variable optical attenuation; OC: optical coupler; SOA: semiconductor optical amplifier; DI: delay interferometer; BPF: bandpass filter; CSA: communication signal analyzer; BERT: bit error ration test; OSA: optical spectrum analyzer.

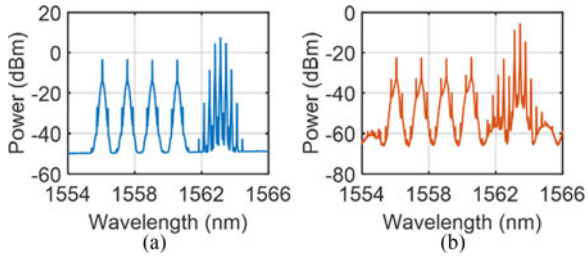

Fig. 8. Measured spectra. (a) NRZ signals and clock light input to the chip. (b) RZ signals and clock light output from the chip (res: 0.02 nm).

3. Experimental Setup and Results

The experimental setup is shown in Fig. 7. It consists of three sections: a transmitter, the integrated chip and a receiver. In the transmitter, four channels of continuous-wave (CW) lights are emitted from a multi-channels tunable laser at wavelengths of 1560.41 nm, 1558.93 nm, 1557.44 nm, 1555.95 nm, respectively. These four CW lights are coupled into a Mach-Zehnder modulator (MZM) with an AWG for generating the 40 Gb/s NRZ-OOK signals with a pseudorandom binary sequence length of $2^{31}-1$. And then a pair of AWGs with four optical delay lines are used to decorrelate the four WDM channels. The clock signal is generated by another MZM, with a center wavelength of 1563 nm. Then, the multichannel NRZ signals and clock signal are coupled into the integrated chip. The total input power level of the multichannel NRZ signals and the clock light are 4 dBm and 12 dBm, respectively. The chip temperature is well controlled at 25 °C to ensure the stable performance, the bias current of SOA1 is 270 mA. Finally, the converted RZ signals are filtered by a tunable optical bandpass filter (BPF) with a 3-dB bandwidth of 0.8 nm for latter analyzing. The spectra of output signals are measured by an optical spectrum analyzer (Yokogawa AQ6370C), and the eye diagrams of the signals are measured by a communication signal analyzer (Tektronix CSA 8000 B). And we also use an error analyzer (SHF 11104A) to measure the BER of the original NRZ signal and the converted RZ signals. The measured spectrums of the input signal to the chip and output signal from the chip are shown in Fig. 8(a) and (b) respectively. The result shows that the measured spectrum is similar to the schematic diagram in Fig. 6, which means that the format conversion scheme has been well implemented by the PIC.

For verifying the effectiveness of the format conversion from NRZ to RZ, we could evaluate the eye diagrams of converted signals. The corresponding eye diagrams are shown in Fig. 9. All the eye diagrams are measured at the same received power level. Fig. 9(a)–(d) shows the eye diagrams of the four input NRZ-OOK signals, respectively. The corresponding converted RZ-OOK signals are shown in Fig. 9(e)–(h). The RMS time jitter is less than 1.5 ps and the output extinction ratio is higher than 9.0 dB. The eye diagrams of the four-channel converted RZ-OOK signals are all clear and open, which indicate that the format conversion from NRZ-OOK to RZ-OOK are well achieved.

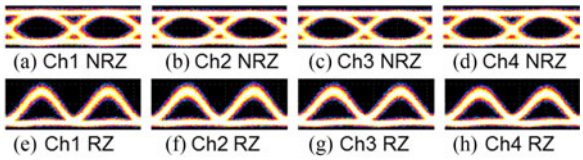

Fig. 9. Measured eye diagrams of all the channels. (a)–(d) Eye diagrams of the input NRZ signals. (e)–(h) Eye diagrams of the converted RZ signals (10 ps/div).

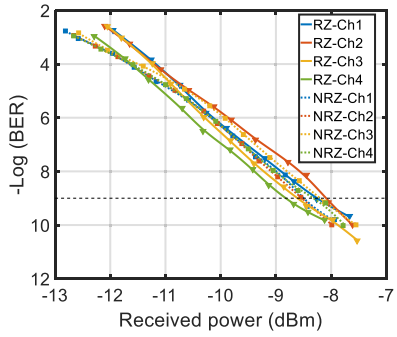

Fig. 10. Measured BER results for multi-channel format conversions from NRZ-to-RZ.

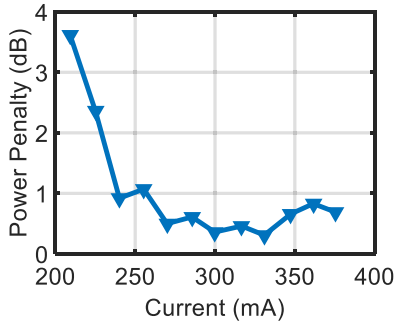

Fig. 11. Power penalty of the format conversion at different SOA bias current.

In order to further quantitatively assess the format conversion, we measure the BER curves as a function of the received power. The power penalties induced by the format conversion process are shown in Fig. 10. Different colourful dash-dotted lines are the BER curves for the original NRZ signals while the same colourful lines are the curves for the corresponding converted RZ signals. The average power penalty at BER of 1×10^{-9} of the four channels are all less than 0.5 dB, which mean that a high-quality multi-channel format conversion result can be obtained based on this PIC. And by optimizing and solving the mismatch of the DI's FSR and the ITU wavelength spacing, the chip will have the scalability of processing more channels simultaneously.

In order to obtain the good performance discussed before, the operation conditions have been optimized, including the SOA biased current, the input power of multichannel NRZ and clock light. The average power penalty as a function of the injected current is evaluated, as shown in Fig. 11, when the SOA biased current increases from 210 mA to 250 mA, the average power penalty of the four channels at BER of 1×10^{-9} decreases from 3.7 dB to less than 1 dB, because a larger XPM can be obtained when the current increase, but the power penalty will not decrease sharply while increase the biased current further. There is a minimum value of power penalty while the biased current is near 300 mA. For the integrated chip, if the biased current is too high, the thermal effect will influence its stability, so in this experiment, we set the biased current at 270 mA.

The effect of the input powers of the multichannel NRZ signals and the clock light is shown in Fig. 12. In principle, the clock light need to be strong enough for providing enough XPM effect

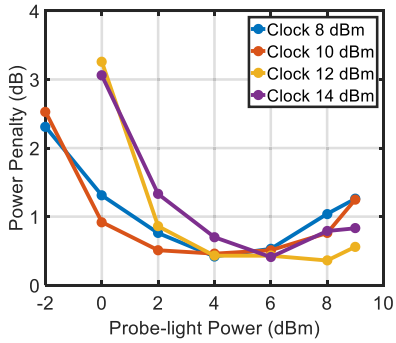

Fig. 12. Power penalty of the format conversion at different input power of the multichannel NRZ signals and the clock light.

in the SOA, and the probe signal power need to be far smaller than the power of clock light for reducing inter-channel crosstalk. For certain clock light power, there is an optimum input probe power, the probe power should not be too small in order to keep the signal to noise ratio (SNR) of the converted output signals. Results also show that larger clock light power is helpful for improving the conversion output performance, but too large clock power will cause decreasing of the converted output power. So, both the input power of the multichannel NRZ signals and the clock light need to be optimized. In this experiment, we set input powers of the multichannel NRZ signals and the clock light at 4 dBm and 12 dBm, respectively. Although we have optimized the operation conditions, the quantum-well material of the long SOA has not been special optimized for enhancing XPM effect and suppressing XGM effect, further work should take this aspect into consideration. That will be helpful for improving the output performance of multichannel signal processing.

4. Conclusion

In summary, we have designed and fabricated a photonic integrated chip with SOAs and a tunable DI as a multichannel photonic integrated signal processor. Utilizing this chip, we have experimentally demonstrated all-optical four-channel format conversions simultaneously from NRZ-OOK to RZ-OOK at 40 Gb/s. In particular, the conversion process has a high output performance with less than 0.5 dB power penalty. Moreover, this chip has the potential to be used for other parallel all-optical signal processing, such as multichannel wavelength conversion, parallel signal regeneration, and so on.

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