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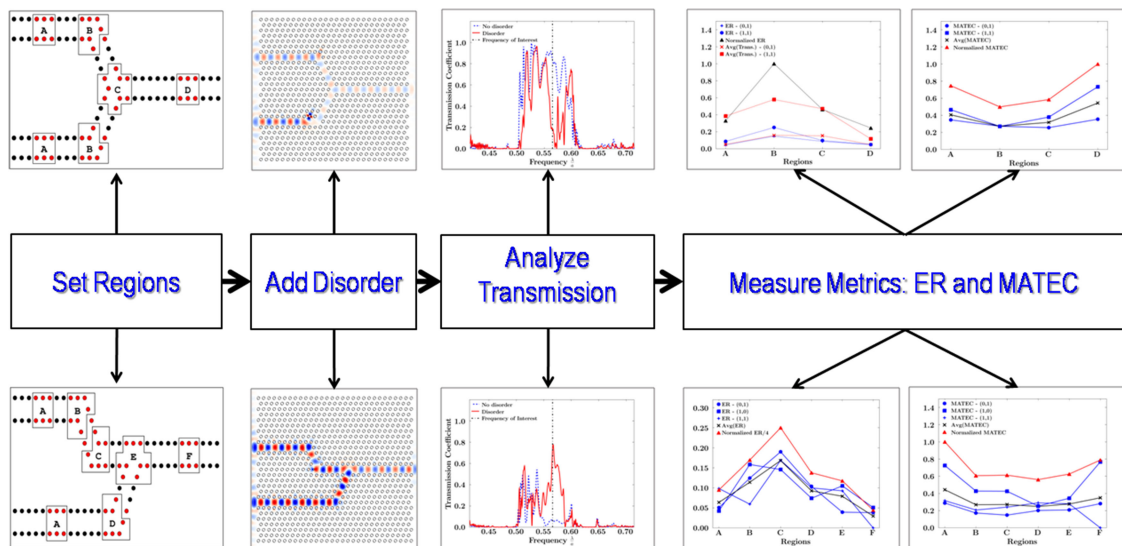# Effect of Structural Disorder on Photonic Crystal Logic Gates

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Effect of Structural Disorder on Photonic Crystal Logic Gates

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Abstract: In this paper, we study the effect of structural disorder on photonic crystals logic gates applying a new approach based on the evaluation of two metrics: the error rate (ER) and the mean absolute deviation of transmission of the error cases (MATEC). ER is the probability that a fabricated photonic crystal logic gate does not accomplish its logic function correctly, and MATEC measures the imperfection degree of the device through the transmission coefficient. The process consists in introducing disorder in specific regions in the boundary of the waveguides that form the logic gate structure. A significant number of simulations is randomly performed for each input combination of the logic gate. The ER and MATEC are calculated, and the process is replicated 20 times with different seed numbers. Finally, a statistical test T is carried out to establish the most critical regions for the device. We evaluate some photonic crystal logic gates with different lattice configurations using this approach. The results show that, for structures with a triangular lattice, regions in the corners and close to the output are more critical to ER and MATEC, respectively. For structures with a square lattice, we found that the intersection regions are the most sensitive for both metrics. As a final consideration, we remark that this methodology can be easily applied to evaluate other kinds of disorder and to analyze photonic crystals devices based on waveguides with different lattice configurations, and can guide the design of future robust gates.

Index Terms: Photonic crystal, logic gates, effect of disorder, robustness analysis.

1. Introduction

Photonic crystals (PhC) are devices that have awaken a great interest since their proposal in 1987, and even more after their experimental demonstration in 1991 [1]–[3]. Fundamentally, PhC are optical devices formed by a periodic modulation in a macroscopic media, usually a semiconductor material. In a two-dimensional PhC the arrangement of the refractive index is varied periodically along two directions, while in the third the medium is uniform [4]. A typical two dimensional PhC consists of a matrix of cylinders of air made in a semiconductor material such as Si or GaAs, or a matrix of cylinders of semiconductor material fabricated onto a semiconductor substrate. The behavior of photons in PhC is fundamentally equivalent to the behavior of electrons in peri-odic atomic potentials. Thus, photonic bands arise as a consequence of constructive interference

phenomena of electromagnetic waves, and photonic band gaps (PBG) occur as a result of destructive interference phenomena [4]. A PBG is the energy or frequency range where the light propagation is prohibited inside the PhC. When radiation with frequency inside the PBG arrives at the structure, it is completely reflected.

Due to this property, similar to the energy gap of electronic semiconductors, photonic crystals are promising for applications that include optical fibers, high-quality resonant cavities and filters, optical integrated circuits, waveguides, quantum and classical computing. Focusing on classical computing, logic gates are in the second abstraction level of the bottom-up hierarchy to build and design computational systems. Taking this into account, photonic crystal logic gates were demonstrated controlling the light beam interference effect trough PhC waveguides [5]–[7]. Nonlinear effects and easiness of fabrication are the principal advantages of using this approach.

To fabricate these logic gates, conventional techniques can be used, such as photolithograph, chemical etching, interference lithography, e-beam lithography and inductively-coupled plasma reactive-ion etching. Although these methods are robust and efficient, imperfections are inevitably introduced during the manufacturing process. Deviations of the radii and displacements of the cylinders from the ideal positions are the typical imperfections presented by a fabricated sample. In the literature, some studies have been reported analyzing the effect of such imperfections on the optical properties of photonic crystals waveguides by considering random disorder in the dielectric function of the system. Different kinds of disorder, such as variations in the filling fraction, in the refractive index, in the position and radius of the cylinders were investigated [8]–[14].

In this work, we study the effect of structural disorder, specifically deviations of the radii and displacement of the cylinders, on photonic crystals logic gates using a new approach based on the evaluation of two metrics: the error rate (ER) and the mean absolute deviation of transmission of the error cases (MATEC). A few logic gates are evaluated to analyze the robustness of these devices to possible defects arising in the fabrication process. This methodology can be easily applied to study the effect of other kinds of disorder on devices based on waveguides with different lattice configurations.

This manuscript is organized as follows: in Section II, we present an overview of PhC logic gates. Section III describes the methodology. Section IV details the obtained main results. A discussion about them and possible solutions to the problems found are presented in Section V. Finally, Section VI gathers the main conclusions.

2. Photonic Crystal Logic Gates

Logic gates can be accomplished with two-dimensional photonic crystals through the use of PhC waveguides. A waveguide is a device formed by introducing line defects in the PhC structure. These devices are employed to guide the electromagnetic radiation with small losses and very high efficiency [15]–[17]. Also, they allow to control the interference effects of light beams propagating throughout the waveguide. Taking advantage of this, logic gates can be projected according to the wave optics theory, in that, if the phase difference between two light beams is $2k\pi$ (where $k = 0, 1, 2, \ldots$), then constructive interference will occur, and the output light will have high power (corresponding to the logic state of 1). If the phase difference is $(2k + 1)\pi$ (where $k = 0, 1, 2, \ldots$), then destructive interference will occur, and the output light will be approximately zero (corresponding to the logic state of 0) [15].

Next, photonic crystal logic gates projected using this principle are detailed.

2.1 OR Gate

The OR logic gate proposed by Fu *et al.* [5], operating at the telecommunication wavelength of 1.5 μm, is composed of a triangular lattice of cylindrical silicon rods, with a dielectric constant of 11.56, embedded in a background medium of air (refractive index 1). The lattice constant and the diameter of the silicon rods are 875 nm and 495 nm, respectively. This logic gate is formed by two intersecting waveguides (inputs) at 10.5 μm to the cross point between them, forming an angle of

$120°$ and a phase difference of 0. Thus, if a single beam is injected into one of the inputs, the signal light can propagate to the output through the waveguide, and a logical value of 1 can be obtained in the output. When two beams are injected in both input ports simultaneously, a constructive interference occurs, and a high power is observed in the output. Obviously, when no single beam is injected into any input port, no light comes to the output, corresponding to the logical value of zero. Thus, the operation of a photonic crystal OR logic gate is demonstrated.

In the same way, but using a two-dimensional photonic crystal composed of a square lattice of cylindrical silicon rods, with a dielectric constant of 11.56, embedded in a background medium of air, D'Souza *et al.* [6] demonstrated the operation of another OR logic gate. The parameters of the structure are 650 nm for the lattice constant and 230 nm for the radii of the cylinders. The device is formed by a square ring resonator waveguide with three other linear waveguides which are connected to each other by the ring resonator. The principle is that the signal injected into the input waveguides split into two through the ring resonator, one travels in clockwise and the other in counterclockwise direction. Constructive interference occurs, and a larger output energy is obtained. The advantage of this device is that it can operate at different wavelengths around the 1.5 μm window.

2.2 XOR Gate

The XOR logic gate proposed by Fu *et al.* is achieved by controlling the destructive interference effect [5]. To accomplish this, the designed structure consists of two waveguides with one lattice constant of path difference to the cross point between them. When the inputs are excited simultaneously with an input power P_0, a phase difference of π generates a destructive interference, and the output signal is approximately zero ($0.0067P_0$). On the other hand, if only one input is excited, the output signal is greater than $0.75P_0$. Thus, considering transmissions greater than 0.70 and lower than 0.01 as logical values 1 and 0, respectively, an XOR logic gate is carried out. The contrast ratio between the output logic states 1 and 0 is high as 20 dB.

On the other hand, D'Souza *et al.*, using the same principle of operation presented in their OR gate [6], but engineering the ring resonator to produce a destructive interference, also demonstrated the XOR logic gate. This device can also operate with different wavelengths, and with a contrast ratio greater than 19 dB.

2.3 Majority Gate

The Majority gate is a logic device with three inputs and one output. The output is the majority function, thus, if at least two inputs are 0 then the output is 0. In contrast, the output is 1 if and only if at least two inputs are 1. This PhC gate was previously presented by our group [7].

Notice that, if one input is fixed at binary 0, an AND gate with two inputs is defined. In the same way, if one input is fixed at binary 1, an OR gate is obtained. This property allows the creation of simple and optimized computational circuits. A Majority gate is a basic logic device in other technologies, such as Quantum-dot Cellular Automata (QCA). In the same way, we believe that majority gates can be used to design optimized computational circuits in photonic crystals.

The schematic structure of the all-optical Majority gate is shown in Fig. 1(a). It is formed by three symmetrical optical waveguides: AY, BY, CY, of equal length. The lattice constant of this device is 875 nm. The diameter and the dielectric constant of the silicon rods are 495 nm and 11.56, respectively. With these parameters, the device will operate optimally for an optical wavelength of 1.5 μm.

Considering the input set (0, 1, 0), a single beam is injected into the input port B, then the signal light can propagate through the optical waveguide BY to the output Y. Since back-reflection losses is present through the propagation path, the signal reach the output Y with a transmission coefficient smaller than 0.35. This corresponds to a logic operation $Maj(0, 1, 0) = 0$, as shown in Fig. 1(b). Similarly, if a single beam is injected into input port A or C the same transmission value is obtained, corresponding to the logic operations $Maj(1, 0, 0) = 0$ and $Maj(0, 0, 1) = 0$, respectively [7].
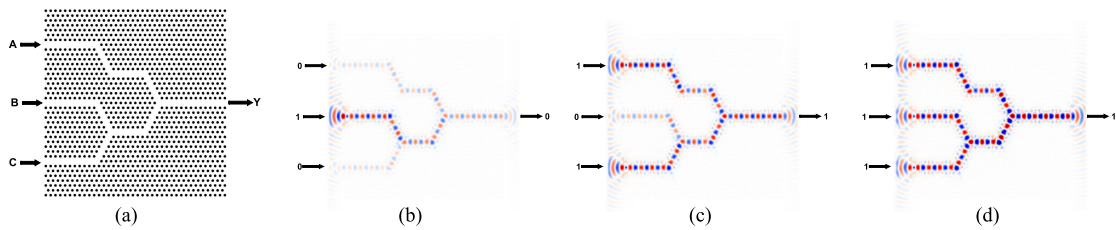
Fig. 1. Majority gate photonic crystal. (a) Dielectric distribution of the PhC structure. (b) Electric field E_z for (b) $Maj(0, 1, 0) = 0$, (c) $Maj(1, 0, 1) = 1$ and (d) $Maj(1, 1, 1) = 1$.
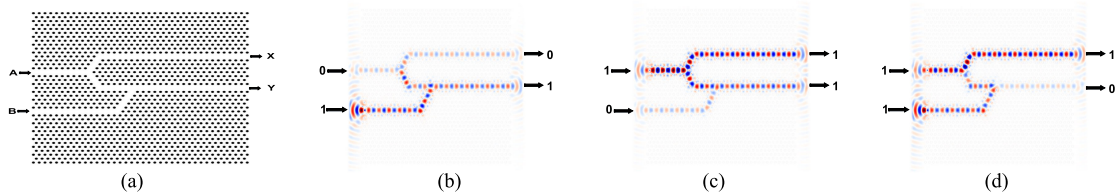

Fig. 2. Feynman gate Photonic crystal. a) Dielectric distribution of the PhC structure. Electric field E_z for b) $Feyn(0, 1) = (0, 1)$, c) $Feyn(1, 0) = (1, 1)$ and d) $Feyn(1, 1) = (1, 0)$.

When two beams are injected into two inputs ports, then the phase difference of these two signal light beams is zero. Constructive interference occurs, and the output signal has a transmission greater than 0.85. This corresponds to the logic operation $Maj(1, 0, 1) = 1$, as shown in Fig. 1(c). The same transmission value is obtained for the cases $Maj(0, 1, 1) = 1$ and $Maj(1, 1, 0) = 1$ [7].

Finally, if beams are injected into the three inputs ports, then the phase difference at the cross points is zero, causing a constructive interference, and achieving 1.00 of transmission. This corresponds to $Maj(1, 1, 1) = 1$, shown in Fig. 1(d). Obviously, when no single beam is injected into any input port, then no light comes to output, corresponding to $Maj(0, 0, 0) = 0$.

In summary, we can establish that when the transmission output is greater than 0.80 it is considered as logic output 1. If the transmission output is less than 0.4, then it is considered as logic output 0. The contrast ratio of this device is greater than 4 dB [7].

2.4 Feynman Gate

In 1961, Rolf Landauer argued that any irreversible computational process, e.g., AND, OR, XOR, implies the loss of $K_B T \ln 2$ joules per bit erased, where K_B is the Boltzmann constant and T is the temperature [18]. One possible solution is achieved by building the process using reversible primitives. These primitives, also known as reversible gates, are information preserving, i.e., they have a one-to-one relation (bijective functions) between inputs and outputs.

The Feynman gate is a reversible logic device with two inputs (A, B) and two outputs (X, Y). The outputs are defined by the function $X = A$ and $Y = A \oplus B$.

Photonic crystals have been pointed out as a promising technology for approaching the thermodynamic limit of computation, thus in an effort to go beyond that limit an all-optical Feynman gate is proposed, shown in Fig. 2(a). The structure parameters are the same used for the Majority Gate. This PhC logic gate was first presented by our group [7].

If a single light beam is injected into input port B, then the optical signal propagates to the outputs X and Y, with a transmission of 0.10 and 0.50, respectively. This corresponds to the logic operation $Feyn(0, 1) = (0, 1)$, as shown in Fig. 2(b). When a single beam is injected into input port A, then the optical signal propagates to both outputs X and Y with transmission greater than 0.40, as shown in Fig. 2(c). This corresponds to the logic operation $Feyn(1, 0) = (1, 1)$.

When the two input ports are excited, then the difference of the path length between the waveguide AY and BY is one lattice constant, and the phase difference is π. Therefore, destructive interference

occurs, and the transmission in the output Y is only 0.01. The transmission at the output X is 0.75. This corresponds to the logic operation $Feyn(1, 1) = (1, 0)$, as shown in Fig. 2(d). Finally, if no single beam is injected in both input ports, then no light comes to the output, corresponding to $Feyn(0, 0) = (0, 0)$ [7].

Summarizing, it is possible to observe transmissions ≥ 0.40 which are considered as logic output 1, and transmissions ≤ 0.10 which are considered as logic 0. This photonic logic gate has a contrast ratio of 6 dB [7].

3. Methodology

In the photonic crystal fabrication process, small amounts of disorder can arise in the structure that influence the performance of the device. Deviations of the radii and displacements of the cylinders from the ideal positions are the typical imperfections presented by a fabricated sample.

To simulate this behavior we define a relation between the position and radius of the original and final states of the cylinder, through the following state function:

$$\Phi_f(x_f, y_f, r_f) = \Phi_i(x_i + \Delta x, y_i + \Delta y, r_i + \Delta t), \tag{1}$$

where x_i and y_i are the Cartesian coordinates of the original position, and r_i is the ideal radius of the cylinder. Δx, Δy and Δr are randomly generated with a Gaussian probability, centered at $\mu = 0$ and with standard deviation $\sigma = 20$. We applied this standard deviation to produce disorder of around 80 nm, at the higher bound of the order of the disorder typically found in these systems, and that is capable to generate unexpected behavior in the performance of the photonic crystal logic gates. x_f, y_f and r_f are the components of the final state Φ_f.

In order to better understand how the disorder affects the performance, we define some regions for each logic device. Several works have demonstrated that imperfections introduced in the cylinders that are not close to the boundary layer of the waveguide, do not affect significantly its performance, while the cylinders in the boundary layer are vital to ensure the functionality of the device [8], [13]. For this reason, in this work, we define each region as a set of n cylinders positioned in the boundary layer surrounding the waveguide. For each one of them, we performed $w \cdot n$ simulations for each input combinations of the logic gate, where w is a multiplicative factor of the cylinders, used to obtain the number of simulations per region. Then, we calculate the error rate (ER) and the mean absolute deviation of transmission of the error cases (MATEC) occurred during the simulations.

ER is the ratio between the number of errors and the number of simulations, described by the following equation:

$$ER = \frac{1}{w \cdot n} \sum_{k=1}^{w \cdot n} \Gamma(t_{f_k}, t_i, \tau), \tag{2}$$

where Γ is a function used to compute an error according to the following rule:

1) Return 1, if the output of the logic operation is 1 and the difference between t_i and t_{f_k} is greater than τ, or if the output of the logic operation is 0 and the difference between t_{f_k} and t_i is greater than τ
2) Otherwise, Return 0.

t_{f_k} and t_i are the transmissions of the device with and without disorder, respectively, and τ is the tolerance value.

MATEC is the mean absolute deviation of the transmissions of the error cases, formally:

$$\text{MATEC} = \frac{1}{n_e} \sum_{k=1}^{n_e} \left| t_{f_k} - t_i \right|, \tag{3}$$

where n_e is the number of errors over the total number of simulations. These values are only measured for the cases when ER $= 1$.

To generate a significant cluster sampling, as indicated by Jain [19], we replicate this process 20 times with different seed numbers. Then, we compute the global average (GA) and the global
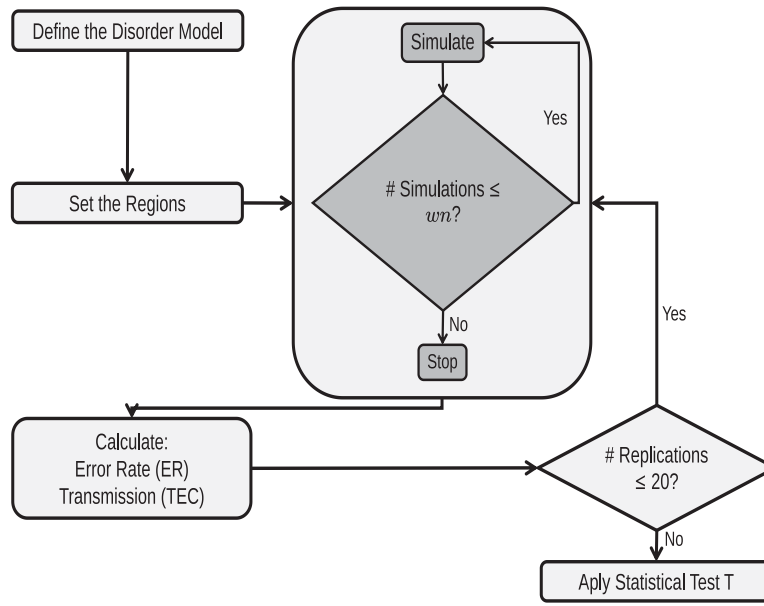
Fig. 3. Flux diagram to accomplish the analysis of the effect of disorder on photonic crystal logic gates.

standard deviation (GSD) for the ER and MATEC. To achieve this, we create a global set with a length of $20 \cdot \theta$, where θ is the number of logic gate input configurations evaluated. Thus, we guarantee the convergence of our method as a result of the larger number of sample data generated.

Finally, we apply a statistical test T between the two regions with greater GA [19]. This test allows us to establish the most critical region for each device and metric through the confidence interval (CI). Thus, if CI does not include 0, we can prove at a specific confidence level that the device is most sensitive to disorder introduced in the region with greater GA. Otherwise, the device presents the same sensitivity to both regions. Also, we normalize the GA of the two metrics using the max-min normalization rule. Fig. 3 shows the flux diagram to apply this process to photonic crystal logic gates.

We apply this methodology to analyze an OR and an XOR logic gates with triangular and square lattice configurations. Also, we investigate the Majority and Feynman gates. We set a tolerance $\tau = 0.1$, as usual for electronic devices. In order to obtain a high assurance, we establish a confidence level in 95% to perform the test T. The simulations were carried out with the finite difference time-domain (FDTD) method using the MIT software package, MEEP [20]. We excited the inputs of the logic gates with our wavelength of interest, $\lambda = 1550$ nm, which is the standard for telecommunications.

Then, for the logic gates with a square lattice, we apply a Gaussian source with centered frequency 0.42695 $\left(\frac{c}{a}\right)$ and with of 0.1009 $\left(\frac{c}{a}\right)$, where c is the speed of light in vacuum and a the lattice constant. The Perfectly Matched Layer (PML) for these devices was set in one lattice parameter. For the devices with triangular lattice, we use a Gaussian source centered at 0.5645 $\left(\frac{c}{a}\right)$ and width of 0.3001 $\left(\frac{c}{a}\right)$. We set a PML in one lattice constant for these devices.

4. Results

In this section, we report the main results obtained applying the process described previously. It is important to highlight that we plot the normalized GA of the error rate divided by 4, in order to get a better data visualization.

To study the effect of disorder on the photonic crystal logic gates of triangular lattice proposed by Fu *et al.* [5], we defined the regions illustrated in Fig. 4(a) and (b) for the OR and XOR, respectively.
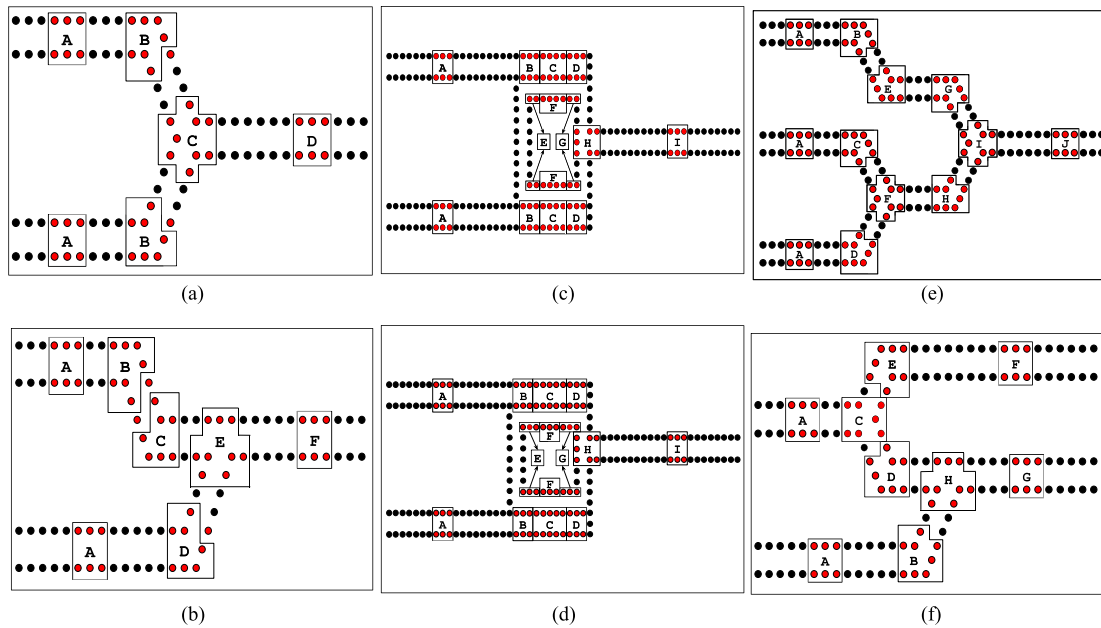
Fig. 4. Regions defined to analyze the effect of disorder on photonic crystal logic gates for (a) the OR structure proposed by Fu *et al.* [5]; (b) the XOR structure also proposed in [5]; (c) the OR structure proposed by D'Souza *et al.* [6]; (d) the XOR structure also proposed in [6]; (e) Majority gate studied by Caballero *et al.* [7]; f) Feynman gate [7].

TABLE 1

ER and MATEC of the Effect of Disorder on the OR Gate Proposed by Fu *et al.* [5]

	OR - Fu *et al.* [5]					
	ER × 10			MATEC		
R	**(0,1)**	**(1,1)**	**GA ± GSD**	**(0,1)**	**(1,1)**	**GA ± GSD**
A	0.45 ± 0.47	0.86 ± 0.64	0.65 ± 0.34	**0.34 ± 0.09**	**0.46 ± 0.11**	**0.40 ± 0.11**
B	**1.48 ± 0.66**	**2.50 ± 1.08**	**1.99 ± 0.66**	0.27 ± 0.04	0.27 ± 0.04	0.27 ± 0.04
C	**0.87 ± 0.68**	**0.97 ± 0.66**	**0.92 ± 0.33**	0.25 ± 0.02	0.37 ± 0.08	0.31 ± 0.08
D	0.48 ± 0.50	0.49 ± 0.54	0.48 ± 0.25	**0.36 ± 0.05**	**0.73 ± 0.16**	**0.55 ± 0.22**

Table 1 shows the ER and MATEC obtained for the OR gate for two different inputs sets: (0, 1) and (1, 1). As can be observed, regions B and C are the most sensitive to ER. Then, we applied the test T between these regions. For region B, the computed GA is 0.1996, and its GSD is 0.0662. For region C, we obtained GA = 0.0922 and GSD = 0.0331. The calculated confidence interval (CI) from the test T is (0.0749, 0.1399). The CI does not include 0. Thus, we proved that region B is the most critical to ER metric with 95% of confidence level. Fig. 5(a) shows the results for this metric and the normalized average. For MATEC, we applied the test between regions A and D, evidently, the most critical regions to this metric. We obtained GA = 0.4060 and GSD = 0.1176 for region A, while for region D the GA is 0.5541 and its GSD is 0.2275. The calculated CI from the test T is (0.0670, 0.2291). In this way, we demonstrated that region D is the most sensitive to MATEC with 95% of confidence level as a result that the CI does not include 0. Fig. 6(a) shows the results for this metric and the normalized average.
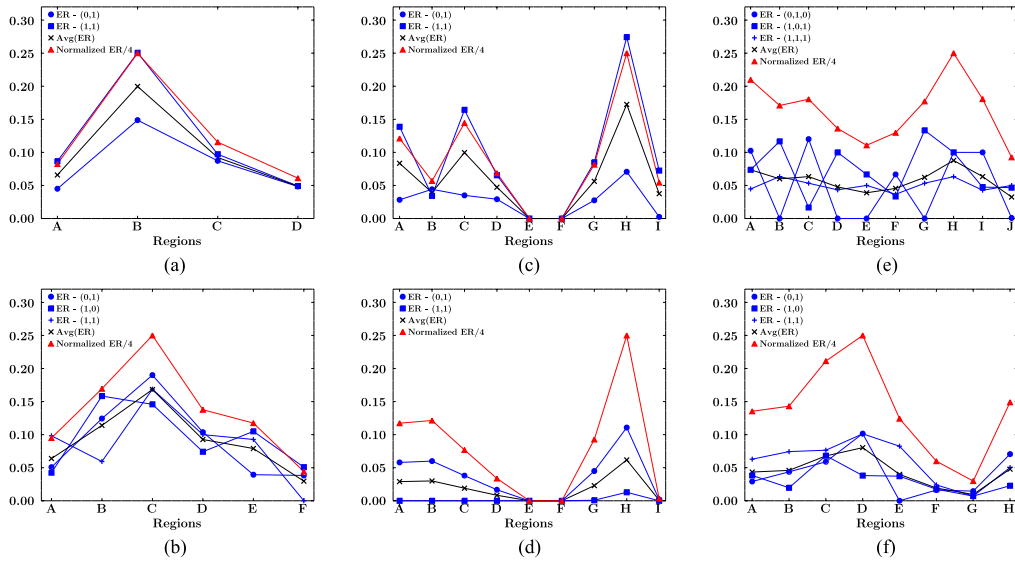
Fig. 5. Error Rate (ER) of the effect of disorder on photonic crystal logic gates. (a) OR by Fu *et al.* [5]; (b) XOR by Fu *et al.* [5]; (c) OR by D'Souza *et al.* [6] (d) XOR by D'Souza *et al.* [6]; (e) Majority Gate [7]; (f) Feynman Gate [7].
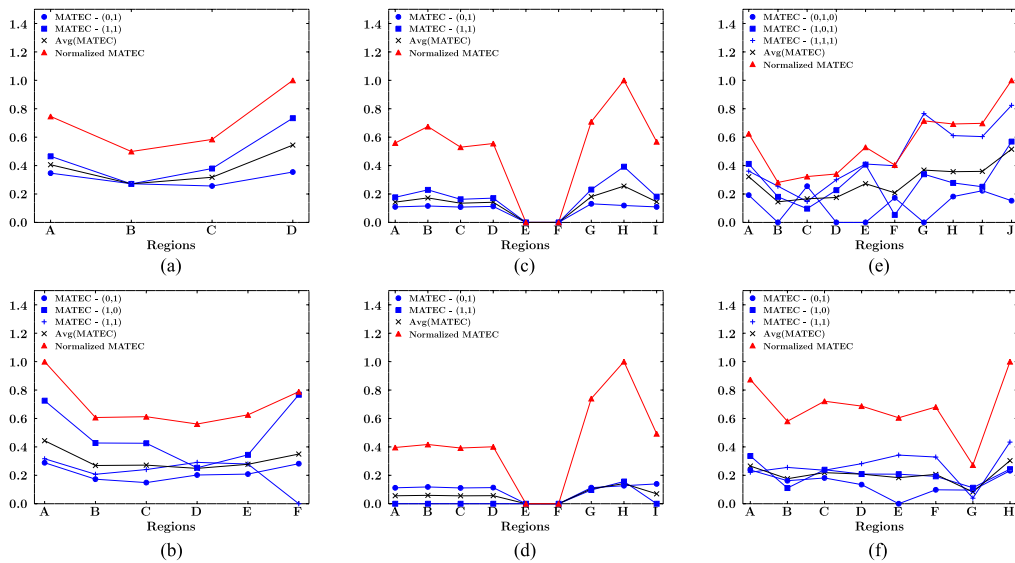
Fig. 6. Mean absolute deviation of the transmission of error cases (MATEC) of the effect of disorder on PhC logic gates. a) OR by Fu *et al.* [5]; b) XOR by Fu *et al.* [5]; c) OR by D'Souza *et al.* [6]; d) XOR by D'Souza *et al.*[6]; e) Majority Gate [7]; and f) Feynman Gate [7].

For the XOR gate of Fu *et al.*, the obtained results are shown in Table 2. Regions B and C are the most critical to ER metric. Then, the obtained CI from the test T between these regions is $(0.03658, 0.0717)$ as a result of a GA = 0.1140 and GSD = 0.056 for region B, while for region C the GA is 0.1681 and its GSD is 0.041. Thus, we proved that region C is the most sensitive to ER with 95% of confidence level due to the CI does not include 0. Fig. 5(b) shows the results for ER metric and the normalized average. For MATEC, we applied the test between regions A and F, clearly the most sensitive to this metric. The computed GA and GSD for region A are 0.4434 and 0.2038, respectively. For region F we obtained a GA = 0.3496 and GSD = 0.2467. The test

TABLE 2

ER and MATEC of the Effect of Disorder on the XOR Gate Proposed by Fu *et al.* [5]

	ER $\times$ 10				MATEC			
R	(0,1)	(1,0)	(1,1)	GA $\pm$ GSD	(0,1)	(1,0)	(1,1)	GA $\pm$ GSD
A	0.50 $\pm$ 0.52	0.42 $\pm$ 0.67	0.98 $\pm$ 0.56	0.63 $\pm$ 0.37	**0.28 $\pm$ 0.02**	**0.72 $\pm$ 0.18**	**0.31 $\pm$ 0.10**	**0.44 $\pm$ 0.20**
B	**1.24 $\pm$ 0.86**	**1.58 $\pm$ 0.97**	**0.59 $\pm$ 0.48**	**1.14 $\pm$ 0.56**	0.17 $\pm$ 0.03	0.42 $\pm$ 0.19	0.20 $\pm$ 0.12	0.26 $\pm$ 0.12
C	**1.90 $\pm$ 0.77**	**1.45 $\pm$ 0.85**	**1.68 $\pm$ 0.73**	**1.68 $\pm$ 0.41**	0.14 $\pm$ 0.02	0.42 $\pm$ 0.16	0.24 $\pm$ 0.06	0.27 $\pm$ 0.12
D	1.03 $\pm$ 0.53	0.74 $\pm$ 0.66	1.00 $\pm$ 0.59	0.92 $\pm$ 0.31	0.20 $\pm$ 0.04	0.25 $\pm$ 0.16	0.29 $\pm$ 0.10	0.24 $\pm$ 0.06
E	0.39 $\pm$ 0.41	1.05 $\pm$ 0.75	0.92 $\pm$ 0.39	0.79 $\pm$ 0.38	0.20 $\pm$ 0.05	0.34 $\pm$ 0.16	0.27 $\pm$ 0.14	0.27 $\pm$ 0.08
F	0.38 $\pm$ 0.60	0.50 $\pm$ 0.52	0.00 $\pm$ 0.00	0.29 $\pm$ 0.31	**0.28 $\pm$ 0.03**	**0.76 $\pm$ 0.06**	**0.00 $\pm$ 0.00**	**0.34 $\pm$ 0.24**

TABLE 3

ER and MATEC of the Effect of Disorder on the OR Gate Proposed by D'Souza *et al.* [6]

	ER $\times$ 10			MATEC		
R	(0,1)	(1,1)	GA $\pm$ GSD	(0,1)	(1,1)	GA $\pm$ GSD
A	0.28 $\pm$ 0.41	1.38 $\pm$ 0.54	0.83 $\pm$ 0.39	0.10 $\pm$ 0.00	0.17 $\pm$ 0.02	0.14 $\pm$ 0.03
B	0.44 $\pm$ 0.53	0.34 $\pm$ 0.25	0.39 $\pm$ 0.20	0.11 $\pm$ 0.00	0.22 $\pm$ 0.01	0.17 $\pm$ 0.13
C	**0.35 $\pm$ 0.44**	**1.64 $\pm$ 0.55**	**0.99 $\pm$ 0.69**	0.10 $\pm$ 0.01	0.16 $\pm$ 0.01	0.13 $\pm$ 0.02
D	0.29 $\pm$ 0.11	0.65 $\pm$ 0.36	0.47 $\pm$ 0.24	0.11 $\pm$ 0.01	0.17 $\pm$ 0.05	0.14 $\pm$ 0.03
E	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00
F	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00
G	0.27 $\pm$ 0.53	0.85 $\pm$ 0.66	0.56 $\pm$ 0.48	**0.13 $\pm$ 0.01**	**0.23 $\pm$ 0.11**	**0.18 $\pm$ 0.05**
H	**0.70 $\pm$ 0.57**	**2.74 $\pm$ 0.76**	**1.72 $\pm$ 1.08**	**0.11 $\pm$ 0.01**	**0.39 $\pm$ 0.05**	**0.25 $\pm$ 0.05**
I	0.02 $\pm$ 0.13	0.72 $\pm$ 0.70	0.37 $\pm$ 0.42	0.10 $\pm$ 0.00	0.18 $\pm$ 0.03	0.14 $\pm$ 0.02

T at 95% of confidence level failed for this case. However, for 90% of confidence level the CI is (0.01422, 0.1735). Thus, we demonstrated that region A is the most sensitive. This results and the normalized average are displayed in Fig. 6(b).

In order to evaluate the logic gates of square lattice proposed by D'Souza *et al.* [6], we defined the regions illustrated in Fig. 4(c) and (d) for the OR and XOR, respectively.

Table 3 shows the obtained results for the OR gate of D'Souza *et al.* We found that regions C and H are the most sensitive to ER metric. Then, for region C, the computed GA is 0.0996 while its GSD is 0.0690. For region H we obtained a GA = 0.1724 and GSD = 0.1083. The calculated CI from the test T is (0.0329, 0.1126).

For MATEC, regions G and H are the most critical to this metric. Thus, we obtained a GA = 0.1811 and GSD = 0.0589 for region G, while for region H the GA is 0.2556 and its GSD is 0.0579. The computed CI for MATEC is (0.0439, 0.1048). Thus, due to the fact that the calculated

TABLE 4

ER and MATEC of the Effect of Disorder on the XOR Gate Proposed by D'Souza *et al.* [6]

	XOR - D'Souza *et al.* [6]					
	ER $\times$ 10			MATEC		
R	(0,1)	(1,1)	GA $\pm$ GSD	(0,1)	(1,1)	GA $\pm$ GSD
A	0.58 $\pm$ 0.32	0.00 $\pm$ 0.00	0.29 $\pm$ 0.55	0.11 $\pm$ 0.01	0.00 $\pm$ 0.00	0.05 $\pm$ 0.00
B	**0.60 $\pm$ 0.37**	**0.00 $\pm$ 0.00**	**0.30 $\pm$ 0.37**	0.11 $\pm$ 0.02	0.00 $\pm$ 0.00	0.05 $\pm$ 0.00
C	0.38 $\pm$ 0.65	0.00 $\pm$ 0.00	0.19 $\pm$ 0.21	0.11 $\pm$ 0.01	0.00 $\pm$ 0.00	0.05 $\pm$ 0.00
D	0.16 $\pm$ 0.30	0.00 $\pm$ 0.00	0.08 $\pm$ 0.13	0.11 $\pm$ 0.01	0.00 $\pm$ 0.00	0.05 $\pm$ 0.00
E	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00
F	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00
G	0.44 $\pm$ 0.61	0.01 $\pm$ 0.08	0.22 $\pm$ 0.30	**0.11 $\pm$ 0.01**	**0.09 $\pm$ 0.02**	**0.10 $\pm$ 0.01**
H	**1.10 $\pm$ 0.78**	**0.12 $\pm$ 0.23**	**0.61 $\pm$ 0.56**	**0.12 $\pm$ 0.01**	**0.15 $\pm$ 0.00**	**0.14 $\pm$ 0.00**
I	0.01 $\pm$ 0.11	0.00 $\pm$ 0.00	0.00 $\pm$ 0.00	0.13 $\pm$ 0.00	0.00 $\pm$ 0.00	0.06 $\pm$ 0.00

CIs for ER and MATEC do not include 0, we proved that region H is the most sensitive region for both metrics with 95% of confidence level, as shown in Figs. 5(c) and 6(c), respectively.

Table 4 details the ER and MATEC results for the XOR gate of D'Souza *et al.* As can be observed, regions B and H are the most critical to ER. Then, we applied the test T between these regions. For region B, we obtained a GA = 0.0300 and GSD = 0.0377, while for region H the GA and GSD are 0.0617 and 0.0566, respectively. The computed CI for this metric is (0.0106, 0.0528).

For MATEC, we applied the test between regions G and H, clearly, the most sensitive regions to this metric. Thus, for region G, we obtained a GA = 0.1048 and GSD = 0.0103, while for region H the GA is 0.1415 and its GSD is 0. The CI obtained from the test is (0.0400, 0.1488). As has been noted, the CIs for ER and MATEC do not include 0, and then we demonstrated that region H is the most critical to both metrics at 95% of confidence level, as shown in Figs. 5(d) and Fig. 6(d).

To study the Majority logic gate, we defined ten regions displayed in Fig. 4(e). The obtained results for ER and MATEC are detailed in Table 5. As can be observed, regions A and H are the most sensitive to ER. Then, we applied the test T between these regions. For region A the computed GA and GSD are 0.0736 and 0.0030, respectively. For region H, we obtained a GA = 0.0877 and GSD = 0.0090. The computed CI from the test T is (0.0138, 0.0143). Thus, we proved at 95% of confidence level that region H is the most critical to ER considering that the CI does not include 0. Fig. 5(e) shows the results and the normalized average for ER.

For MATEC, we applied the test between regions G and J, evidently the most sensitive to this metric. Then, for region G the computed GA is 0.3683, and its GSD is 0.0534, while for region J we obtained a GA = 0.5152 and GSD = 0.0748. The calculated CI for MATEC is (0.1236, 0.1702). As it has been noted, the CI does not include 0, and thus we demonstrated with 95% of confidence level that region J is the most sensitive to MATEC. Fig. 6(e) shows the results and the normalized average for this metric.

Finally, we investigated the effect of disorder on the Feynman gate. We defined the regions illustrated in Fig. 4(f) to evaluate this device. The obtained results for ER and MATEC are detailed in Table 6.

As can be observed, regions C and D are the most critical to ER. Then, we applied the test T between these regions. For region C the computed GA is 0.0678, and its GSD is 0.03305, while for region D the GA and GSD are 0.0803 and 0.0277, respectively. The calculated CI for ER is (0.0004, 0.0201). As has been noted the CI does not include 0, and thus we proved that region D

TABLE 5

ER and MATEC of the Effect of Disorder on the Majority Gate [7]

	Majority gate [7]							
	ER × 10				MATEC			
R	(0,1,0)	(1,0,1)	(1,1,1)	GA ± GSD	(0,1,0)	(1,0,1)	(1,1,1)	GA ± GSD
A	**1.02 ± 0.28**	**0.73 ± 0.36**	**0.44 ± 0.43**	**0.73 ± 0.00**	0.19 ± 0.06	0.41 ± 0.12	0.36 ± 0.11	0.32 ± 0.04
B	0.00 ± 0.00	1.16 ± 0.20	0.63 ± 0.49	0.60 ± 0.01	0.00 ± 0.00	0.18 ± 0.05	0.25 ± 0.08	0.14 ± 0.02
C	1.20 ± 0.21	0.16 ± 0.14	0.53 ± 0.40	0.63 ± 0.00	0.25 ± 0.08	0.09 ± 0.03	0.14 ± 0.04	0.16 ± 0.02
D	0.00 ± 0.00	1.00 ± 0.29	0.43 ± 0.34	0.47 ± 0.00	0.00 ± 0.00	0.22 ± 0.07	0.30 ± 0.09	0.17 ± 0.02
E	0.00 ± 0.00	0.66 ± 0.30	0.50 ± 0.34	0.38 ± 0.01	0.00 ± 0.00	0.40 ± 0.12	0.41 ± 0.12	0.27 ± 0.03
F	0.66 ± 0.28	0.33 ± 0.35	0.36 ± 0.13	0.45 ± 0.00	0.17 ± 0.05	0.05 ± 0.02	0.39 ± 0.12	0.20 ± 0.03
G	0.00 ± 0.00	1.33 ± 0.07	0.53 ± 0.22	0.62 ± 0.01	**0.00 ± 0.00**	**0.33 ± 0.10**	**0.76 ± 0.23**	**0.36 ± 0.05**
H	**1.00 ± 0.30**	**1.00 ± 0.27**	**0.63 ± 0.37**	**0.87 ± 0.00**	0.18 ± 0.06	0.27 ± 0.08	0.61 ± 0.19	0.35 ± 0.05
I	1.00 ± 0.34	0.47 ± 0.20	0.42 ± 0.20	0.63 ± 0.00	0.22 ± 0.07	0.25 ± 0.08	0.60 ± 0.18	0.35 ± 0.05
J	0.01 ± 0.27	0.46 ± 0.35	0.50 ± 0.13	0.32 ± 0.20	**0.15 ± 0.05**	**0.56 ± 0.17**	**0.82 ± 0.25**	**0.51 ± 0.07**

TABLE 6

ER and MATEC of the Effect of Disorder on the Feynman Gate [7]

	Feynman gate [7]							
	ER × 10				MATEC			
R	(0,1)	(1,0)	(1,1)	GA ± GSD	(0,1)	(1,0)	(1,1)	GA ± GSD
A	0.29 ± 0.29	0.38 ± 0.39	0.62 ± 0.37	0.43 ± 0.25	**0.23 ± 0.45**	**0.33 ± 0.59**	**0.22 ± 0.55**	**0.26 ± 0.12**
B	0.43 ± 0.36	0.19 ± 0.12	0.74 ± 0.36	0.45 ± 0.20	0.16 ± 0.54	0.11 ± 0.18	0.25 ± 0.55	0.17 ± 0.09
C	**0.58 ± 0.36**	**0.68 ± 0.47**	**0.76 ± 0.54**	**0.67 ± 0.33**	0.18 ± 0.55	0.23 ± 0.71	0.23 ± 0.82	0.21 ± 0.16
D	**1.01 ± 0.34**	**0.38 ± 0.33**	**1.01 ± 0.49**	**0.80 ± 0.27**	0.13 ± 0.51	0.20 ± 0.50	0.28 ± 0.74	0.20 ± 0.13
E	0.00 ± 0.00	0.37 ± 0.29	0.82 ± 0.34	0.39 ± 0.17	0.00 ± 0.00	0.20 ± 0.44	0.34 ± 0.51	0.18 ± 0.08
F	0.16 ± 0.33	0.17 ± 0.18	0.23 ± 0.00	0.19 ± 0.12	0.09 ± 0.50	0.19 ± 0.27	0.32 ± 0.00	0.20 ± 0.06
G	0.14 ± 0.16	0.07 ± 0.23	0.07 ± 0.25	0.09 ± 0.15	0.09 ± 0.24	0.11 ± 0.35	0.03 ± 0.38	0.08 ± 0.07
H	0.70 ± 0.40	0.22 ± 0.24	0.50 ± 0.26	0.47 ± 0.21	**0.23 ± 0.59**	**0.24 ± 0.36**	**0.43 ± 0.38**	**0.32 ± 0.10**

is the most sensitive to ER at 95% of confidence level. Fig. 5(f) shows the results for this metric and the normalized average. For MATEC, we applied the test between regions A and H, obviously the most sensitive regions to this metric. Then, for region A, we obtained a GA = 0.2650 and GSD = 0.1249. For region H, the computed GA is 0.3217, and its GSD is 0.1052. The calculated CI for this metric is (0.0274, 0.0858). Thus, we demonstrated with 95% of confidence level that region H is the most critical to MATEC as a result that the CI does not include 0. Fig. 6(f) shows the results and the normalized average for this metric.

Lastly, we found that regions in the corners of a structure with triangular lattice are more critical to the ER while the regions close to the outputs are worst for the MATEC. On the other hand, for the logic gates with a square lattice, the highest sensitivity is located in the intersection regions. Also,
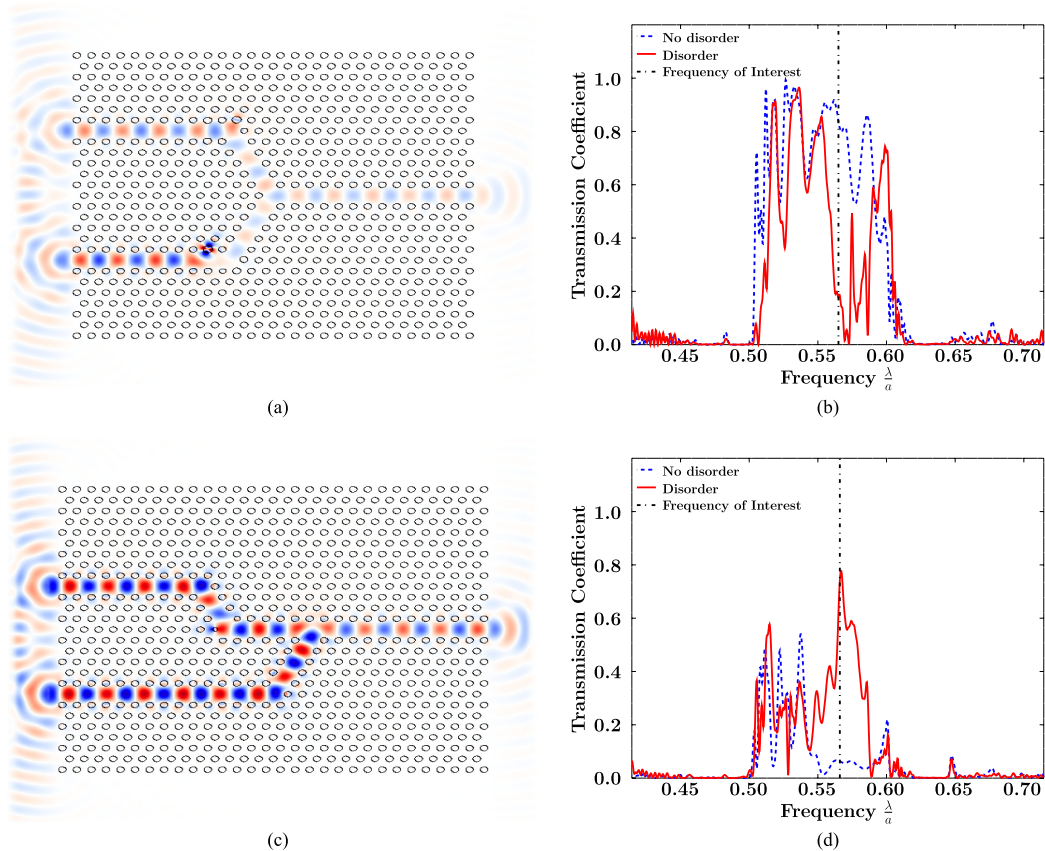
Fig. 7. Electric field E_z for an example of a photonic crystal with a triangular lattice, with disorder projected to generate (a) constructive interference and (c) destructive interference. Transmission coefficient of the device with and without disorder for structures projected to represent (b) constructive interference and (d) destructive interference.

we discovered that regions E and F do not influence the performance of these devices. In addition to this, the Feynman gate has show to be the most robust device for ER and MATEC within the PhC logic gates formed by a triangular lattice. For the logic gates formed by a square lattice, the XOR is the most robust for ER while for MATEC is the OR.

5. Discussion

The obtained results show that the ER and MATEC are metrics that allow us to evaluate the effect of structural disorder and to establish the region for which we must be more careful to manufacture a photonic crystal logic gate. It is important to note that these metrics are correlated through the error. Here, we consider an error when the expected logic gate output value is inverted.

In this way, we found that for particular geometrical configurations of the cylinders of each region with introduced disorder, the photonic crystal logic gate does not accomplish its logic function correctly.

To explain this behavior, we choose a photonic crystal OR gate with a triangular lattice, and with introduced disorder in the region with greater ER (region B for this case). This device is projected to generate a constructive interference when the two inputs waveguides are excited, and a high transmission must be obtained. In contrast, a very low transmission is obtained due to the effect of the disorder, see Fig. 7(a). We analyzed the electromagnetic modes and the photonic band gap (PBG) of this structure, and we found that the transmission for some frequencies of our interest
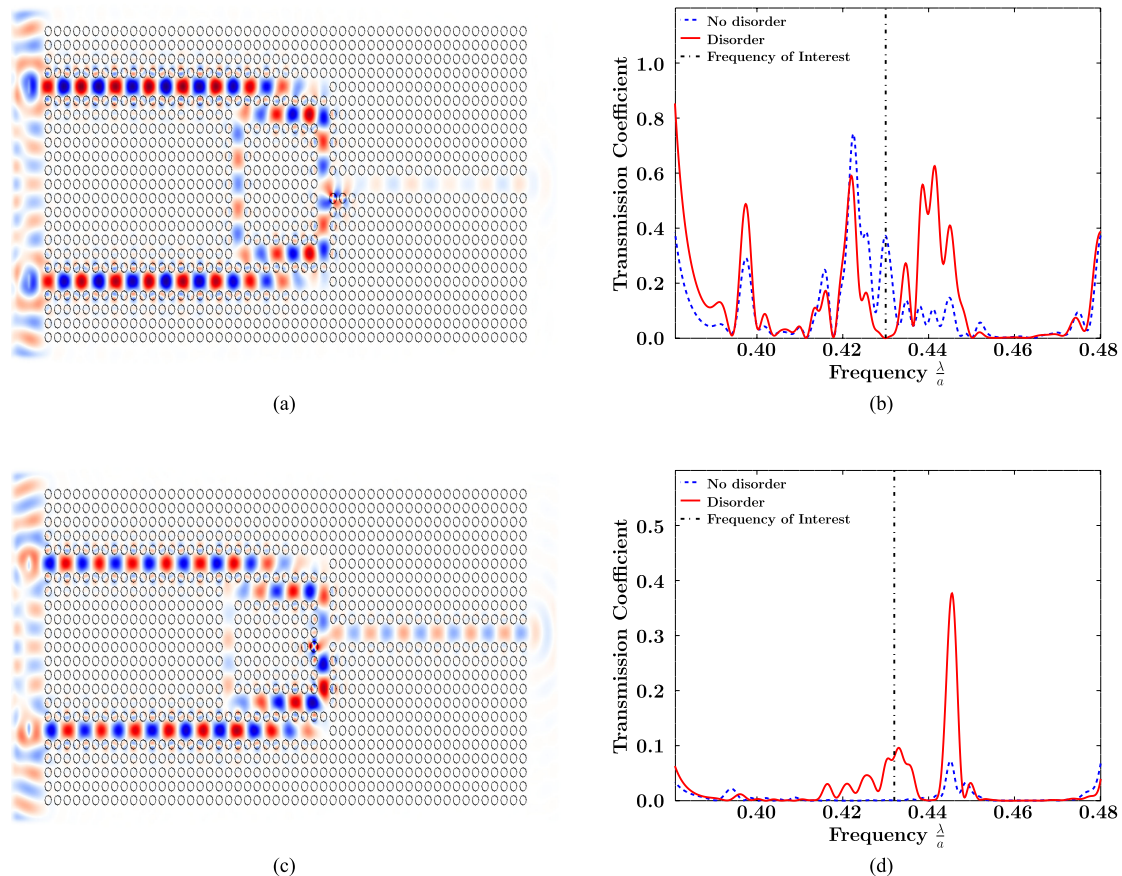
Fig. 8. Electric field E_z for an example of a photonic crystal with a square lattice, with disorder projected to generate (a) constructive interference and (c) destructive interference. Transmission coefficient of the device with and without disorder for structures projected to represent (b) constructive interference and (d) destructive interference.

(0.56 $\frac{c}{a}$ in this case) swapped, as illustrated in Fig. 7(b). We observed that disorder can create point defects (cavities) in the photonic crystal logic gate and these can push up or down a single mode as well as narrow the PBG.

We applied the same process for the XOR logic gate with a triangular lattice. We choose a sample with introduced disorder in the region C. In this case, the device is projected to generate a destructive interference when the two input waveguides are excited. However, a high transmission coefficient is obtained, as illustrated in Fig. 7(c). As can be observed, the transmission of some frequencies of our interest also swapped, as shown in Fig. 7(d).

A similar behavior is observed for structures with a square lattice. Then, for the OR gate, we choose a PhC sample with introduced disorder in the region H. This device is also projected to generate a constructive interference when the two inputs waveguides are excited, nevertheless a low power is obtained for the geometrical configuration illustrated in Fig. 8(a). The transmission coefficient for this case is shown in Fig. 8(b). We can observe that for the frequencies of our interest (0.42 $\frac{c}{a}$ in this case), the transmission coefficient of the structure with disorder is inverted with respect to the non-disordered one.

For the XOR gate with a square lattice, we choose a photonic crystal sample with disorder in the region H. This device was originally projected to generate a destructive interference and a low power in the output when the two inputs waveguides are excited. However, a high power is obtained due to the effect of disorder, as shown in Fig. 8(c). As can be observed in Fig. 8(d), the transmission

coefficient of the frequency of our interest for the structure with disorder is inverted again when compared with the non-disordered structure.

As a final consideration, we stress that the methodology proposed here can be easily applied to study the effect of disorder on devices based on photonic crystals waveguides with different lattice configuration. Here, we have focused on structural disorder because it is usually the dominant effect in state-of-art samples and experimental measurements can be fully reproduced by considering only such type of disorder [21]. In addition to this, we believe that a certain degree of surface roughness in the cylinders will effectively give us an equivalent result of hole-size or hole-position random deviations. Also, adjusting the standard deviation of the Gaussian distribution and with a simple modification of the state function Φ, we can apply this approach to evaluate other kinds of disorder such as refractive index, imperfect shapes, and surface roughness. Another important point is that in this work, we have studied the effects of disorder on the transmission properties of photonic crystal logic gates which are mainly determined by the two-dimensional propagation of the beam through the photonic crystal.

For the systems studied here, two-dimensional models are good enough to describe the physics of realistic three-dimensional photonic crystal slabs [22]. However, to describe figures of merit that are fundamentally three dimensional, like the out-of-plane losses or mode volumes as it is extensively discussed in [23], our two-dimensional model will be certainly inaccurate.

6. Conclusion

In this paper, we have studied the effect of structural disorder on photonic crystals logic gates using a new approach based on the evaluation of two metrics: the error rate (ER) and the mean absolute deviation of transmission of the error cases (MATEC). We applied this process to evaluate some photonic crystal logic devices with different array lattice configurations. ER is the probability that a fabricated photonic crystal logic gate does not accomplish its logic function correctly, and MATEC measures the imperfection degree of the device through the transmission spectrum.

The results obtained in this work show that for structures with triangular lattices, regions in the corner and close to the output are more critical to ER and MATEC metrics, respectively. For structures with a square lattice, we found that the intersection region is the most sensitive to both parameters.

We have also found that the evaluation of ER and MATEC for photonic crystal logic gates can establish new standards and paradigms for the design and manufacture of future robust gates.

Finally, we highlight that the methodology described here can be easily applied to evaluate other kinds of disorder and to analyze devices based on photonic crystal waveguides with any lattice configuration. As a future work, we plan to project possible solutions to avoid/minimize the effect of disorder unintentionally introduced in the fabrication process of photonic crystal logic gates.

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