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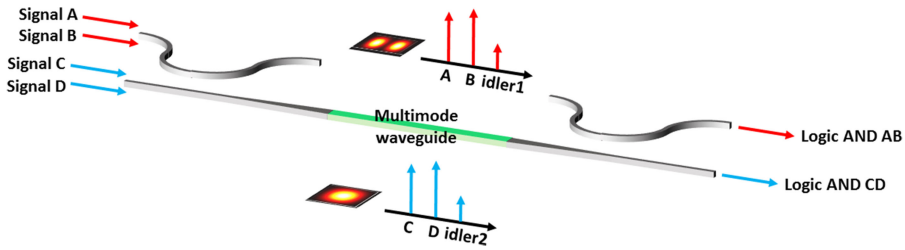

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Dual-Channel AND Logic Gate Based on Four-Wave Mixing in a Multimode Silicon Waveguide

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Abstract: We experimentally demonstrate on-chip dual-channel all-optical AND logic operations based on four-wave mixing (FWM) for on-off keying (OOK) signals in a multimode silicon waveguide. A two-mode (de)multiplexing circuit consisting of tapered directional coupler-based (de)multiplexers and a multimode waveguide is designed and fabricated for this application. Experimental results show open eye-diagrams and confirm the logic operations with moderate power penalties for both modes.

Index Terms: Optical logic devices, four-wave mixing, mode-division multiplexing, silicon nanophotonics.

1. Introduction

As the demand for high-capacity network is becoming increasingly critical, optical interconnects and communications have been regarded as a potential solution to help break the bottleneck of electronics thanks to its lower power consumption and larger bandwidth [1]. As a subsequent procedure of optical communication, all-optical signal processing, which can potentially operate at the line rate of optical transmission [2], provides us with an alternative way to process data efficiently without risking degrading the overall performance of the computing system in the case of using optic-to-electric (O/E) conversions. As key elements for all-optical signal processing, logic operations such as NOT, AND, OR, and XOR, have been investigated for a variety of modulation formats and realized with different nonlinear processes in various media, including highly nonlinear fibers [3], semiconductor optical amplifiers [4], chalcogenide waveguides [5], periodically poled lithium niobate devices [6] and silicon waveguides [7]–[9]. Half adders and half subtracters as well as optical computing have also been reported as advanced logic operations recently [10]–[14]. Among these nonlinear devices, silicon waveguide is considered to have advantages over the others for its compatibility with CMOS technique, high nonlinear coefficient and a variety of nonlinear

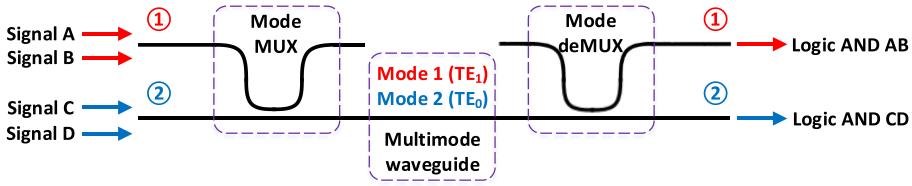

Fig. 1. Schematic diagram of on-chip dual-channel all-optical AND logic operations.

effects such as FWM and cross-phase modulation, etc. Since the capacity of all-optical signal processing is expected to be improved according to the increasing capacity of optical interconnects and communications, logic devices which support large-capacity operations based on the silicon-on-insulator (SOI) platform are becoming highly demanded [15].

On the other hand, mode-division multiplexing (MDM) has been widely explored as a new dimension to increase the transmission capacity of single fibers and waveguides [16], [17]. It is noted that logic operations in previous work are usually realized under single mode condition, therefore multiple single mode waveguides are needed for parallel logic operations with multiple pairs of inputs, which will result in a large footprint (considering the footprint of the single mode waveguides themselves and the guard spaces between them). However, using multimode device can deal with this problem with only one waveguide that takes smaller space than single mode case, thus making a relatively compact structure. Recently, mode-selective wavelength conversion based on FWM in a multimode silicon waveguide has been demonstrated, which offers a way of exploiting the wavelength dimension in MDM systems [18], [19]. MDM wavelength conversion with mode selectivity based on dual-mode fiber has also been proposed in simulation [20]. AND logic operation using OOK signals based on FWM generates idlers carrying the AND logic product via wavelength conversion. Considering the similarity between wavelength conversion and FWM-based logic operations, combining logic operations with MDM technique is therefore a potential method to perform parallel logic operations with multiple pairs of inputs in order to expand the logic operation capability of a single nonlinear device as well as reduce the footprint. Specifically, it is done by efficient intra-modal FWM along with low crosstalk from inter-modal FWM enabled by dispersion engineering. Nevertheless, such functionality has never been demonstrated so far.

In this paper, we design and fabricate a multimode silicon waveguide to realize dual-channel all-optical AND logic operations based on FWM. A mode multiplexer based on tapered directional coupler is utilized to couple two input channels to the TE_0 and TE_1 modes of the multimode waveguide. After FWM in the multimode waveguide, idlers carrying the AND logic result of each channel are output to different ports according to their spatial modes. Theoretical analysis of the waveguide design is presented. As a proof of concept, two 5 Gb/s OOK signals are used in the experiment, resulting in an aggregate bit rate of 10 Gb/s. Correct temporal waveform sequences and eye diagrams are presented to confirm the validity of our design. Bit error rate (BER) measurements show power penalties of 0.9 dB and 1.5 dB for single-channel operation, along with additional 1.3 dB and 1.1 dB in the case of dual-channel operations evaluated at 7% forward error correction (FEC) threshold.

2. Operation Principle, Chip Design and Device Characterization

The schematic diagram of on-chip dual-channel all-optical AND logic operations is shown in Fig. 1. Two channels are multiplexed to a multimode silicon waveguide on mode 1 (in the following corresponding to the TE_1 mode) and mode 2 (corresponding to the TE_0 mode), respectively, and each channel carries two OOK signals with different wavelengths. Strong FWM is obtained in the multimode waveguide when the pump and signal lights are on the same mode while weak FWM is obtained when they are on different modes due to phase mismatch [18]. Logic operation using OOK signals based on FWM in the single mode case can generate idlers carrying the AND logic product of the pump and signal lights. Thus, if signals A and B are input to CH1, they will be

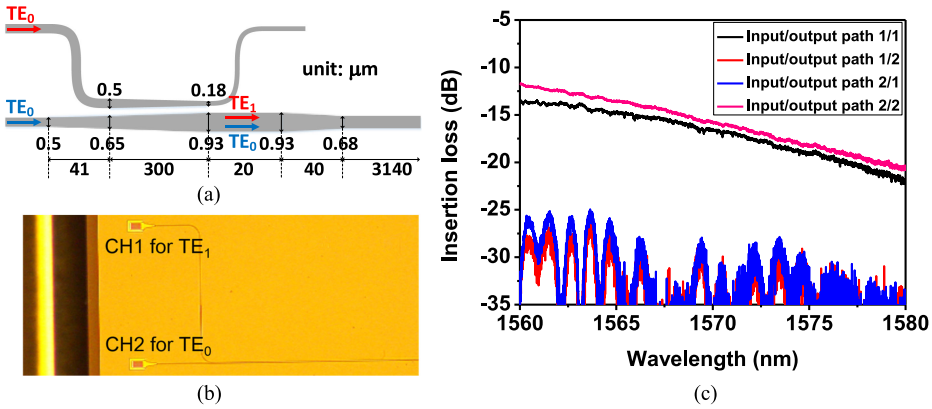

Fig. 2. (a) Structure of the mode multiplexer based on tapered directional coupler. (b) Microscope image of the fabricated mode multiplexer. (c) Measured transmission and mode crosstalk of the two channels (CH1 and CH2) of the two-mode (de)multiplexing circuit.

coupled to mode 1 in the multimode waveguide thanks to the mode multiplexer. Two idlers will then be generated on mode 1 after FWM, which carry the AND logic product of signals A and B. Similarly, if signals C and D are launched in the multimode waveguide on mode 2, they will generate idlers on mode 2 carrying the AND logic product of signals C and D. The generated idlers will then be demultiplexed to different output ports depending on their spatial modes and the AND logic products of the two groups of signal can be obtained individually after band pass filtering. A single nonlinear device can thus be used to simultaneously realize two AND logic operations.

The mode-selective FWM process is determined by the phase matching condition between the interacting waves, which depends on the dispersion properties of the multimode waveguide [21], and changing the waveguide geometry can greatly affect its dispersion properties. The second-order dispersion β_2 for both TE_0 and TE_1 modes of a strip SOI waveguide (with upper SiO_2 cladding layer) of $H = 220$ nm with different widths are firstly calculated by a vectorial finite difference mode solver [22]. In order to achieve a high FWM conversion efficiency within both TE_0 and TE_1 modes, the waveguide width is chosen to be around 700 nm so that β_2 for both modes have similar and close to zero dispersion values over C-band. Simulation results and detailed analysis of the dispersion engineering of the multimode waveguide can be found in our prior work [19]. A two-mode (de)multiplexing circuit consisting of tapered directional coupler based (de)multiplexers and a multimode waveguide is then designed for the experiment.

The fabricated multimode waveguide, which is the key part of the on-chip circuit, is 3.14 mm long with a height of 220 nm and width of 680 nm. The mode (de)multiplexer is based on tapered directional couplers due to their simple structure and large fabrication tolerance [23], which is illustrated in Fig. 2(a). Vertical grating couplers are used to couple light to and from the chip. The waveguides are fabricated on a SOI wafer (top silicon layer: 220 nm, buried oxide layer: 2 μm) with upper cladding layer of SiO_2. The microscope image of the fabricated mode multiplexer section is shown in Fig. 2(b). According to experimental verification, the maximum FWM conversion efficiency is achieved at 1570 nm, which is chosen as the pump wavelength later. Fig. 2(c) shows the measured transmission and crosstalk of the two channels (CH1 and CH2) of the two-mode (de)multiplexing circuit, presenting total insertion losses of 17 dB and 16 dB between input/output 1/1 and 2/2, respectively, along with mode crosstalk of -17 dB and -18 dB at 1570 nm with input optical power of 7 dBm.

3. Experimental Setup and Results

The experimental setup for the proof-of-concept work demonstrating two parallel 5 Gb/s AND logic operations, resulting in a total aggregate logic capacity of 10 Gb/s, is illustrated in Fig. 3. Two

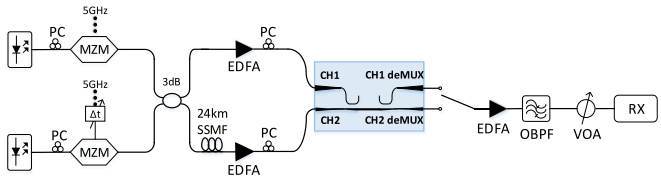

Fig. 3. Experimental setup for the dual-channel AND logic operations.

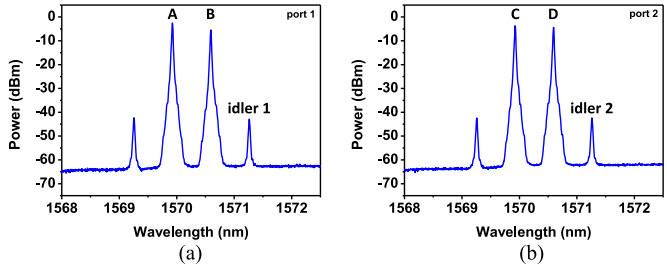

Fig. 4. Spectra measured at output (a) port 1 and (b) port 2 under simultaneous AND logic operation.

channels of continuous waves light are generated from two external cavity laser sources centered at $\lambda_1 = 1570$ nm and $\lambda_2 = 1570.7$ nm. The commercial software MATLAB is used to generate two independent pseudo-random binary sequences (PRBSs) of length 2^9-1 (for the convenience of verifying the logic operation) which are loaded into the arbitrary waveform generator and converted into corresponding electrical signals. Then the lights are modulated at a rate of 5 Gb/s by two Mach-Zehnder electro-optic modulators (MZMs) with the signals respectively, to obtain the logic signals A and B. The two signals are combined by a 3 dB coupler and then split into two tributaries which are then amplified by erbium doped fiber amplifiers (EDFAs). Each tributary has two signals as the inputs of the AND logic operation. The logic signals C and D are obtained from the signals A and B after decorrelation in a length of 24 km standard single mode fiber (SSMF), and they can be regarded as two independent signals from signals A and B due to the properties of PRBSs. Bit alignment of the two signals in each tributary is realized by adding delays to one of the electrical signals when light is modulated. The polarization states of the lights are adjusted by polarization controllers (PCs) to match the TE polarization of the device. The total power of the two signals input to each port of the mode multiplexer is about 25 dBm, and the powers of each signal are identical. After FWM in the multimode waveguide, the generated idlers are demultiplexed to the corresponding output ports, amplified by an EDFA, filtered out by an optical band pass filter (OBPF) with bandwidth of 0.5 nm, and finally collected by a receiver. After O/E conversion, the temporal electric signal is recorded by a high-speed digital oscilloscope (Tektronix, 33 GHz ADC bandwidth) and processed off-line. BERs of the logic signals are also measured off-line. Every BER point is evaluated over 2 million bits.

Fig. 4(a) and (b) show the spectra of the two signals (separated by 0.7 nm) as well as that of the two idlers (centered at 1571.4 nm and 1569.3 nm) measured at output port 1 and 2, for TE_1 and TE_0 mode, respectively, when the AND logic operation is realized in parallel. As can be seen from the power difference between signal and idler, the measured FWM conversion efficiency is about -40 dB for both modes. The temporal waveforms and eye diagrams of the two input signals and the generated idler for CH1 and CH2 are presented in Fig. 5(a) and 5(b), respectively. Here we consider only the idler at 1571.4 nm for both modes as an example. By comparing the 20-bit-long temporal waveform sequences of the two signals and the idler in each tributary, the dual-channel AND logic operations of our design is confirmed according to the output data streams.

Fig. 6 shows the results of BER off-line measurements for the two idlers obtained at output port 1 (corresponding to idler on the TE_1 mode) and port 2 (corresponding to idler on the TE_0 mode), respectively, when signals propagate in parallel (i.e., dual-channel AND logic operations

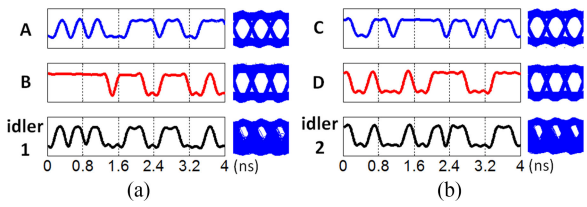

Fig. 5. Temporal waveforms and eye diagrams of (a) signal A, signal B and idler 1, (b) signal C, signal D and idler 2.

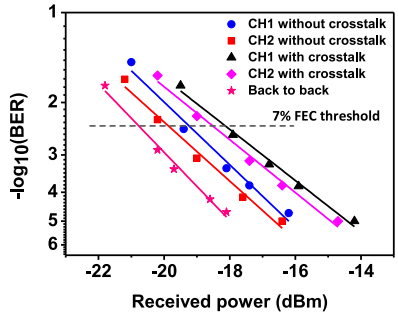

Fig. 6. BER measurements for the TE_1 and TE_0 idlers, with and without mode crosstalk, respectively.

with mode crosstalk) as well as when the signals propagate in each channel individually (i.e., single-channel AND logic operation without mode crosstalk). Power penalties compared to the back-to-back case in the absence of mode crosstalk are 0.9 dB and 1.5 dB at 7% FEC threshold for TE_0 and TE_1 modes, respectively, while additional 1.3 dB and 1.1 dB penalties are measured with crosstalk. BER below FEC limit is achieved and error free operation can be realized by using FEC decoding. Crosstalk may originate from the leakage of light in the mode (de)multiplexer, as well as inter-channel nonlinear absorptions caused by two-photon absorption and free-carrier absorption.

As can be seen from the eye diagrams of the two idlers for the present proof-of-concept work, the system performance is mainly limited by the optical signal-to-noise ratio of the idlers or low FWM conversion efficiency. However, higher operation speed can be realized by further optimization. The FWM conversion efficiency can be improved by reducing the insertion loss of the chip, which is mainly due to the mismatch between the measured central wavelength of the passband of the vertical grating coupler and the waveguide zero dispersion wavelength. Higher FWM conversion efficiency can also be achieved by using higher power pump or a longer multimode waveguide, and by optimizing the dispersion properties of the waveguides [24]. Besides, the 3 dB FWM conversion bandwidth is 1.2 nm for both modes, thus further optimization needs to be done by taking into account the dispersion property of the mode (de)multiplexer, which may also have an impact on the FWM conversion efficiency. The logic operation scale could possibly be extended to more channels provided that more modes are included and optimum phase matching conditions can be found, therefore potential applications in large-capacity logic devices for basic logic functions such as AND and XOR are to be expected. Apart from this, advanced logic functions such as half adders, half subtracters and digital comparators etc. can also be expected based on this work for further investigations.

4. Conclusion

We have reported the first experimental demonstration of dual-channel AND logic operations of NRZ-OOK PRBS data streams at 2×5 Gb/s based on a single multimode silicon waveguide. A two-mode (de)multiplexing circuit has been designed and fabricated for this application. Spectra, correct temporal waveforms, as well as the eye diagrams of the signals and the idler of individual

channel when the AND logic operation is realized in parallel have verified the validity of our design. We also made BER measurements indicating that power penalties are 0.9 dB and 1.5 dB for the conversion of each mode taken individually along with additional 1.3 dB and 1.1 dB in the case of parallel AND logic operations at 7% FEC threshold. As a proof of concept, the logic operation speed is limited indeed, however it can be improved by optimizing the dispersion characteristics of waveguides and raising the length of multimode waveguide. Further extension in terms of the number of channels can be expected by engineering the dispersion characteristics of more higher-order modes, and advanced logic functions can be achieved by parallel operations of different logic gates.

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