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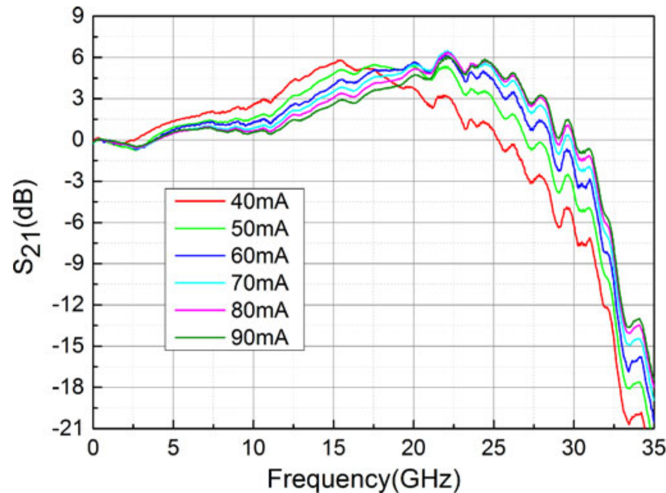

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Abstract: In this paper, a simple and cost-effective packaging scheme for improving the modulation bandwidth of directly modulated laser is presented and demonstrated. Combined with the equivalent circuit, the effect of disequilibrium on signal injection efficiency is comprehensively and systematically studied. The simulation and measurement results have a good agreement, which show that the high frequency performance of module can be effectively improved with the proposed packaging scheme. Finally, employing the proposed packaging scheme, we achieve the 3-dB bandwidth of up to 32 GHz regarding the directly modulated semiconductor laser module with the butterfly package.

Index Terms: Semiconductor laser, directly modulation, package design, disequilibrium

1. Introduction

The rapid increase of data traffic puts enormous pressure on communication capacity. One of the effective solutions for increasing communication capacity is to improve the modulation bandwidth of the optical source [1]–[4]. Although some techniques, such as the advanced modulation format technique [5] and the equalization technique [6], can overcome the bandwidth limitation of optical source, high computational complexity and large electronics power consumption is required. Therefore, it is still the most practical approach to employ a broadband optical source. Electro-absorption modulators integrated with a distributed feedback laser (EML) and directly modulated laser (DML) are promising candidates and have been developed over many years for optical fiber communication [7], [8]. Although an EML has a large extinction ratio, which plays a critical role in long-range communication (e.g., 40 km), high power consumption is an inevitable problem because of the additional operation of the electro-absorption modulator (EAM). Furthermore, as many factors resulting from the integration of distributed feedback (DFB) laser and EAM need to be considered [9], such as electrical isolation, optical isolation, and high speed, the fabrication of EML chips becomes rather complicated, especially when the operation speed exceeds 25 Gb/s. Therefore, the cost will increase. Unlike the EML, the DML does not have the problems mentioned above. The mature manufacture process and simple structure enable an excellent performance to be achieved, such as high linearity, high output power, small size, low power consumption, and high-yield production. Thus, the DML is considered the best solution for short-range communication. According to [10],

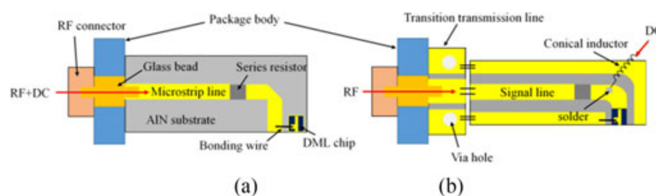

Fig. 1. Schematic of conventional packaging schemes. (a) Transmission pathway of the RF signal and DC is the same. (b) Isolation of RF signal from DC.

the modulation performance of a semiconductor laser is very important in optical communication systems. However, the modulation bandwidth of the DML is inferior compared with that of the EML [11]. The modulation bandwidth can be improved by increasing the intrinsic bandwidth of the DML chip with a proper design, which plays a dominant role in the improvement of the modulation bandwidth of the DML. However, regarding the DML module, the packaging process of the DML chip is also important. Improper packaging processes will lead to the loss of high frequency signals during transmission and thus, deteriorate the final performance of the module. Therefore, a suitable high frequency package design of the DML module should be considered.

To get a stable lasing of light, the drive current (DC) of the DML module should be setted above threshold. Then, the modulated RF signal from the signal source is fed into the laser chip. Usually, there are two schemes to realize the injection of the RF signal and DC. Fig. 1(a) and (b) show the different schemes reported earlier. In Fig. 1(a), the RF signal and DC share the same transmission pathway [12]. The RF signal from the signal source is fed from the RF connector to the laser chip jointly with the DC through the RF microstrip line and series resistor. Such a structure makes the packaging process simpler and there is no need to design an independent DC bias circuit. However, it can suffer from the complexity of heat dissipation. Because the intrinsic resistance of the DML chip is about 10 Ω, a 40 Ω thin-film resistor is usually fabricated in series with the chip in order to match with the 50 Ω measurement system,. Hence, the DC has to flow past the series resistor and the heat that will be generated will increase the power consumption of the thermoelectric cooler (TEC) in order to stabilize the temperature of the chip. Furthermore, it is inconvenient to adjust the RF signal and the DC separately. Therefore, a bias tee is generally used before the RF connector. There is no doubt that an interference factor will be introduced as the RF signal passes through the bias tee, which in turn affects the high frequency performance of the module.

Fig. 1(b) shows another reported scheme in which the RF signal and the DC have been injected into the chip via different pathways, which can be used to solve this problem mentioned above [13]. In addition, the grounded coplanar waveguide (GCPW) transmission line is used instead of the microstrip line in Fig. 1(a) due to its many advantages compared with the microstrip line, such as a wide frequency range, low loss, high operating frequency, and excellent shield noise capability. The transition transmission line is used for connecting the glass bead and the GCPW transmission line. Two vertical interconnect access (VIA) holes are used to achieve better grounding. In this scheme, an independent DC bias circuit is designed between the series resistor and chip. Hence, this will prevent the current from passing through the series resistor and, thus, will help to prevent the production of heat and ultimately decrease the power consumption. The high frequency inductor in the DC bias circuit plays an essential role: it used for transferring the DC into the chip and preventing RF signal leakage simultaneously. The high frequency inductor lead is usually attached to the RF signal line by welding or soldering. Therefore, the disequilibrium of the high frequency signal flow between the conical inductor lead and transmission line will inevitably occur, which can decrease the signal injection efficiency, deteriorate the quality of modulated signal, and decrease the modulation bandwidth of the DML. Furthermore, due to the limitation of the soldering process, the area between the series resistor and chip must be enough large for soldering. This will lead to impedance discontinuity between the series resistor (40 Ω) and the chip (∼10 Ω). Hence, the reflection performance of the module will also deteriorate [14].

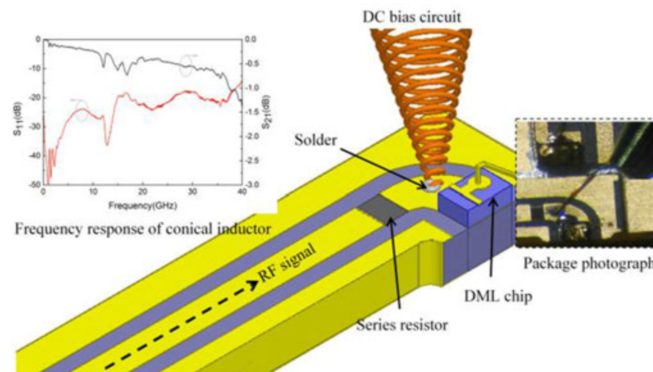

Fig. 2. Conventional packaging scheme of DML chip. The insets are the partial photography (right) and the frequency response of conical inductor measured in shunt on a 50 Ω trace (left).

Faced with these problems, we propose a new packaging scheme in which the DC bias circuit is placed behind the chip with regard to the direction of RF signal injection. Therefore, the disequilibrium of the high frequency signal flow is weakened, which helps to enhance the signal injection efficiency. In addition, the shape of the series resistor has been changed to an irregular one for fitting the turn of the pathway and its position is closer to the chip. These improvements will help to optimize the frequency response of the DML module.

In the paper, we firstly investigate the influence of the disequilibrium on the modulation bandwidth of the DML module theoretically by using the equivalent circuit model. Then, we propose a simple and cost-effective packaging scheme for improving the modulation bandwidth. Moreover, to evaluate the effectiveness of the proposed method, we pack a DML chip in a butterfly body with a coaxial connector and investigate the effect of disequilibrium. Finally, using the proposed packaging scheme and chip designed by us, an ultra-wideband DML module is presented and tested.

2. Circuit Model and Simulation Results

Fig. 2 shows the scheme of the RF signal pathway and DC pathway. The bias inductor is placed between the series resistor and DML chip. In order to prevent leakage of the signal and the interference of external factors through the DC pathway, the bias inductor should have both a high cut-off frequency and high inductance value. Thus, the conical inductor with an inductance of 0.84 μH (made in Piconic, Inc.) is the best candidate for this owing to the many advantages mentioned above. The inset (left) shows the frequency response of the conical inductor measured in shunt using a 50 Ω trace. It can be seen that the useable bandwidth can reach 17 GHz and 40 GHz with an insertion loss of 0.75 dB and 1.5 dB, respectively. Meanwhile, the reflection has been suppressed below -18 dB at 17 GHz and below -14 dB at 40 GHz. Therefore, the conical inductor exhibits a good performance and meets the packaging requirement. However, the operation of the conical inductor at a high frequency requires carefully assembly. In order to prevent any packaging-related parasitic parameters, the conical inductor lead length should be as short as possible and the disequilibrium between the lead and the RF transmission line should also be taken into consideration. The lead is attached to the transmission line by welding or soldering. Therefore, due to the introduction of soldering, it is inevitable to produce the contact capacitance which will lead to the disequilibrium of the high frequency signal flow, as shown in Fig. 2 (right inset). The signal injection efficiency is also decreased. We can see that the solder accumulates between the lead and RF feeding line. In this section, we will study how the disequilibrium affects the performance of the DML module by using the equivalent circuit model and simulation.

Fig. 3 shows the simplified equivalent circuit model of the DML module based on the conventional packaging scheme as shown in Fig. 1(b) in the Advanced Design System (ADS). The area designated by the gray dot line illustrates the intrinsic DML chip circuit model. R_1 is the series resistor

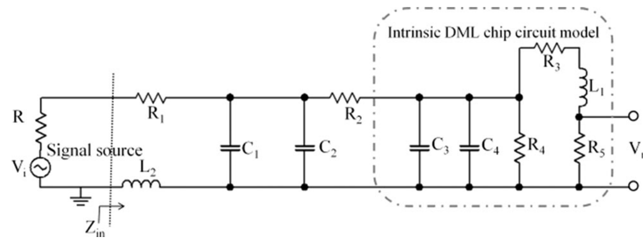

Fig. 3. Conventional equivalent circuit model of packaged DML module with signal source.

TABLE 1
Device Parameters

Parameter	Value	Description
R	50 Ω	Source impedance
R_1	40 Ω	Series resistance
L_2	0.2 nH	Inductance of bonding wire
C_1	0.3 pF	Contact capacitance between lead and transmission line
C_2	0.93 pF	Parasitic capacitance between chip and submount
R_2	7 Ω	Parasitic resistance between chip and submount
C_3	15.02 pF	Capacitance associated with the confined carriers
C_4	4.6 pF	Capacitance associated with the unconfined carriers
R_4	5.08 Ω	R4, R3 and R5 are related to DC components in the rate equation
R_3	0.18 Ω	
R_5	0.2 Ω	
L_1	4.55 nH	Inductance from photon storage

used for matching with the laser chip. R_2 and C_2 are modeled as the parasitic response of the laser chip. C_1 is the contact capacitance between lead and transmission line. If the soldering process is correctly done, C_1 should be very small. L_2 represents the inductance value of the bonding wire that has been used for connecting the chip pad and the RF feeding line. The modulated signal applied to the laser chip is represented by a voltage source with a 50 Ω impedance. From the circuit model, the relation between the source voltage V_i and the voltage V_m applied to the active region of chip can be expressed as

$$\frac{V_m}{V_i} = \frac{r}{(r+R_2)+(R_1+R+j\omega L_2)\left[1+j\omega\left(C_1+C_2\right)(r+R_2)\right]} \times \frac{R_5}{R_5+R_3+j\omega L_1} \tag{1}$$

Where

$$r = \frac{1}{1/(R_5+R_3+j\omega L_1)+1/R_r} \tag{2}$$

$$R_r = \frac{1}{j\omega\left(C_3+C_4\right)+1/R_4} \tag{3}$$

To evaluate the influence on the frequency response of the DML module when changing the value of C_1, the transmission response $G(f)$ and the reflection response $R(f)$ have been analyzed by using the device parameters listed in Table 1. The $G(f)$ and $R(f)$ are determined by the

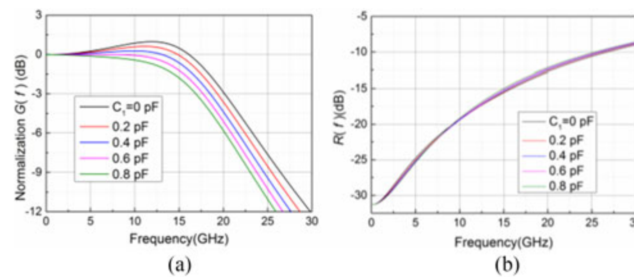

Fig. 4. Calculated (a) transmission response $G(f)$ and (b) reflection response $R(f)$ of DML module with different values of C_1.

follow equations.

$$G(f) = 20\log_{10}[V_m(f)/V_m(0)] \quad (4)$$

$$R(f) = 20\log_{10}[(Z_{in} - R)/(Z_{in} + R)] \quad (5)$$

Fig. 4(a) and (b) show the calculated results of $G(f)$ and $R(f)$ with different values of C_1, respectively. It can be seen that with increasing C_1, the 3-dB bandwidth is degraded. If the contact between the conical inductor lead and RF feeding line is ideal and perfect ($C_1 = 0$ pF), the bandwidth will be increased by 3 GHz compared with that when C_1 is 0.8 pF. Meanwhile, there is no distinct difference in the influence of the contact capacitance on the reflection response for various values of C_1, as shown in Fig. 4(b). Thus, we should reduce the contact capacitance as much as possible to improve the transmission bandwidth of the module. However, it is impossible to obtain an ideal contact when the conical inductor lead is fixed on the transmission line by soldering owing to the improper manual process or poor mechanical tolerance. Therefore, we have to develop a new packaging scheme to solve the problem and obtain a desirable performance.

In the new packaging scheme, the conical inductor has been soldered behind the chip with respect to the direction of RF signal flow. Therefore, the series resistor can be placed as close as possible to the chip. Fig. 5(a) shows the improved equivalent circuit model of the DML module. Compared with the equivalent circuit using the conventional packaging technique, the contact capacitance C_1 between lead and transmission line disappears, which means that the disequilibrium is weakened and even eliminated. Owing to the adjustment of the conical inductor lead location, C_1 is also shifted, as shown in Fig. 5(a). In fact, according to the optimized equivalent circuit model, we can roughly conclude that the value of C_1 has very little influence on the high-frequency performance of the DML module. This is because the RF signal flow is first passed the chip and then utilized to modulate the intensity of output light. There are only few leaked signal is flowed through the contact capacitance and so the effect of the contact capacitance on the transmission response is very little. In other words, the signal injection efficiency has been improved. This conclusion has been confirmed by calculations, as shown in Fig. 5(b). It can be seen that although the values of C_1 are different, the reflection response does not change and meanwhile, the variation in the transmission response can hardly be distinguished. That means we do not need to control the value of the contact capacitance precisely when the conical inductor lead is soldered on the transmission line pad. That helps to increase the redundancy of the soldering process and decrease the complexity of the packaging technique.

3. Experimental Results

Fig. 6 shows a photograph of the DML module packaged in a butterfly body with 7 pins and a coaxial connector based on the proposed packaging scheme. The operating temperature, 25 °C, of the DML module is controlled by the TEC. The lens-coupled output power is 9 mW at 80 mA. In order to achieve the condition when the contact capacitance is 0 pF, we have injected the DC

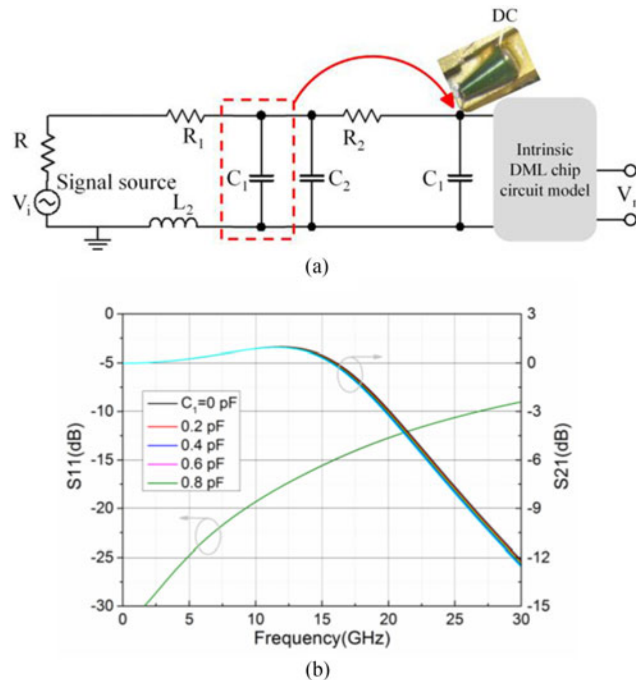

Fig. 5. Proposed equivalent circuit model of DML module (a) and the calculated frequency response with different values of C_1 using the new packaging scheme (b). The red arrow represents the adjustment of the contact capacitance.

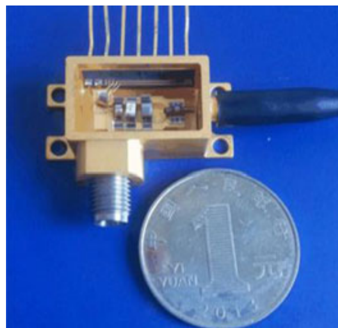

Fig. 6. Photograph of DML module with a butterfly package.

through the coaxial connector. By fitting the equivalent circuit with the measured S-parameters, the values of C_1 can be determined. Fig. 7(a) and (b) show the measured transmission response S21 and the reflection response S11 with different packaging schemes by using a vector network analyzer (VNA). The results clearly show that the 3-dB bandwidth of the DML module deceases as C_1 increases. It can be seen that with the conventional packaging scheme, the 3-dB bandwidth can be up to ~26 GHz when the value of C_1 is 0 pF. If the soldering process is not abnormal, the 3-dB bandwidth will be decreased by 2.5 GHz at 0.47 pF compared with that when C_1 is 0 pF. In addition, Fig. 7(b) shows that there is no obvious difference in the reflection responses in spite of the various contact capacitance values. That means the conventional packaging scheme has a greater impact on the transmission performance than on the reflection performance. The measurement results show a good agreement with the simulation results. With the new packaging scheme that we designed, the 3-dB bandwidth is improved and has reached up to ~25.5 GHz, as shown in Fig. 7(a). The lower reflection response is obtained in a range of less than ~9 GHz. It is worth

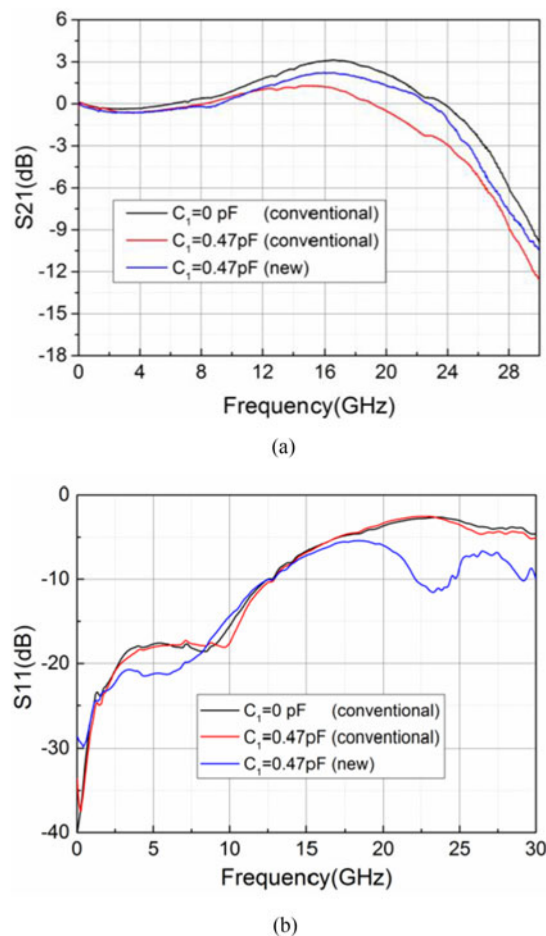

Fig. 7. Measured transmission response (a) and reflection response (b) of the DML module at a laser current of 80 mA in different packaging conditions.

noting that the new package scheme has reduced the soldering process requirement and simplified the package technique, especially for high-frequency optoelectronic devices.

4. 32-GHz DML Module

Using the proposed packaging scheme, we packed a DML module, as shown in Fig. 6. The chip is fabricated using nanoimprint lithography technology and operated at a 1.3 μm wavelength. The length of the chip is 200 μm and the diameter of the electrode pad is 60 μm. To verify the effect of the proposed packaging scheme, we firstly calculated the intrinsic response of the DML chip using the method described in [15], as shown in Fig. 8(a). Fig. 8(b) shows the measured 3-dB bandwidth of DML module based on the proposed packaging scheme. It can be seen that with increasing DC, the 3-dB bandwidth increases and saturates gradually and has a good agreement with the intrinsic bandwidth. However, due to the bandwidth limitation of photodiode the transmission response has a quick drop around 30 GHz. Nevertheless, the 3-dB bandwidth of the module can be still up to 32 GHz when the injection current is 90 mA, which is improved compared to that in [16]. We expect that this module can have a potential application in high-speed optical communication, such as 43 Gb/s, 56 Gb/s, or even 100 Gb/s. The comparison of the intrinsic response and the module response can provide a guide for the packaging design of the ultra-wideband DML module.

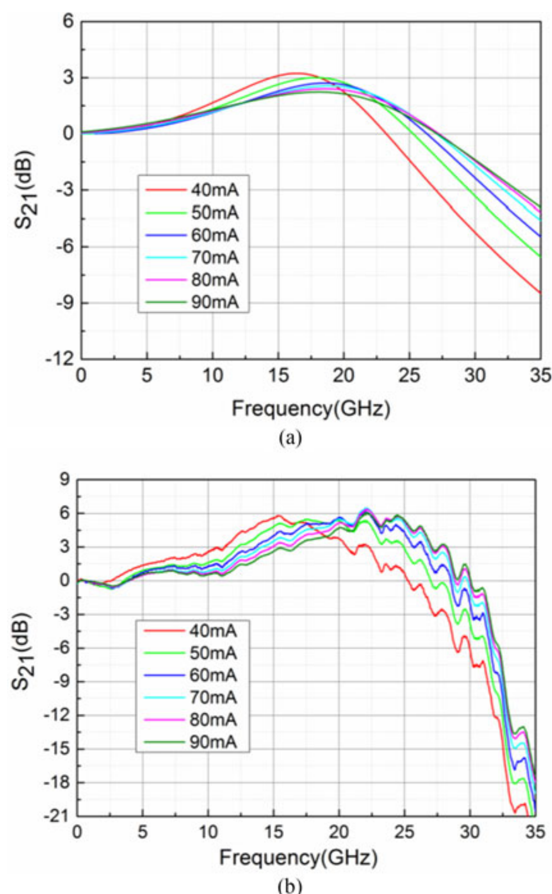

Fig. 8. Calculated intrinsic response (a) of DML chip based on the method in [15]. Measured 3-dB bandwidth of DML module (b) based on the proposed packaging scheme.

5. Conclusion

A novel packaging scheme of a DML chip is proposed in this paper. The detailed analysis and simulation using the equivalent circuit model indicate that the disequilibrium due to the abnormal soldering process has a significant effect on the frequency response of the DML module. When the disequilibrium is enhanced, the transmission bandwidth is degraded and the reflection response is almost kept constant. However, with the proposed packaging scheme, the disequilibrium is greatly weakened, as demonstrated by the simulation results. That means our scheme has a lower requirement for soldering process quality and mechanical equipment precision. Moreover, in the design of the RF signal transmission circuit, any process that may introduce disequilibrium should be seriously considered. To verify our analysis, we packed a DML chip in a butterfly body and measured its frequency response. The measurement results show the same tendency as the simulation results. By using the proposed packaging scheme, the 3-dB bandwidth of the DML module can be improved. Furthermore, we achieve a 3-dB bandwidth of 32 GHz. Based on these results, we hope that the proposed packaging scheme can provide a useful solution for packaging high-frequency DML chips.

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