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Lei Chen
Han Ye
Yumin Liu
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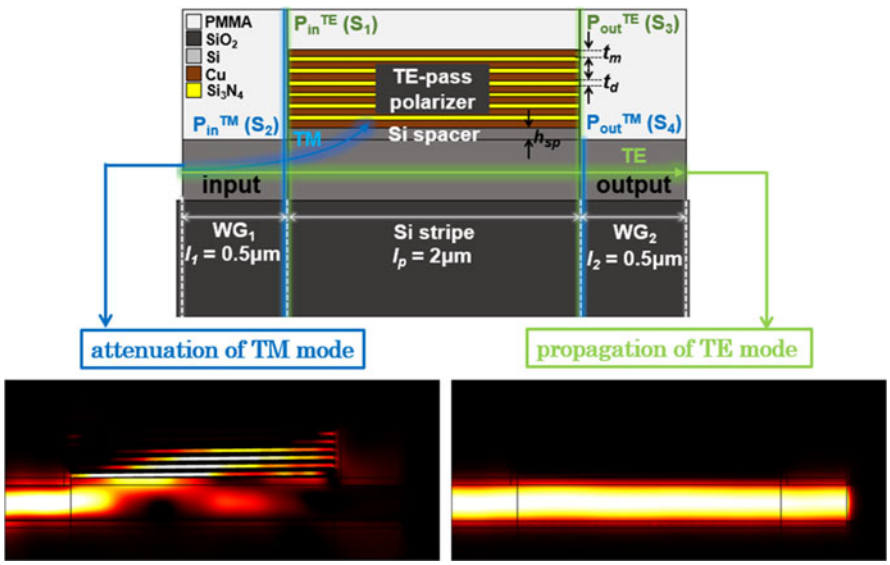

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Lei Chen, Han Ye, Yumin Liu, Dong Wu, Rui Ma, and Zhongyuan Yu

State Key Laboratory of Information Photonics and Optical Communications, Beijing University of Posts and Telecommunications, Beijing 100876, China

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Abstract: We propose and investigate a silicon photonic TE-pass polarizer consisting of alternating layers made out of copper/silicon nitride (Cu/Si_3N_4). Based on a Si stripe waveguide, the launched dominant fundamental TE mode can normally pass through it with little influence, whereas the unwanted fundamental TM mode ends up in nearly zero output as it is gradually coupled into a plasmonic mode. Particularly, the polarizer with wedge-shaped Cu/Si_3N_4 structure can achieve extremely high extinction ratio (ER) of 52.34 dB and low insertion loss of 0.35 dB within an ultracompact device length of 2 μm. It also presents a relatively wide operating bandwidth of 61 nm maintaining ER $>$20 dB. Furthermore, considering Si_3N_4 itself a good Cu^{2+} ion diffusion barrier and its good adhesion to copper, the device fabrication is reasonably practicable using complementary metal–oxide semiconductor (CMOS)-compatible technologies. Last but not the least, we first present and analyze the connection between mode property and device performance, which could provide a significant step forward for establishing and improving the polarization diversity systems of great importance in nanophotonic integrated circuits.

Index Terms: Plasmonics, subwavelength structures, silicon nanophotonics, waveguide devices.

1. Introduction

Silicon photonics, integrated optics, and nanophotonics are cutting-edge research fields in close connection, giving rise to tremendous potentialities for realizing photonic integrated circuits with high compactness and performance [1]. Plasmonics, which is a cross-disciplinary branch of nanophotonics, is considered as an excellent candidate for further down scaling device footprint. Surface plasmon polaritons (SPP) wave, in the form of collective oscillations of electrons in a metal, can propagate along a metal-insulator surface with subwavelength mode size [2]. Based on the silicon-on-insulator (SOI) platform, a variety of active/passive nanophotonic systems containing SPP-dominate components can be constructed using mature complementary metal-oxide-semiconductor (CMOS) technologies [3]. Large birefringence of the SOI platform provides itself with great advantages in implementing polarization diversity schemes that are classified into polarization division multiplexing

(PDM) and polarization transparent transmission. For the former one, waveguide-based polarization beam splitters [4]–[11] are the most studied PDM devices. Such kind of devices support both TE and TM modes that propagate in two SOI channels separated from one source. The later one, the focus of our work, can be realized using polarization state polarizers [12]–[20] or rotators [22], [23]. A number of common polarizers are probably based on shallowly etched Si stripe waveguides, horizontally/vertically slotted Si waveguides, hybrid plasmonic waveguides, and so on. In general, the polarizers are based on the principle that dominant polarization mode can pass through with little influence whereas the unwanted one cannot. The following are some reported work. As described in [12], a section of Ag/SiO_2/Si hybrid waveguide is inserted directly into a Si stripe to trap TM mode, giving rise to an extinction ratio (ER) of 18.6 dB and an insertion loss (IL) of 3.2 dB/21.8 dB for TE/TM mode within a device length of 13 μm. In [13], similarly, a section of Cr/Si_3N_4/Si hybrid waveguide is inserted into a Si stripe in order to improve ER, however, metal of Cr instead of Ag causes large IL to TE mode. In [14], Xu *et al.* propose a TE-pass polarizer consisting of a slot waveguide coated by a Si stripe and two Ag stripes, presenting an ER of 19.61 dB and an IL of 0.39 dB for TE mode within a device length of 3.2 μm. In [15], although the reported TE-pass polarizer has a device length of merely 0.8 μm, it achieves poor ER of 19 dB and IL of 1 dB. Very recently, both Xu *et al.* [16] and Huang [17] introduce a thin indium tin oxide (ITO) layer into the slot waveguide-based TE-pass polarizer. The former work reports an ER of 25.26 dB and an IL of 0.21 dB within a moderate device length of 4.5 μm. The latter one reports an ER as high as 42 dB and a low IL of 0.38 dB. However, both of them are experimentally unfeasible using standard CMOS-compatible technology despite the attractive device performance indices [21]. Consequently, we can conclude that the key requirements for designing a TE-pass polarizer are high ER, low IL, wide operating bandwidth, small footprint, low power consumption, low cost, large fabrication tolerance, simple construction and ease of integration.

In this paper, combining metal-induced polarization dependence of SPP mode with intrinsic birefringence of SOI waveguide, a TE-pass polarizer consisting of alternating Cu/Si_3N_4 layers with the purpose of suppressing TM mode propagation in Si stripe, is proposed and investigated numerically. Notice that, it is distinctively different from all the previous ones reported in [12]–[20]. First, considering the Si_3N_4 itself a good dielectric Cu^{2+} ion diffusion barrier and its good adhesion to copper, the device could be fabricated free from using optically lossy diffusion barriers [27]. Second, the essential metal layers are designed outside Si stripe to minimize their adverse impacts on TE mode propagation. Third, no tapered structure with large footprint is needed for TE phase matching or mode conversion. Fourth, compared with noble metals and 2-D materials like graphene, metal of Cu is the most appropriate one for its CMOS compatibility, low cost, and good plasmonic behavior [15]. Specifically, Cu has obvious advantages over silver (vulnerable to oxidization), gold (costly to use), and aluminum (poor plasmonic behavior in near-infrared region). Fifth, the slab construction makes itself easy to be fabricated, integrated with other plasmonic components and extended for many other applications. Last but not least, we first propose and analyze the connection between SPP mode excitation efficiency and device performance, which is neither proposed nor studied. Previous studies mostly focus on how to convert a TM dielectric mode to a SPP one utilizing electric component polarized vertically to a metal/insulator interface. Therefore, our designed polarizer with attractive features is worth investigating, despite the fact that it is not yet implemented experimentally.

2. Numerical Simulations

2.1 Modelling and Design

Fig. 1 shows schematic view of the polarizer without keeping aspect ratio for the structure. A Si stripe waveguide with width of $W = 500$ nm and height of $H = 275$ nm is the basic structure on SOI substrate [6]. WG_1 (WG_2) with length of $l_1 = 500$ nm ($l_2 = 500$ nm) is the input (output) waveguide. Without blocking SPP power transfer, 2 μm-long Cu (Si_3N_4) layers with fixed (varying) thickness of $t_m = 30$ nm (t_d) are used. For ease-of-fabrication and compactness, we use 7/6-layer

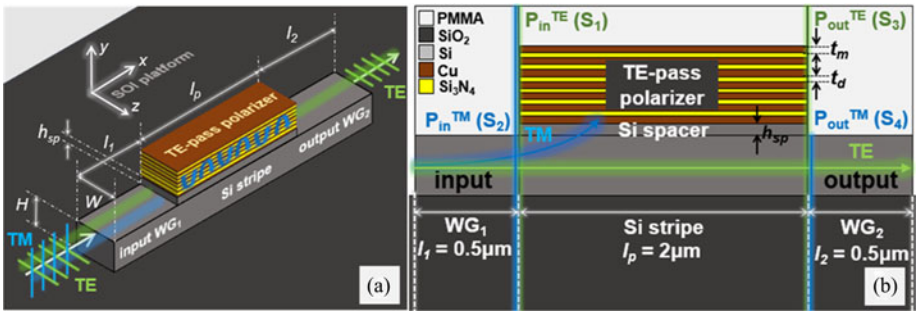

Fig. 1. (a) Three-dimensional and (b) lateral schematic view of the proposed TE-pass polarizer consisting of alternating Cu/Si_3N_4 layers based on a Si stripe waveguide etched on the SOI platform.

Cu/Si_3N_4 structure to keep it with a similar size as the Si stripe despite that more Cu layers could probably absorb more TM power. The cladding made out of polymethyl methacrylate (PMMA) is used because it is necessary, on the one hand, for preventing the formation of copper oxide which is a Cu^{2+} ions source leading to copper contamination, on the other hand, for directly integrating with other plasmonic components [22], [24]. At 1550 nm, the relative dielectric constants of Cu, Si_3N_4, SiO_2, Si, and PMMA are 0.606 + 8.26i, 1.97, 1.45, 3.48, and 1.481, respectively [25]. In our modelling, TE (TM) mode is transverse electric (magnetic) wave that has in-plane magnetic (electric) field components as marked in Fig. 1(a). Based on the finite element method, boundary mode analysis is used to solve the mode index n_{eff} (real part of effective mode index) of Si stripe waveguide and multilayer Cu/Si_3N_4 structure. A numerical port is set for launching the fundamental TE/TM mode. Perfectly matched layers are exerted on all boundaries of the simulation domain. Mesh refinement allowing accurate local field solving is made around all metal/insulator interfaces. Specifically, the size of free triangular mesh for cladding and substrate is set as 1 nm $\sim$ 50 nm, for Cu and Si_3N_4 slabs is set as 0.1 nm $\sim$ 5 nm, and for Si waveguide is set as 1 nm $\sim$ 10 nm. The mesh minimum is sufficient for convergence of simulation results.

Device performance indices for evaluating the polarizer are introduced in the following. We first define the *x*-component of power flux density as *Poavx*. Then light power P_{in}^{TE}, P_{in}^{TM}, P_{out}^{TE}, and P_{out}^{TM} are calculated as integral values of *Poavx* along corresponding boundaries. As marked in Fig. 1(b), green lines S_1 and S_3 (blue lines S_2 and S_4) are integral boundaries for TE (TM) power calculations. Thus P_{in}^{TE}/P_{in}^{TM} ($P_{out}^{TE}/P_{out}^{TM}$) is the TE/TM power entering into (output) the Cu/Si_3N_4 layers-coated Si stripe, which effectively avoids counting propagation losses caused by WG_1 and WG_2 themselves in. Therefore, expressions for ER of TE mode and insertion loss IL_E/IL_M of TE/TM mode are defined as

$$ER = 10\log_{10}(P_{out}^{TE}/P_{out}^{TM}) \quad (1)$$

$$IL_E = 10\log_{10}(P_{out}^{TE}/P_{in}^{TE}) \quad (2)$$

$$IL_M = -10\log_{10}(P_{out}^{TM}/P_{in}^{TM}). \quad (3)$$

It should be noted that we use S_3 to calculate P_{out}^{TE} for the purpose of taking the impact of polarizer on TE mode propagation into account. On the contrary, we use S_4 to calculate P_{out}^{TM} because SPP power confined in and consumed by the Cu/Si_3N_4 layers is exactly desired. The absorbed part of P_{out}^{TM} is not considered as the residual TM power that could continue propagating in WG_2. In addition, operating bandwidth BW of the polarizer is evaluated by calculating a spectrum range maintaining ER $>$ 20 dB.

2.2 Connection Between Mode Property and Device Performance

To begin with, two operating modes supported in the Si stripe are TE mode with $n_E = 3.0033$ and TM mode with $n_M = 2.4851$. An Si spacer with length of $l_p = 2\mu$m, width of $W = 500$ nm and

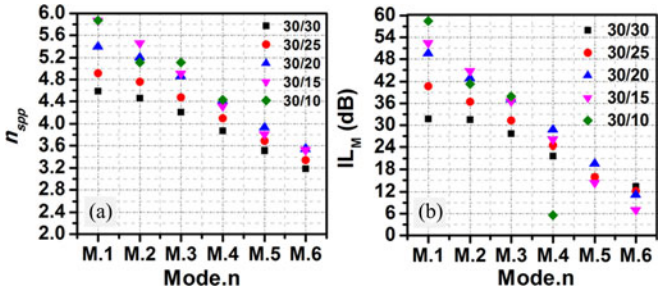

Fig. 2. (a) Mode index n_{spp} and (b) IL_M for SPP modes M.1–M.6 calculated for different Cu/Si_3N_4 layers thickness t_m/t_d.

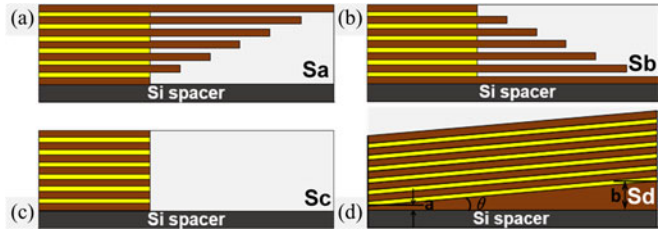

Fig. 3. Lateral schematic views of the polarizer with optimized multilayer structures. (a) Sa, (b) Sb, (c) Sc, and (d) Sd.

height of $h_{sp} = 55$ nm is required and directly added on the Si stripe for the purpose of satisfying phase matching of TE mode. This is because the Cu/Si_3N_4 layers-coated Si stripe presents a mode index slightly different from the n_E of WG_1 and WG_2. Next, we solve the first six SPP eigenmodes supported in the polarizer and calculate IL_M values each SPP mode can achieve. According to n_{spp} values from maximum to minimum, these SPP modes are named by symbols Mode.n in the order of M.1–M.6. As shown in Fig. 2, n_{spp} and IL_M of M.1–M.6 are calculated for different t_d. Fig. 2(a) shows that t_d variation has no impact on n_E of TE mode due to the overlapped data points. The Cu/Si_3N_4 layers with thickness of $t_m/t_d = 30/30$ [nm] present a minimum n_{spp}. Fig. 2(b) shows IL_M behaviors of M.1–M.6, on the one hand, M.1 with maximum n_{spp} tends to be attenuated more thoroughly, which is reflected in its maximum IL_M. On the other hand, the attenuation capability of the device goes down rapidly as the manner of n_{spp} does. In a regularly shaped plasmonic nanostructure such as the horizontally placed Cu/Si_3N_4 layers, we can assume that an efficiently excited SPP mode with deeply penetrated power in metal is always accompanied with a steady field distribution and a large mode index. However, there are seldom experimental approaches that can excite such kind of SPP modes due to their very large mode indices. Therefore, exciting a SPP mode with n_{spp} as large as possible by a TM wave directly injected into WG_1 with merely $n_M = 2.4851$ is the most practicable way. Predictably, to confine and exhaust TM mode as much as possible, it is required to improve n_M of WG_1 or diminish n_{spp} of polarizer to some extent. For fixed $n_M = 2.4851$, we could only try to pull down the n_{spp} to approach n_M, that is, narrow the difference value Δ of mode index between WG_1 and polarizer. It is assumed that the device performance could also be improved by narrowing Δ.

2.3 Structure Optimization and Performance Improvement

We propose an approach of breaking symmetry of the Cu/Si_3N_4 structure in horizontal or vertical direction without adding or reducing layers, with the purpose of destroying the steady SPP mode profiles with large n_{spp} supported in the original structure plotted in Fig. 1. The four optimized multilayer structures labeled as Sa, Sb, Sc, and Sd are shown in Fig. 3(a)–(d), respectively. The two structures whereas the structure Sc has Cu/Si_3N_4 layers in the same lengths. The

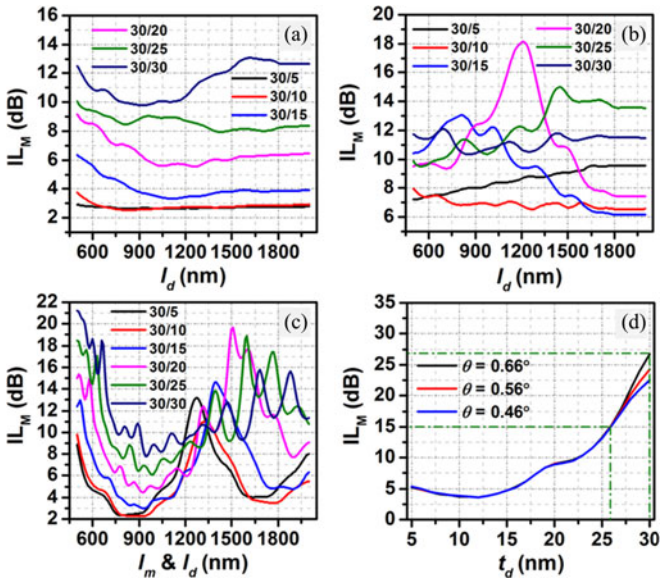

Fig. 4. Dependence of IL_M on (a) l_d of Sa, (b) l_d of Sb, (c) l_m and l_d of Sc, and (d) t_d of Sd for different tilt angles θ.

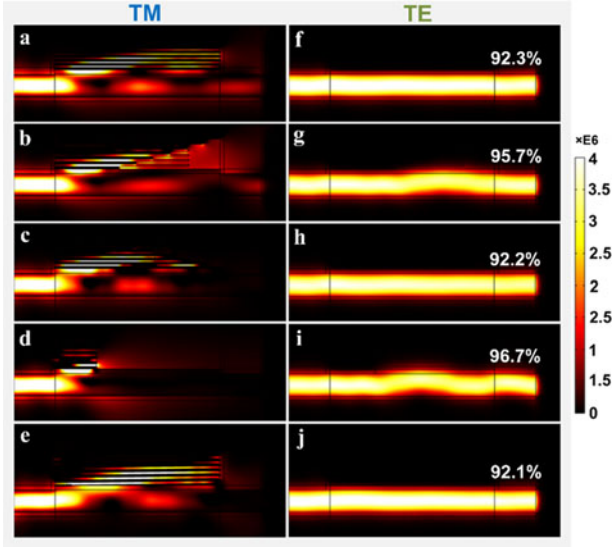

Fig. 5. (a)–(e) *Poavx* distributions of TM mode for original structure Sa, Sb, Sc, and Sd, respectively. (f)–(j) *Poavx* distributions of TE mode for original structure Sa, Sb, Sc, and Sd, respectively. (See Fig. 7 for detailed structure outlines.)

wedge-shaped structure Sd presents a tilt angle θ compared with the original structure with horizontal layers. All the structures are filled with PMMA.

Fig. 4(a)–(d) show the dependence of IL_M on structural parameters for Sa-Sd in sequence. In Fig. 4(a), with length of Si_3N_4 layers l_d varying from 500 nm to 2000 nm, Sa with $t_m/t_d = 30/30$ [nm] presents the maximum $IL_M = 13.07$ dB. In Fig 4(b), Cu/Si_3N_4 layers with $t_m/t_d = 30/20$ [nm] can lead to a maximum $IL_M = 18.13$ dB. In Fig. 4(c), with varying length l_m&l_d of Cu/Si_3N_4 layers, Sc shows a similar behavior with Sa, $t_m/t_d = 30/30$ [nm] leads to a maximum $IL_M = 21.25$ dB. Then, in Fig. 4(d), Sd with larger tilt angle $\theta = 0.66^\circ$ and $t_d = 30$ nm achieves the maximum $IL_M = 26.77$ dB.

Next, as can be seen in Fig. 5, we present TM (5(a)–5(e)) and TE (5(f)–5(j)) mode propagation behaviors in the form of *Poavx* distributions for Sa-Sd, exploring the optimized device performance.

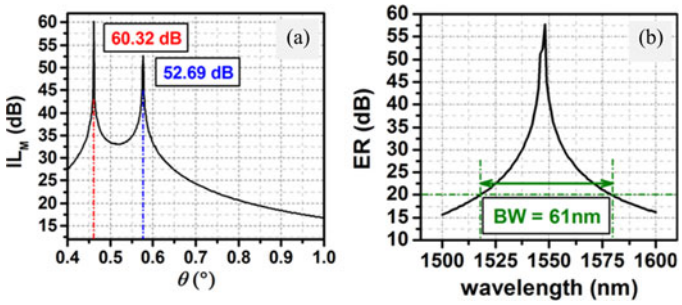

Fig. 6. Dependence of (a) IL_M on tilt angle θ. (b) ER on incident wavelength for Sd.

Notice that, on one hand, TM *Poavx* distributions are presented with their best TM-attenuation capability as given above, and on the other hand, each TE *Poavx* distribution is labeled with calculated TE power propagation efficiency which is defined as ratio of P_{out}^{TE} to incident power 1[W]. Let us focus on the TM mode first. For the original structure shown in Fig. 5(a), we notice that in addition to some TM power converting into confined SPP power, there is still a large portion of TM power directly passes through Si stripe and entering into WG_2. In Fig. 5(b), rather than suppressing or eliminating TM power, top long Cu layers introduce hybrid SPP mode that is reflected back and forth between Si stripe and Cu layers. That is, a metal-insulator-semiconductor region supporting hybrid SPP mode is formed due to the low-index material filled between Cu layers and Si stripe [26]. Moreover, there is still residual TM power passing through. In Fig. 5(c), the uncoupled TM power entering into WG_2 mainly comes from the TM dielectric mode propagating in Si stripe. Here we need to give some explanations. In the case of keeping all *Poavx* illustrations exactly sharing one color bar with same scale, we cannot see the part of power in WG_2 very clearly. Simulation results with a color bar scaling from 0 to 3 with 6 orders of magnitude can give a clear view similar to Fig. 5(a). Then, Fig. 5(d) shows that there is little SPP power confined in Cu/Si_3N_4 layers, the most of power is propagating along Si-PMMA interfaces. Fig. 5(e) shows a wedge-shaped Cu/Si_3N_4 structure can eliminate TM mode with $IL_M = 26.77$ dB. As can be seen clearly, the most TM power is converted into confined SPP power despite the fact that there is still residual TM power existing in Si stripe. However, different from the case happened in Fig. 5(c), we see no power enters into WG_2 while adjusting the color bar. Then in terms of the TE mode propagation, we can see from Fig. 5(f), (h), and (j), the TE mode profiles are well maintained due to the bottom 2 μm-long Cu layer being directly coated on Si stripe. However, the cases in Fig. 5(g) and (i) are different because of the relatively shorter bottom Cu layers of 1520 nm and 500 nm. Therefore, Sa and Sc showing less metal contact to Si stripe can cause less absorption loss to TE mode which is reflected in higher power propagation efficiency, whereas other structures with 2 μm-long bottom Cu layers suppress TE mode to some extent and result in relatively lower power propagation efficiency. In addition, simulation results show that, polarizers based on original structure and structure Sa-Sd, can achieve ER of 12.27 dB, 13 dB, 18.19 dB, 21.4 dB, and 26.63 dB, respectively.

There is no doubt that SPP-based component is an ideal tool to realize polarization state control. Although increasing metal usage can improve the device performance, increased accompanying absorption will deteriorate TE mode propagation. Even if the problem can be solved using external directional coupler to split TM mode, the device footprint is too large to be compact. In other words, with regard to the bottom Cu layer cling to Si stripe, we try to find its optimum thickness to ensure both efficient SPP excitation and low absorption of TE mode. Then, for the best ER of TE mode based on structure Sd, keeping other Cu/Si_3N_4 layers unchanged, we merely optimize thickness of the bottom Cu layer. We let θ vary within a narrow range ($a = 1$ nm, $b < 25$ nm) and then calculate P_{out}^{TM}, where a (b) is the head (tail) thickness of the bottom Cu layer. As presented in Fig. 6(a), Sd achieves a maximum $IL_M = 60.32$ dB at $\theta = 0.462^\circ$ and a second maximum $IL_M = 52.69$ dB at $\theta = 0.577^\circ$. The sweeping step length used in simulation is $\theta = 0.001^\circ$. We prefer the structure Sd with $\theta = 0.577^\circ$ due to its larger $b = 21$ nm. Consequently, the TE mode can pass through

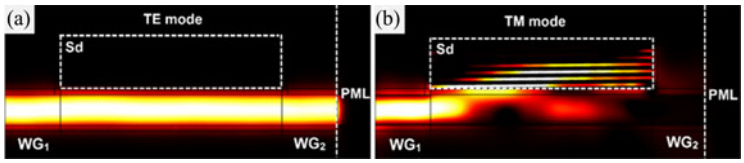

Fig. 7. For Sd with optimized a/b = 1/21 [nm] and $\theta = 0.577^{\circ}$, *Poavx* distributions for (a) TE and (b) TM mode propagation. (The unpresented color bar is the same as the one used in Fig. 5.)

Si stripe with extremely high ER = 52.34 dB and low IL_E = 0.35 dB. In addition, as calculated in Fig. 6(b), we obtain a moderate BW = 61 nm while maintaining an ER > 20 dB. One thing to note is that we calculate the BW without considering material dispersion because of the tiny difference of refractive index in wavelength range of 1500 ∼ 1600 nm. We use constant refractive index of 3.48, 1.45, and 1.97 for Si, SiO_2, and Si_3N_4 in the simulation [5].

In terms of loss mechanism, absorption and reflection caused by metals, mode mismatch between waveguides and radiation of rough slab surfaces might be responsible for the insertion loss of TE mode. For our design, absorption of the bottom Cu layer and mode mismatch are the main causes. However, the issues are desirably addressed by designing metal layers outside and inserting a Si space layer, giving rise to a well-matched TE mode profile. For the optimized structure Sd with $\theta = 0.577^{\circ}$ and device performance indices of ER = 52.34 dB and IL_E = 0.35 dB shown in Fig. 7, the TE mode is passing through with power propagation efficiency of 92.2%. Fig. 5(a) shows that for structure Sa, there is still some uncoupled power passing through WG2. However, in Fig. 5(d), structure Sd greatly contributes to the complete power coupling and ends up with little dielectric mode escaping out. In addition to high performance indices, structure Sd occupies full space and free itself from PMMA or some other low-index materials, which thus blocks the formation of hybrid SPP mode and relieves the fabrication process. Considering both power penetration into Cu layers and SPP coupling in Si_3N_4 layers, ultrahigh IL_M is a result of complete light-matter interaction in metal/insulator multilayer structure and high-efficient mode matching at inclined metal/insulator interfaces. In terms of the appearance of IL_M peaks in Fig. 6(a), we can explain it by figuring out the electromagnetic power loss distributions in bottom Cu layer for Sd with $\theta = 0.577^{\circ}$ (position of the second IL_M peak) and $\theta = 1^{\circ}$ (position of a general IL_M value). As can be expected, we find that the electromagnetic loss density of the former one is much higher than that of the latter one. In other words, higher electromagnetic loss in metals means more efficient SPP coupling and, thus, less dielectric mode.

3. Experimental Feasibility

According to [24], copper oxide being a source of Cu^{2+} ions could cause copper contamination via Cu^{2+} ions diffusion and drift into surrounding mediums, despite the fact that neither electric current nor heat is applied in our work. According to [27], optically lossy metals such as Ti, W, Pd, and TiN are applicable diffusion barriers used in plasmonic devices, however, optically low-loss silicon nitride with good adhesion to copper is recently considered as a perfect dielectric alternative. Here, fabrication processes for Sd-type polarizer could be introduced as following. First, a 330 nm-thick Si layer (a 275-nm thick Si stripe and a 55 nm-thick Si spacer) is prepared on glass substrate via chemical vapor deposition. Second, 30 nm-thick Cu layers and 30 nm-thick Si_3N_4 layers are prepared layer by layer via gradient plasmon enhanced chemical vapor deposition under specific temperature. Third, electron-beam lithography (to tailor designed device size) and gray-scale-beam lithography (to fabricate wedge-shaped layers at a tilt angle) are used to shape the designed structure [30]–[33]. Finally, PMMA cladding is deposited around. Notice that, the layer thickness could be precisely controlled via thin-film preparation techniques such as atom-layer-deposition, magnetron sputtering, and plasmon enhanced chemical vapor deposition [27]–[29]. As we all know, the length and width of a layer could be tailored very precisely via electron-beam lithography [28]. In addition, as suggested in [29], when we prepare a thin film using sputtering or evaporation,

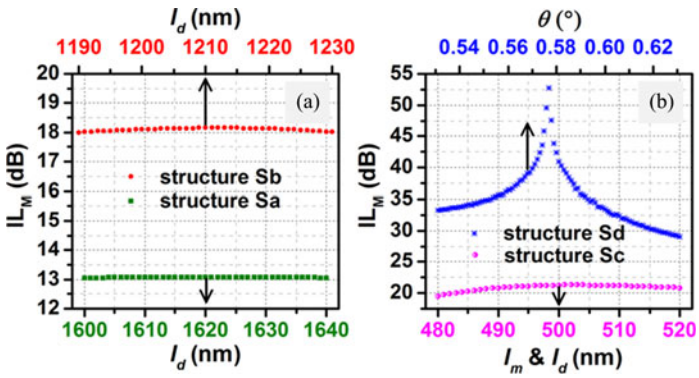

Fig. 8. Fabrication error tolerance of structures. (a) Sa and Sb. (b) Sc and Sd.

it is worth noting that film roughness and grain size generally scale with deposition thickness of the film. Then a feasible approach to prepare the film with large grain size and low surface roughness is introduced. We could first prepare a 1 μm-thick film and then reduce the film thickness to several nanometers by standard chemical mechanical polishing.

4. Fabrication Tolerance

During the fabrication process, lithography and film preparation could cause fabrication errors and performance variations to the device. In addition to achieving excellent performance indices analyzed above, the relatively large thickness and length of Cu/Si_3N_4 layers could also allow relaxed fabrication tolerance. That is, rather than a very thin metal (dielectric) film with t_m (t_d) $=$ 5 nm, when preparing a Cu (Si_3N_4) layer with t_m (t_d) $=$ 30 nm, no very accurate thickness control is required. As discussed in section 2.3, structure Sa and Sb have optimum values of IL_M (dB) at l_d $=$ 1620 nm and l_d $=$ 1210 nm, respectively. It can be seen from Fig. 8(a), IL_M of Sa and Sb keep themselves almost constant while l_d undergoing a deviation of $\pm$20 nm. In a similar way as shown in Fig. 8(b), Sc presents a relatively steady trend for l_d variations. However, IL_M of Sd drops to 29.02 dB from 52.69 dB as θ varies about 0.1°, exerting demanding technical requirements on the fabrication process. Therefore, in terms of the different level of accuracy control, the designed polarizer based on structures Sa, Sb, Sc, and Sd should be selectively chosen according to operating environments with different tolerance requirements.

5. Conclusion

In summary, we investigate a novel TE-pass polarizer aiming to attenuate the fundamental TM mode from an input Si stripe waveguide, whereas let the fundamental TE mode pass through without influence. Within an ultracompact device length of 2 μm, the polarizer can achieve ER as high as 52.34 dB, IL_E as low as 0.35 dB, and ultrahigh IL_M of 52.69 dB. Such a simple structure can be integrated with a wide variety of silicon photonic waveguides, because the slab construction makes it very easy to be reconfigured and adjusted according to each specific waveguide type. It is noteworthy that the wedge-shaped device presents an ultrasensitive behavior to tilt angle variation, which could be exploited as an angle sensor or a strain sensor. What's more, we first propose and analyze the connection between mode property and device performance that could be taken into consideration in future establishment and improvement for polarization diversity systems. In general, our work may play a part in implementing high-performance polarization diversity schemes in ultracompact nanophotonic integrated circuits.

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