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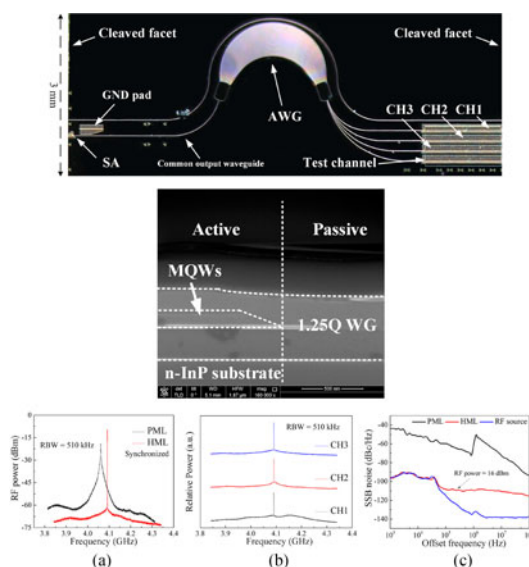Lingjuan Zhao
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Abstract: We report a low-cost arrayed waveguide grating (AWG) based mode-locked semiconductor laser designed for multichannel synchronous ultrashort pulse generation. Both the fabrication process and chip characterization results are discussed in detail. By deploying a bundle active–passive photonic integration technique, only one regrowth step is required to monolithically integrate a semiconductor optical amplifier array, an AWG, and a common saturable absorber on a single InP substrate. Combined with a shallow ridge waveguide structure common for both active and passive sections and formed in a single dry etching process, our process allows the fabrication of the monolithic photonic integrated circuit chip in a much simplified process. The fabricated device demonstrated multichannel mode-locking operation at a repetition frequency of 4.1 GHz in a fundamental mode-locking regime under both passive mode-locking and synchronous hybrid mode-locking conditions. Timing jitter as low as 1 ps was obtained, and preliminary pulse chirping characteristics were analyzed by a frequency-resolved optical gating technique. The exhibited performance makes our device a promising candidate as a multichannel ultrashort pulse optical source for future cost-effective *high-speed optical networking and signal processing applications*.

Index Terms: Active-passive integration, arrayed waveguide grating, photonic integrated circuits, semiconductor lasers, synchronized multichannel mode-locked lasers.

1. Introduction

Monolithically integrated semiconductor mode-locked laser diodes (MLLDs) are of great interest as ideal ultrashort optical source s for future high-speed optical networking and signal process applications, ranging from optical access network to bio-imaging and arbitrary waveform generation to remote sensing [1]–[3]. Semiconductor MLLDs with repetition rates of tens of gigahertz and extremely low timing jitter performance have been widely reported in the literature [4]–[6], with potentials to significantly scale up the operation speed of the whole systems. However, this puts stringent requirements on the corresponding electronic circuit section for the required high-speed

optoelectronic conversion process, in addition to the thermal issues associated with increasing power dissipation of faster electronic circuits. An effective solution for relaxing the electronic circuit operation speed requirements while maintaining the same system bandwidth is to employ a time- and wavelength-interleaved approach, where the pre-multiplexed optical modulation data streams are de-multiplexed into a parallel data processing block where an array of photodiodes and afford-able off-the-shelf low-speed electronics can be deployed [7]. The key challenge in this case lies in the realization of a synchronized multiwavelength channel mode-locked laser source with a relatively low repetition frequency but high channel count. Several multichannel pulse generation schemes have been proposed and demonstrated, including spectral slicing of a femtosecond mode-locked laser [8], dispersion-managed fiber ring mode-locked laser [9] and external cavity mode-locked laser design [10]. Although repetition frequency and wavelength channels of the proposed pulsed light sources can be easily tuned in these approaches, multiple discrete bulky components including semiconductor optical amplifier (SOA), modulator, polarization controllers, specialty fibers, and bulk optical elements are required, making the whole system bulky, costly, and sensitive to environmental perturbations, which, in turn, limit their volume manufacturing and large-scale field deployment.

InP-based photonic integrated circuit (PIC), on the other hand, offers an effective System-On-Chip solution where both active and passive optical components of a complex optical system can be monolithically integrated onto a single semiconductor substrate, leading to an ultra-compact, low cost, power efficient and highly reliable optical chip design that can be volume manufactured based on standard semiconductor manufacturing technologies [11]. Up to now, only a few PIC designs capable of multichannel mode-locking optical pulse generation have been reported. One approach was based on the multichannel DBR mode-locked laser array [12], which requires relatively expen-sive electron beam lithography for the DBR sections defining different wavelength channels, and an external optical injection scheme for synchronization. We have previously also reported an arrayed waveguide grating (AWG) based fifth-order harmonically mode-locked semiconductor laser using a commercial InP photonic foundry process in a Multi Project Wafer (MPW) run [13], [14], where an SOA array, optical delay lines, an AWG, an intracavity common saturable absorber (SA), and a common output SOA were monolithically integrated based on the butt-joint active-passive integra-tion approach in the InP platform, obtaining four-channel synchronized mode-locking operation in the fifth harmonic frequency of 12.7 GHz.

In this paper, we report our recent progress on developing a more cost-effective synchronized multichannel mode-locked semiconductor laser based on a flat-top spectral response AWG em-ploying an in-house fabrication process. In this AWG-based design, the chip can be easily scaled up to higher channel counts if required. The fabricated prototype laser operates in a fundamen-tal mode-locking regime with a repetition frequency of $\sim$4.1 GHz, a much lower repetition rate that would be compatible with the operation frequency of today's low-cost electronic circuits. Our prototype device employs a bundle integrated guide (BIG) process [15] to monolithically integrate multiple active and passive components. Compared with the previously reported butt-joint approach [13], in this case, only one single epitaxial regrowth step is required, thus significantly simplifying the fabrication process. The bundle process produces a very smooth active-passive interface thus minimizing residual reflections, which is critical for reliable operation of monolithic MLLDs, leading to a much wider biasing parameter space for stable mode-locking. A strong passive mode-locking (PML) tuning range of over 65 MHz has been demonstrated. Our process also deploys a simple single step dry etching process defining the shallow ridge waveguide for both active and passive sections. Time and frequency domain operational characteristics under both passive and hybrid mode-locking regimes were characterized in detail. Pulse chirping characteristics were also quan-tified using frequency-resolved optical gating (FROG) technique in a preliminary study showing linear chirped pulse that can be further compressed. Overall, we believe our device design, pro-cess and performance demonstrated a potential viable technology path for high-volume low-cost synchronized multichannel ultrashort pulse applications.
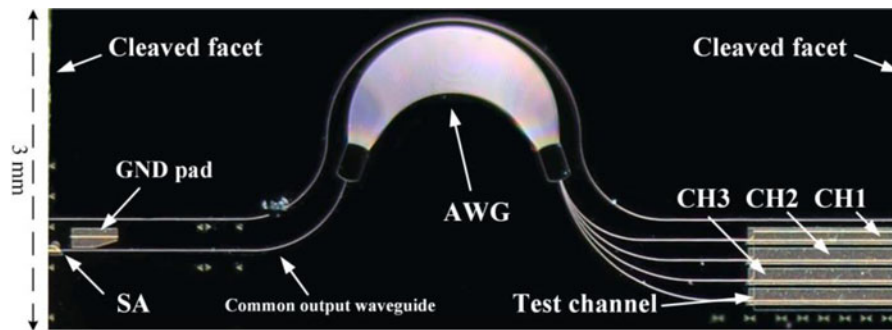
Fig. 1. Optical microscope image of the fabricated AWG-based synchronized multichannel mode-locked semiconductor laser. The device operated under both passive and hybrid mode-locking conditions. The RF ground contact (GND) was fabricated right next to the saturable absorber contact for direct on chip RF probing.

2. Device Design and Fabrication

An optical microscope image of the fabricated multichannel AWG-based fundamentally mode-locked semiconductor laser (AWGMLSL) is shown in Fig. 1. The device consists of three sections: 1) an SOA gain array section (active) with a channel spacing of 200 μm, which provides optical gain for each wavelength channels; 2) a 375 GHz channel spacing AWG (passive) with a flat-top spectral response, designed to precisely divide the broad gain spectrum of each SOA into different channels with equal wavelength separation, and allowing individual channel mode-locking operation with a relatively broad spectral width for producing a narrow optical pulse; and 3) a common SA section (active), sharing the same multiple quantum well (MQW) active material as the SOA array, located at the left cleaved edge of the common output waveguide as shown. Each of the SOA sections, along with the corresponding channel of the spectral filtering AWG and the common SA section forms a distinct mode-locking laser cavity at a unique wavelength channel (total channel cavity length defined by cleaved facets is $\sim$10200 μm, corresponding to a fundamental mode-locking frequency of $\sim$4.05 GHz). The overall chip dimension is 3 $\times$ 8 mm^2.

The AWGMLSL chip fabrication process started with a metal–organic chemical vapor deposition (MOCVD) process by growing the n-cladding layers and the active region epitaxial structure, where a 500-nm n-doped InP buffer layer, an undoped 250-nm-thick InGaAsP quaternary waveguide layer of bandgap wavelength 1.25 μm (1.25 Q), a 20-nm-thick undoped InP etch stop layer, and an InGaAsP based MQW active region with six compressively strained InGaAs-InGaAsP MQWs were successively grown on a n-type InP substrate. The passive section was formed by masking the active region using a SiO$_2$ masking layer grown by plasma enhanced chemical vapor deposition (PECVD), and then etching away the MQW active region in the passive section using a selective chemical etch, stopping on the InP etch stop layer. After removing the SiO$_2$ mask, a one single regrowth step completed all the remaining epitaxial layer stack by growing in sequence an undoped top 1.25 Q waveguide layer, p-type InP cladding, and the p-type InGaAs contact layer across the entire wafer. Compared with the butt-joint active-passive technique, this integration approach employs only a single regrowth step and produces a very smooth active-passive interface with minimal index discontinuity, as is shown in Fig. 2. This is critical for stable operation for an integrated mode-locking laser chip, which can be easily disrupted by residual reflections at the active-passive interface [16], and allows for a broad tuning range of stable mode-locking operation. Afterward the uniform 3-μm-wide 2-μm-deep ridge waveguide was formed using standard photolithography process and inductively coupled plasma (ICP) etching, stopping slightly inside the top 1.25 Q waveguide layer, defining both the active and passive waveguide sections. The ridge sidewalls were then protected by depositing an additional SiO$_2$ layer. Contact window opening, p- and n-metal definitions and rapid thermal annealing all followed standard semiconductor laser fabrication process. The SOA gain sections and the SA section are designed to be 1500 μm and 100 μm, respectively.
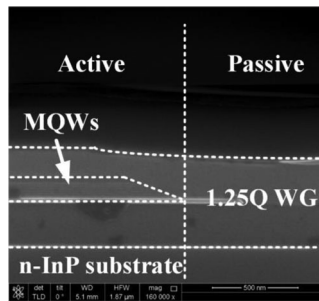
Fig. 2. SEM cross-sectional image of the active-passive interface using the bundle active-passive integration approach.
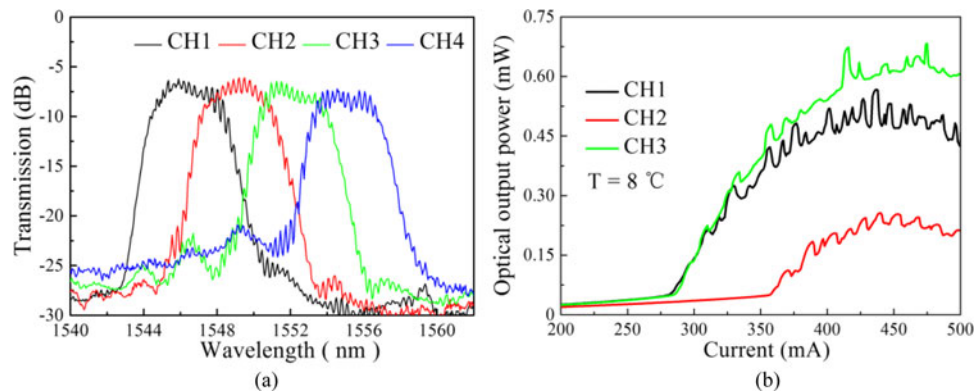

Fig. 3. (a) TE mode transmission spectra of the 1 × 4 AWG with flat-top spectral response design. (b) CW L-I curves of the three consecutive channels (the fourth channel was not in operation due to passive waveguide damage during fabrication) of the AWGMLSL chip with the common SA section unbiased and the SOA section forward biased at a stage temperature of 8 °C.

3. Device Characterization

We first measured the TE mode transmission characteristics of the 1 × 4 AWG used in our chip design, fabricated separately as a test structure. In order to obtain a flattened spectral response, we added a multimode interferometer at the common output waveguide side in conjunction with the adjacent free propagation region. More design details and fabrication procedure can be found in [17]. As is shown in Fig. 3(a), the average channel spacing of the passive AWG is around 3 nm, with an average 3-dB spectral width of ~3.5 nm, and the AWG insertion loss is about 7 dB, which is comparable with other InP AWG performance reported in the literature.

A fabricated multi-channel AWGMLSL chip was mounted p-side up onto a Cu heatsink and tested at a fixed stage temperature of 8 °C, controlled by a thermoelectric cooler. One of the channels was not operational due to passive waveguide damage during processing, and we labeled it as a test channel in Fig. 1. Rest of the characterization efforts was focused on the remaining three adjacent channels. Fig. 3(b) shows a typical continuous wave (CW) light-current (L-I) curves of the three channels of the AWGMLSL chip with the common SA section left floating and SOA sections forward biased. Lasing thresholds were between 285 mA and 355 mA. The relatively high lasing threshold of this prototype chip are mainly attributed to two processing related issues: a) By employing secondary ion mass spectrometry (SIMS) analysis technique, relatively high background silicon and oxygen doping at the regrowth interface was observed right above the MQW region, which can act as an n-type inversion layer and non-radiative recombination centers degrading the internal quantum efficiency and causing higher lasing threshold; b) the measured passive waveguide propagation loss was around 3~4 dB/cm, mainly due to scattering losses of the relatively rough waveguide
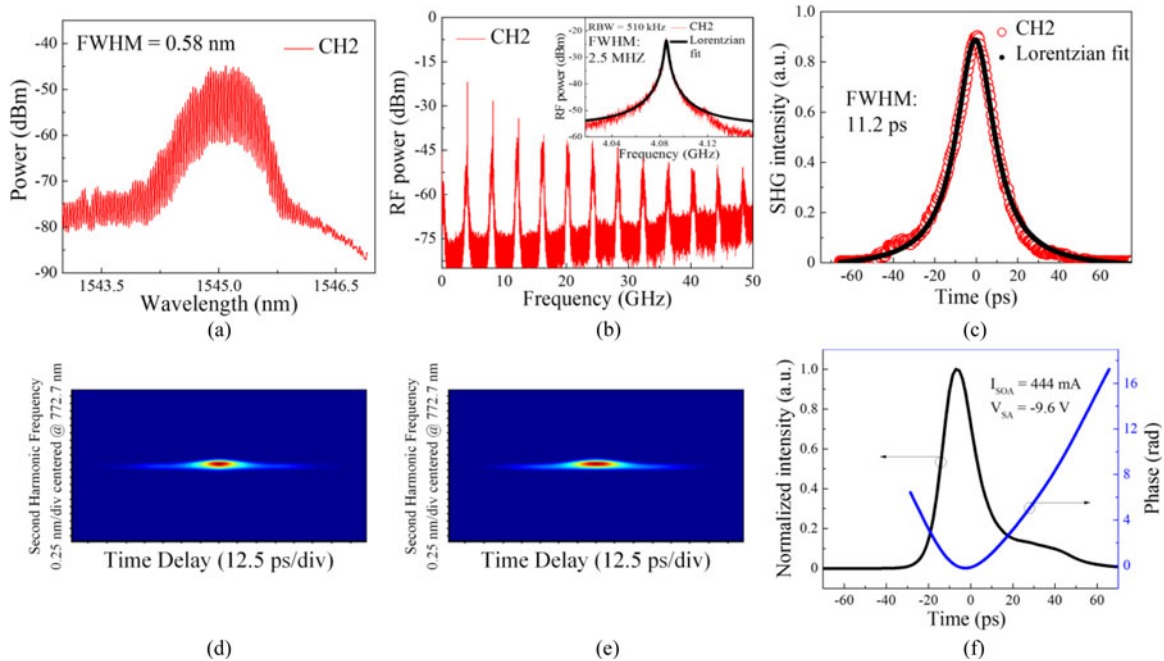
Fig. 4. Representative single channel passively mode-locking of the AWGMLSL chip (a) zoomed-in view optical spectrum, (b) full-span RF spectrum (inset: zoomed-in view around fundamental frequency with Lorentzian fit), (c) time domain autocorrelation trace experimental result of a short pulse with Lorentzian fit, (d) measured FROG spectrogram, (e) recovered FROG spectrogram from fitting, and (f) retrieved pulse intensity profile and temporal phase. (Bias condition: $I_{SOA-CH2}$: 444 mA, $V_{SA} = -9.6$ V, T = 8 °C).

side walls, which is higher compared to our previously reported butt-joint case [13]. These two processing related issues are both well understood and will be improved in future fabrication runs.

PML operation of each individual mode-locked channels was first achieved by forward biasing the SOA gain section current and reverse biasing the SA section at appropriate levels (CH1: $I_{SOA} = 425$ mA, $V_{SA} = -8.5$ V; CH2: $I_{SOA} = 444$ mA, $V_{SA} = -9.6$ V; CH3: $I_{SOA} = 494$ mA, $V_{SA} = -9.4$ V). The mode-locking performance was characterized in detail by coupling the AWGMLSL chip optical output to a lensed anti-reflection coated single mode fiber. Then via an optical isolator (>45 dB isolation), the signal was amplified with an erbium-doped fiber amplifier before routing to an Optical Spectrum Analyzer (OSA) for optical spectrum monitoring, a 50 GHz photodetector connecting to an Agilent PXA N9030A Signal Analyzer for microwave spectrum measurements, and an A.P.E. second-harmonic generation autocorrelator for time domain characterizations.

Fig. 4(a) shows a zoomed-in view of the optical spectrum of a representative channel. The full width at half-maximum (FWHM) spectral widths of each individual mode-locked channels are in the range of 0.58 nm to 0.71 nm. A 50-GHz span view of the RF power spectrum of the same representative channel is shown in Fig. 4(b). Strong fundamental mode-locking spectral peak near 4.08 GHz with higher order harmonics can be clearly observed with a >50 dB signal-to-noise-floor ratio. The measured FWHM RF linewidth is 2.5 MHz (RBW = 510 kHz) as shown in the inset of Fig. 4(b) along with a Lorentzian fit. The relatively broad linewidth is mainly attributed to the low Q factor of the mode-locking cavity [18], which is caused by the aforementioned excessive losses introduced during processing. We expect reduced lasing thresholds with a narrower RF linewidth for the AWGMLSL chip in later optimized waferfab runs. Fig. 4(c) shows the time domain autocorrelation trace of the same mode-locked channel. Assuming a Lorentzian pulse shape, the extracted FWHM pulse width of all three individually mode-locked channels ranged from 11.2 ps to 15.9 ps. Pared with the corresponding optical spectral width, the time-bandwidth products (TBPs) of the
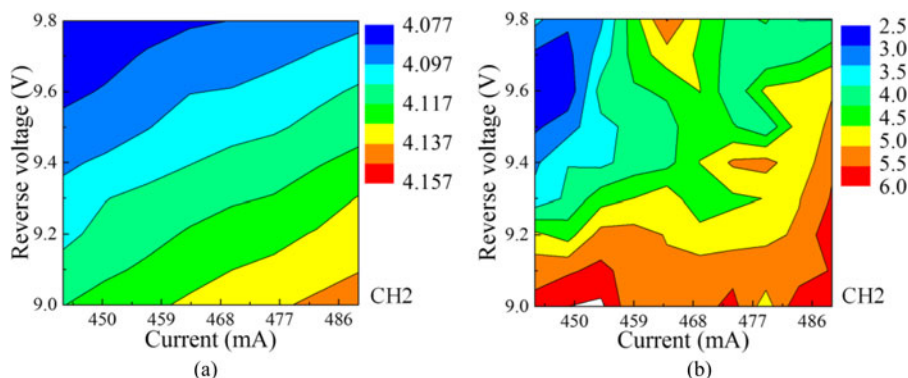
Fig. 5. (a) Repetition rate and (b) linewidth as a function of the gain section forward biased current and the SA section reverse biased voltage of a representative passively mode-locked channel of the AWGMLSL chip.

AWGMLSL laser channels were between 0.8 to 1.4. These TBP values are somewhat larger than the Lorentzian pulse transform limit, indicating the optical pulse contains chirping, which can be attributed to the interplay of self-phase modulation effects between the SOA gain and SA sections [19]. We further examined the optical pulse characteristics by employing a second harmonic generation frequency-resolved optical gating (SHG-FROG) technique giving true pulse shape and phase information of the optical pulse, which is not available from autocorrelation measurement [20]. The measured raw SHG-FROG spectrogram is shown in Fig. 4(d) with a color-coded intensity profile. Fig. 4(e) shows the numerically recovered spectrogram with a retrieval error equal to 7.2E-5, which proves the result is reliable according to [20]. The retrieved pulse intensity profile and temporal phase are plotted in Fig. 4(f). We see that a steeply rising leading edge with a long trailing edge is observed in the retrieved pulse profile, which explains the small plateau in the lower part of the autocorrelation trace shown in Fig. 4(c). The temporal phase is roughly quadratic, leading to a linear chirping of the optical pulse, which means the pulse can be further compressed by external off-chip dispersion compensation. Further detailed FROG experiments are underway and systematic analysis will be reported in a later publication.

Frequency tunability is another important mode-locked laser characteristic as it makes them more tolerant against manufacturing process variations and field operation conditions. We investigate the mode-locking frequency of a given passively mode-locked laser channel, as a function of the gain section current and the SA reverse voltage, as shown in Fig. 5(a). We can see that the mode-locking frequency increases monotonically with higher forward biased current and decreases with greater reverse biasing voltage, leading to a broad tuning range greater than 65 MHz while maintaining stable mode-locking. Corresponding RF linewidth evolution of the mode-locked channel under the same operating conditions are also plotted in Fig. 5(b). We could see a gradual RF linewidth broadening trend in the contour map with a combined contribution of increasing forward biased current and reducing reverse biasing voltage. The RF linewidth remains below 6 MHz under the investigated tuning range.

Simultaneous multichannel PML operation at same frequency was then achieved by fine tuning the mode-locking frequency through adjusting the SOA gain section current at 432 mA, 460 mA, and 474 mA for CH1, CH2, and CH3, respectively. The SA section reverse voltage was set at −7.7 V. Fig. 6(a) shows the optical spectrum of the AWGMLSL with all the channels simultaneously operating under the PML conditions, measured through the common output waveguide. The optical output power nonuniformity between channels is less than 2 dB, which is largely caused by waveguide loss variations experienced by the corresponding wavelength channels due to fabrication process variations. Further process improvements are underway. The frequency power spectrum of each individually mode-locked channels can be verified by applying a tunable optical bandpass filter
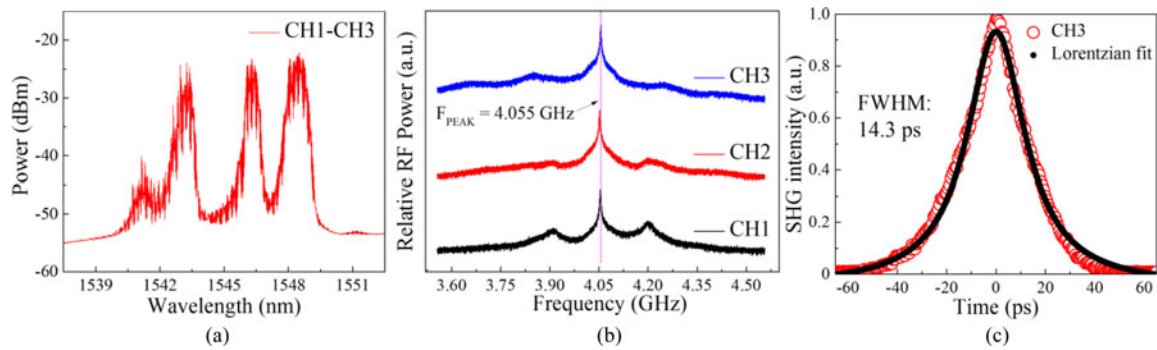
Fig. 6. AWGMLSL chip under simultaneous multichannel PML operation (a) optical spectrum, (b) zoomed-in view of RF power spectra of all three channels filtered by a tunable bandpass filter, and (c) autocorrelation trace of a representative mode-locked channel filtered by a tunable bandpass filter (operating condition: $I_{SOA-CH1}$: 432 mA, $I_{SOA-CH2}$: 460 mA, $I_{SOA-CH3}$: 474 mA, V_{SA} : −7.7 V, T = 8 °C).
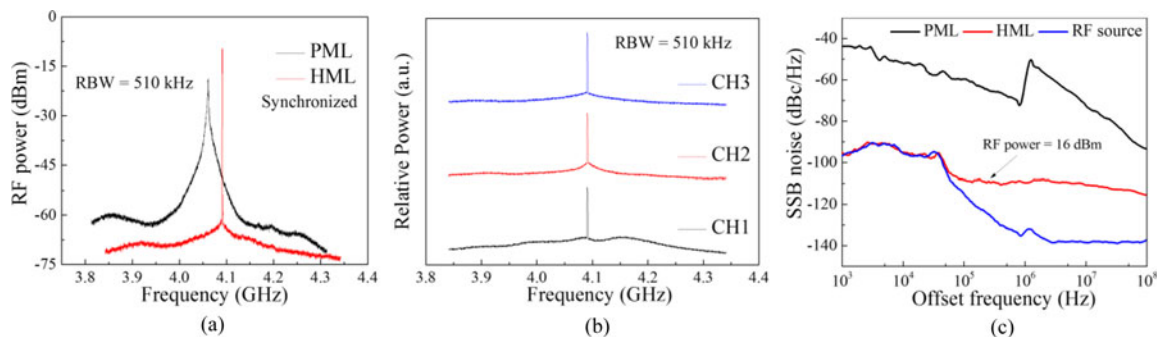

Fig. 7. Multichannel simultaneous mode-locking operation measured through the common output waveguide (a) fundamental RF spectral peak under the simultaneous PML and the synchronized HML conditions, (b) HML RF power spectra of individual mode-locked channels filtered with a tunable bandpass filter, and (c) single sideband phase noise plots (1 kHz – 100 MHz) comparing the simultaneous PML and the synchronized HML conditions, as well as RF clock source. Simultaneous PML Bias conditions same as in Fig. 6. HML conditions: RF driving frequency: 4.09 GHz, RF input power: 16 dBm.

tuned to the desired wavelength channel of the optical output signal. A zoomed-in view of the RF power spectra of each of the individually mode-locked channels are shown in Fig. 6(b), we can see that all the channels were indeed operating at the same fundamental frequency of 4.055 GHz after careful tuning of the biasing conditions. Fig. 6(c) shows the measured autocorrelation trace of a representative channel under the simultaneous multichannel passive mode-locking condition, isolated by employing the same tunable bandpass filter approach. The deconvolved pulse widths assuming a Lorentzian pulse shape for all three channels ranged from 9.3 ps to 14.5 ps. For practical system applications, optical pulse train with low timing jitter is desirable, with below 1 ps a reasonable figure of merit [3]. Simultaneous multichannel passively mode-locked optical pulse train has high overall timing jitter and phase noise due to the absence of synchronization to external clock, both between channels and from pulse to pulse within the same channel output. This is reflected in the broad linewidth of the fundamental RF frequency tone as shown in Fig. 6(b) presenting individual channels or in Fig. 7(a) for the combined output of three simultaneously operated PML channels.

Electrical modulation on the SA section with an external RF clock signal will lead to a hybrid mode-locking (HML) operation, with sharply reduced timing jitter and optical pulse synchronization to the electrical clock [21]. We applied an RF clock signal to the common SA section of the AWGMLSL through a Bias-Tee with a ground-signal probe. By optimizing the RF driving frequency and input power (frequency = 4.09 GHz, power = 16 dBm), a maximum pedestal suppression around the

mode-locking frequency was obtained as shown in Fig. 7(a), with a dramatic RF linewidth narrowing compared to the simultaneous PML case, measuring the simultaneous multichannel optical output from the common output waveguide. Individual channels of the synchronous HML state were also characterized by applying the same tunable bandpass filtering technique. Fig. 7(b) shows the fundamental frequency RF power spectra of all three mode-locked wavelength channels that were precisely locked to the 4.09 GHz RF clock signal, and maintaining good mode-locking stability. Single sideband (SSB) phase noise plots of the multichannel mode-locked AWGMLSL chip under the simultaneous PML condition, the synchronous HML condition, as well as the RF clock source (Agilent 83623B) centered at 4.09 GHz were compared in Fig. 7(c), respectively. Integrating from 1 kHz to 100 MHz, we obtained a timing jitter of 0.21 ps for the RF clock, 1 ps for the HML synchronous AWGMLSL combined output signal from the three wavelength channels, while the corresponding value for the PML case was 112 ps. The small timing jitter for the HML case shows that synchronous hybrid mode-locking operation has indeed been achieved between the three wavelength channels. We expect the timing jitter to further decrease in following up optimized wafer runs with reduced waveguide losses and the incorporation of a polyimide-planarized SA structure design for reducing SA section capacitance, as well as an impedance matched RF probe in the measurement setup, resulting in enhanced hybrid mode-locking efficiency.

4. Conclusion

We present for the first time detailed design, fabrication and characterization results of a low-cost synchronized multichannel AWG-based mode-locked laser, operating at a fundamental repetition rate of ~4.1 GHz. By combining a bundle active-passive integration process with a shallow ridge waveguide structure for both active and passive sections, only one regrowth step plus one dry etching process were required, which leads to a greatly simplified fabrication process of the integrated photonic chip compared to the traditional butt-joint integration approach as well as improved mode-locking stability by minimizing residual intracavity reflections. By adjusting the biasing conditions of individual wavelength channels, passive mode-locking with a broad tuning range of >65 MHz was demonstrated. Optical pulse quality was also analyzed in detail. Optical pulse with linear chirp has been observed through SHG-FROG measurement, indicating potential for further pulse compression through dispersion compensation. Synchronous multichannel mode-locking operation with timing jitter down to 1 ps was demonstrated in the electrical HML conditions. Further timing jitter performance improvement is expected in future wafer runs with the help of the improvement of the fabrication process, as well as the RF test setup upgrade. The relatively low fundamental frequency operation at 4.1 GHz is also compatible with the state-of-the-art low-cost electronic front-end circuits. Overall we believe our result s here demonstrate the potential feasibility of the monolithic integrated AWGMLSL chip designed for future cost-effective semiconductor MLLDs based high-performance signal processing and optical networking systems.

References

[1] P. J. Delfyett, "Ultrafast single- and multiwavelength modelocked semiconductor lasers: Physics and applications," in *Ultrafast Lasers: Technology and Applications*, New York, NY, USA: CRC, 2002.
[2] G. C. Valley, "Photonic analog-to-digital converters," *Opt. Express*, vol. 15, no. 5, pp. 1955–1982, 2007.
[3] S. Srinivasan *et al.*, "Low phase noise hybrid silicon mode-locked lasers," *Front. Optoelectron.*, vol. 7, no. 3, pp. 265–276, 2014.
[4] K. Yvind, D. Larsson, L. J. Christiansen, J. Mørk, J. M. Hvam, and J. Hanberg, "High-performance 10 GHz all-active monolithic modelocked semiconductor lasers," *Electron. Lett.*, vol. 40, no. 12, pp. 1–2, 2004.
[5] K. Yvind *et al.*, "Low-jitter and high-power 40-GHz all-active mode-locked lasers," *IEEE Photon. Technol. Lett.*, vol. 16, no. 4, pp. 975–977, 2004.
[6] C. Gordón, R. Guzmán, V. Corral, X. Leijtens, and G. Carpintero, "On-chip colliding pulse mode-locked laser diode (OCCP-MLLD) using multimode interference reflectors," *Opt. Exp.*, vol. 23, no. 11, pp. 14666–14676, 2015.
[7] T. R. Clark, J. U. Kang, and R. D. Esman, "Performance of a time- and wavelength-interleaved photonic sampler for analog-digital conversion," *IEEE Photon. Technol. Lett.*, vol. 11, no. 9, pp. 1168–1170, Sep. 1999.

[8] G. Wu, S. Li, X. Li, and J. Chen, "18 wavelengths 83.9 Gs/s optical sampling clock for photonic A/D converters," *Opt. Exp.*, vol. 18, no. 20, pp. 21162–21168, 2010.

[9] M. P. Fok, K. L. Lee and C. Shu, "4 × 2.5 GHz repetitive photonic sampler for high-speed analog-to-digital signal conversion," *IEEE Photon. Technol. Lett.*, vol. 16, no. 3, pp. 876–878, Mar. 2004.

[10] M. Mielke, G. A. Alphonse, and P. J. Delfyett, "168 channels × 6 GHz from a multiwavelength mode-locked semiconductor laser," *IEEE Photon. Technol. Lett.*, vol. 15, no. 4, pp. 501–503, Apr. 2003.

[11] R. Nagarajan *et al.*, "Large-scale photonic integrated circuits," *IEEE J. Sel. Topics Quantum Electron.*, vol. 11, no. 1, pp. 50–65, Jan./Feb. 2005.

[12] L. Hou, M. Haji, B. Qiu, and A. C. Bryce, "Mode-locked laser array monolithically integrated with MMI combiner, SOA, and EA modulator," *IEEE Photon. Technol. Lett.*, vol. 23, no. 15, pp. 1064–1066, Aug. 2011.

[13] S. Liu *et al.*, "AWG-based monolithic 4 × 12 GHz multichannel harmonically mode-locked laser," *IEEE Photon. Technol. Lett.*, vol. 28, no. 3, pp. 241–244, Feb. 2016.

[14] S. Liu *et al.*, "Synchronized 4 × 12 GHz hybrid harmonically mode-locked semiconductor laser based on AWG," *Opt. Exp.*, vol. 24, no. 9, pp. 9734–9740, 2016.

[15] Y. Tohmori, X. Jiang, S. Arai, F. Koyama, and Y. Suenatsu, "Novel structure GaInAsP/InP 1.5-1.6 μm bundle integrated-guide (BIG) distributed Bragg reflector laser," *Jpn. J. Appl. Phys.*, vol. 24, no. 6, pp. L399–L401, Jun. 1985.

[16] Y. Barbarin *et al.*, "Realization and modeling of a 27-GHz integrated passively mode-locked ring laser," *IEEE Photon. Technol. Lett.*, vol. 17, no. 11, pp. 2277–2279, Nov. 2005.

[17] X. Zhang,, S. Liu, D. Lu, R. Zhang and C. Ji, "Design and fabrication of a 400 GHz InP-based arrayed waveguide grating with flattened spectral response," *Chin. Phys. Lett.*, vol. 32, no. 5, 2015, Art. no. 054202.

[18] P. T. Ho, "Phase and amplitude fluctuations in a mode-locked laser," *IEEE J. Quantum Electron.*, vol. 21, no. 11, pp. 1806–1813, Nov. 1985.

[19] D. J. Derickson, R. J. Helkey, A. Mar, J. R. Karin, J. G. Wasserbauer, and J. E. Bowers, "Short pulse generation using multisegment mode-locked semiconductor lasers," *IEEE J. Quantum Electron.*, vol. 28, no. 10, pp. 2186–2202, Oct. 1992.

[20] R. Trebino, *Frequency Resolved Optical Gating: The Measurement of Ultrashort Laser Pulses*, Boston, MA, USA: Kluwer, 2002.

[21] C. Ji *et al.*, "Synchronized transform-limited operation of 10-GHz colliding pulse mode-locked laser," *IEEE Photon. Technol. Lett.*, vol. 18, no. 4, pp. 625–627, Feb. 2006.