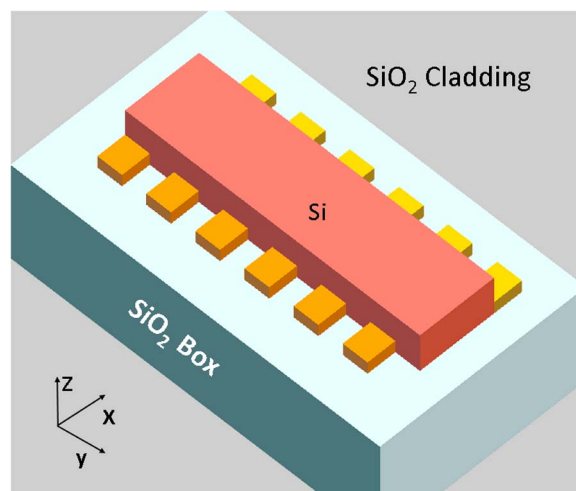


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Volume 8, Number 1, February 2016

Yao Sun
Yule Xiong
Winnie N. Ye



DOI: 10.1109/JPHOT.2015.2511080
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Yao Sun, Yule Xiong, and Winnie N. Ye

Silicon Macro/Nano Photonics Group, Carleton University, Ottawa, ON K1S 5B6, Canada

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Manuscript received October 20, 2015; revised December 11, 2015; accepted December 16, 2015.
Date of publication December 22, 2015; date of current version January 13, 2016. Corresponding author: Y. Sun (e-mail: yaosun@cmail.carleton.ca).

Abstract: We demonstrate the design and experimental results of a silicon-on insulator (SOI) polarization rotator design based on asymmetric periodically loaded waveguides. The rotator design features a compact device footprint of $15.78 \mu\text{m}$, with a measured polarization rotation extinction ratio of 11.8 dB at 1525 nm while maintaining at least 6 dB ER over the entire C-band. The fabrication of this rotator is fully compatible with the standard complementary metal-oxide semiconductor (CMOS) process with a SiO_2 top cladding. So far, this is the most compact polarization rotator demonstration utilizing the asymmetric periodically loaded SOI waveguides. However, the device is sensitive to fabrication errors; thus, the performance is limited by the current fabrication technology.

Index Terms: Silicon waveguide, polarization rotation.

1. Introduction

Silicon-on-insulator (SOI) technology is a promising platform for photonic applications with low-cost and large volume production due to its compatibility with the complementary metal-oxide semiconductor (CMOS) process. With public accessible CMOS foundries and multi-project wafer (MPW) runs, SOI based photonics integrated circuits (PICs) can be realized at an affordable cost [1]. However, the high index-contrast between silicon and the top cladding (SiO_2 or air) of the SOI waveguides leads to considerable polarization birefringence. Consequently, SOI based PICs are in general highly polarization-sensitive, making polarization management a necessity. One solution to manage the polarization on chip is the polarization-diversity approach, where polarization beam splitters (PBS) and polarization rotators (PRs) are the key elements [2]. A PBS first separates the input light into two orthogonally polarized beams, while a PR rotates the polarization state of one beam into its orthogonal counterpart (TM to TE, or *vice versa*), thus maintaining one polarization state throughout the signal processing circuit. After independently processing these two signals of the identical polarization state, a second PR is then used for the second beam to rotate the polarization state and to compensate for the loss incurred in the first PR. The two orthogonal beams will finally be recombined by a second PBS.

Polarization rotation (PR) on the SOI platform has been demonstrated in various configurations, including twisted waveguides [3]–[5], angled walls [6], [7], cut-corner structure [8]–[10], subwavelength trenches [11], or with help of an over-layer of different materials such as polycrystalline silicon or silicon-oxynitride [12], [13]. However, these devices either suffer from a large device footprint or multiple additional fabrication steps. Asymmetrical directional coupler

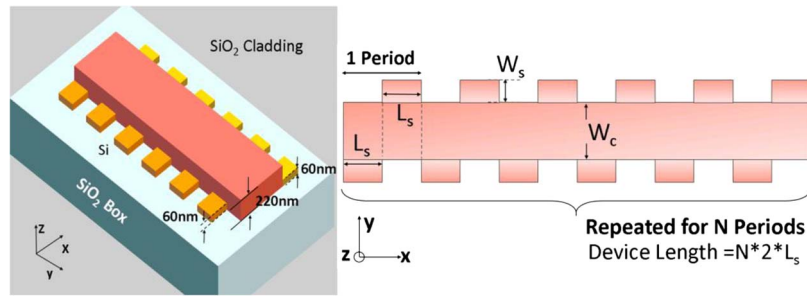


Fig. 1. Structure and top view of the proposed polarization rotator design.

based PR designs [14], [15] were reported to be simple to fabricate; however, the design is sensitive to width variations. Recently, plasmonic waveguide based PRs [16], [17] and waveguide bends based PRs have been proposed in order to minimize the rotation length for realizing ultra-compact sizes [18], [19]; however, no experimental results have been reported yet. Polarization splitter rotators (PSR) can be used to achieve polarization rotation; however, these structures in general have large footprint of a few hundred micrometers [20]–[22]. In addition, the PSR presented in [21] requires an air cladding to realize vertical asymmetry and thus is incompatible with most metal back end-of-line processes.

In 1991, a passive PR based on an asymmetrically periodic loaded waveguide was demonstrated by Shani *et al.* [23]. Although it has been proven that this structure can be used to obtain a highly efficient polarization rotation [23]–[27], the proposed designs range from 320 μm to 1225 μm in length and have only been demonstrated on III-V materials (GaAs, InP etc.). Our SOI-based PR is compact ($\sim 15.78 \mu\text{m}$) and can be fabricated by the standard CMOS process with a simple two-step lithography etching. The structure uses SiO_2 as the top cladding which enables the monolithic integration in SOI based PICs. The periodic structure enables flexible waveguide parameter selections. In recent studies, Bragg diffraction based PRs have been demonstrated in [7] and [10] resulting in wavelength selective ($\sim 1490 \text{ nm}$ in [7] and $\sim 1468 \text{ nm}$ [10]) devices with large footprints ($\sim 1000 \mu\text{m}$ in [7] and $308 \mu\text{m}$ in [10]). Compared to this work, by only utilizing the mode beating behavior in non-symmetric waveguides, our design achieves a much more compact ($15.78 \mu\text{m}$) device footprint and operates at a wider wavelengths range (1525 nm – 1540 nm). So far, this is the most compact polarization rotator demonstration utilizing the asymmetric periodic loaded SOI waveguides.

2. Structure Design and Operation Principle

The schematic of the proposed PR is illustrated in Fig. 1. It is a rib waveguide with longitudinally periodic perturbations (loadings) in the slab section of the waveguide, where the periodic loadings on left and right side are mismatched. As shown in Fig. 1, the width of the slab is W_s and each perturbed section has a slab length of L_s , while the width of the waveguide core is W_c . The structure is formed by repeating the alternation of the left and right slab perturbations for N periods. The device can be realized in a simple two-step etching process where one shallow etch is required to form the periodic loadings on either side of the slab, followed by one full etch to define the core.

The polarization conversion of our proposed PR design is based on the mode beating behavior and coupling between the periodic asymmetric sections. The physical principle of the PR is that the geometric mismatch introduced by the waveguide asymmetry is responsible for the cross-coupling between the two polarizations. The beat length L_b of the two polarized modes is defined as

$$L_b = \frac{\lambda}{\Delta n_{\text{eff}}} \quad (1)$$

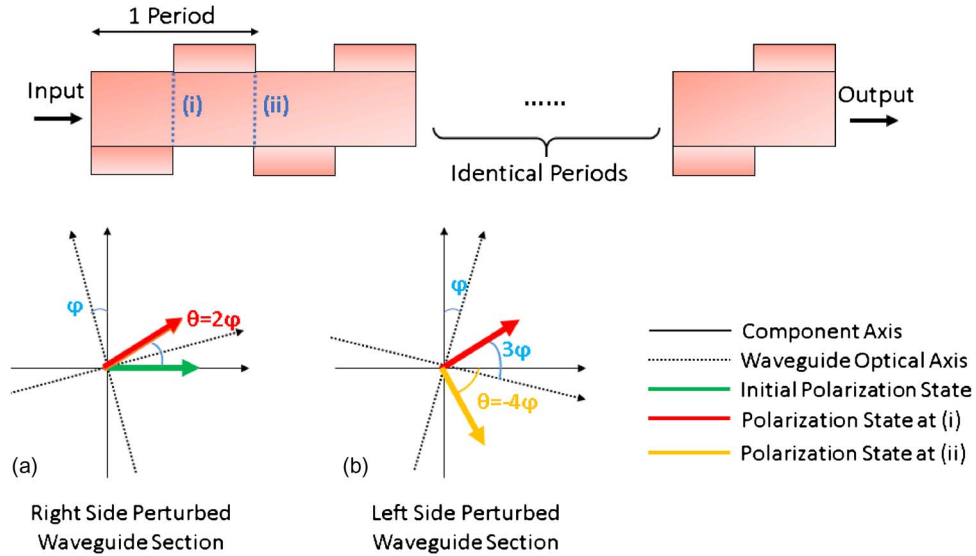


Fig. 2. Polarization rotation at the asymmetrical waveguide sections, where φ is the rotation angle with respect to the optical axis induced by the waveguide asymmetry, and θ is the rotation angle of the mode's polarization state.

where Δn_{eff} is the effective index difference between the TE and TM modes. The asymmetric waveguide cross-section of each mismatched segment introduces a rotation φ to the optical axis along the propagation direction. Here, a right side perturbed waveguide section will offer a $+\varphi$ rotation angle to the optical axis, while a $-\varphi$ will be obtained by a left side perturbed section. The rotation angle (φ) for the asymmetrical waveguide section can be calculated by following

$$\tan\varphi = \frac{n^2(x, y)E_y^2(x, y)dxdy}{n^2(x, y)E_x^2(x, y)dxdy} \quad [16] \quad (2)$$

where $n(x, y)$ is the refractive index distribution, and $E_x(x, y)$ and $E_y(x, y)$ represent the lateral and transverse electrical components of an eigenmode, respectively. When the length of a single perturbed section equals to an half of L_b , constructive interference between the two modes will occur, leading to a $+2\varphi$ rotation to the polarization state at the output of the waveguide. Fig. 2 shows an example of how the polarization state rotates in one full period of asymmetrical waveguide sections, where θ is the total rotation angle to the input. Assuming a TE-mode being launched at the left side, the polarization state of the mode at location (i) will be $\theta = +2\varphi$, given that the right perturbed waveguide offers a $+\varphi$ rotation to the optical axis [Fig. 2(a)]. As shown in Fig. 2(b), the mode has a 3φ rotation angle with respect to the optical axis of the left perturbed waveguide section, where a $-\varphi$ to the waveguide optical axis is induced by the waveguide asymmetry at location (i). The polarization state of the mode will be rotated by $-\varphi$ at location (ii). The final resulting mode has a $\theta = -4\varphi$ rotation angle, compared to the initial TE input.

In our design, the length of each perturbed section L_s is chosen to match to a half of L_b (i.e., $L_s = 0.5 * L_b$). Thus, after repeating N alternation of left side and right side perturbed sections, the polarization of the input mode will be rotated by an angle θ after N periods, where

$$\theta = (-1)^N 4N\varphi. \quad (3)$$

This analysis is consistent with the explanation presented in [26] and [27], except here we introduce the concept of N identical periods. By phase matching between the two orthogonal modes of the asymmetric loaded waveguide, polarization rotation of any angle can be achieved. Fig. 3 plots the rotation angle (θ) vs. number of periods (N). The chosen waveguide geometry in the demonstrated design introduces a 3.75° rotation in the waveguide optical axis ($\varphi = 3.75^\circ$). As

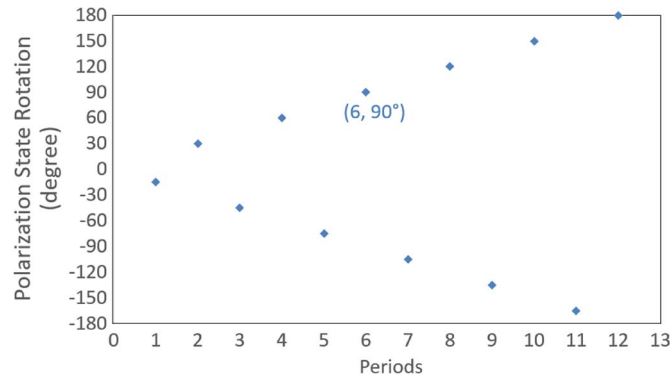


Fig. 3. Polarization state rotation (θ) vs. periods N .

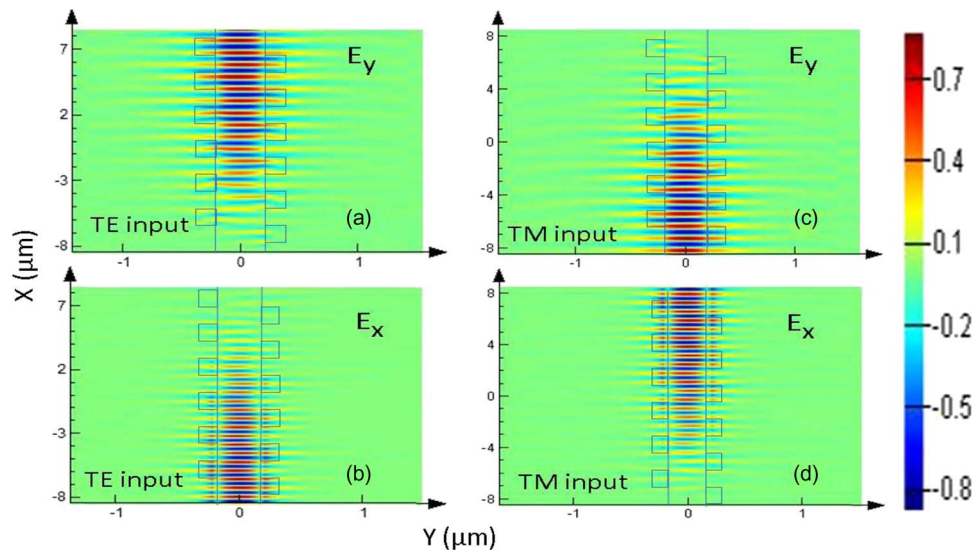


Fig. 4. Transverse electric field components E_x and E_y along the proposed polarization rotator design (top view) for TE [(a) and (b)] and TM [(c) and (d)] polarized inputs.

can be seen from the plot, the rotation angle of the polarization state accumulates after passing each pair of right side and left side perturbed waveguide sections. A full rotation ($\theta = 90^\circ$) is found at $N = 6$. The original polarization state will be restored ($\theta = 180^\circ$) when $N = 12$. This observation agrees with the operating principles of the demonstrated design.

Fig. 4(a)–(d) show the conversion of the E_x and E_y electrical field components of the waveguide mode calculated via a three-dimensional-finite-difference time-domain (3D-FDTD) method. Fig. 4(a) and (b) show that as the TE polarized input mode propagates along the device, the E_x component attenuates and ceases to exist at the output, while the E_y component appears and eventually dominates at the output. Similarly, for a TM polarized input mode, the polarization rotation phenomenon can be observed in Fig. 4(c) and (d): As the input mode is gradually rotated along propagation, the pre-dominant E_y component disappears, while the output shows the E_x component.

3. Parameter Optimization

The design optimization of the proposed PR structure is done using the eigenmode expansion (EME) method and cross-checked by the 3D-FDTD simulations. In our simulations, we focus on the C-band wavelengths from 1530 to 1565 nm with both the TE and TM input modes. The

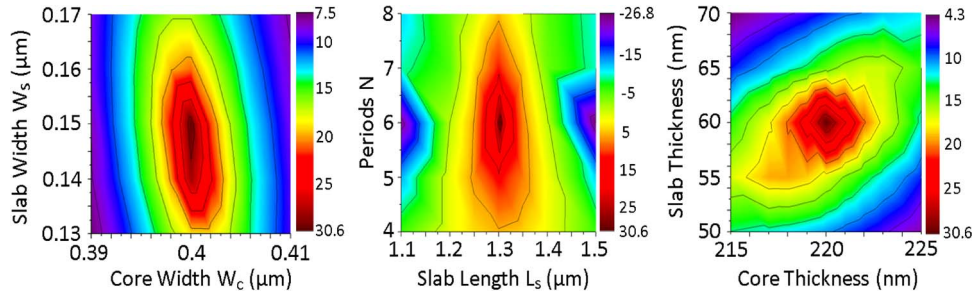


Fig. 5. Extinction Ratio (ER) as a function of waveguide core width (W_c) and slab width (W_s) combinations (left), Periods (N), and slab length (L_s) combinations (middle) and slab thickness and core thickness combinations (right) calculated by EME at 1550 nm wavelength.

TABLE 1

Summary of optimized geometrical parameters

Core Thickness (μm)	Slab Thickness (μm)	W_c (μm)	W_s (μm)	L_s (μm)	N	Device Length (μm)
0.22	0.06	0.4	0.15	1.315	6	15.78

refractive indexes of Si and the surrounding cladding are assumed to be $n_{\text{Si}} = 3.476$ and $n_{\text{SiO}_2} = 1.444$, respectively. Due to the availability of the foundry services standards (IMEC, for example), the thicknesses of the waveguide core and slab are chosen to be 220 nm and 60 nm, respectively.

Our design optimization involves maximizing the performance parameter Extinction Ratio (ER) of the proposed polarization rotator, where ER is defined as

$$\text{ER}_{(\text{TE-TM})} = 10 \log \frac{P_{\text{TE-TM}}}{P_{\text{TE-TE}}} \quad (4)$$

Here, $P_{\text{TE-TM}}$ is the power coupled to TM polarized mode at the output when the input polarization is TE, while $P_{\text{TE-TE}}$ is the residual power of the TE polarized mode left at the output. A positive ER means more than a half of the input mode's power is coupled to the orthogonally polarized mode at the output. Due to the operating principle of the proposed PR design, the TE-to-TM and TM-to-TE mode conversions are reciprocal.

For a given access waveguide height of 220 nm and the slab height of 60 nm, the rotator performance depends on the geometrical parameters W_c , W_s , L_s and the periods N . The initial parameters are found through simulations via FimmPROP. To optimize the core and slab width W_c and W_s , we fix $L_s = 1.315 \mu\text{m}$ and period $N = 6$. The left side of Fig. 5 shows the calculated ER as a function of W_c and W_s combinations. The best ER of 30.6 dB is found when $W_c = 0.4 \mu\text{m}$ and $W_s = 0.15 \mu\text{m}$. The chosen waveguide geometry will introduce a 3.75° rotation to the waveguide optical axis ($\varphi = 3.75^\circ$). The calculated ER is over 20 dB at 1550 nm wavelength for $W_c = 0.4 \mu\text{m} \sim \pm 0.003 \mu\text{m}$ and $W_s = 0.15 \mu\text{m} \pm 0.015 \mu\text{m}$. Next, we determine the optimal value of L_s and N by fixing $W_c = 0.4 \mu\text{m}$ and $W_s = 0.15 \mu\text{m}$. The middle part of Fig. 5 shows the ER as a function of N and L_s , where the best ER of 30.60 dB is found when $L_s = 1.315 \mu\text{m}$ and $N = 6$. The calculated ER is over 20 dB within the L_s range of $1.27 \mu\text{m}$ to $1.335 \mu\text{m}$ for $N = 6$. We then perform the fabrication tolerance analysis on slab thickness and core thickness. The right part of Fig. 5 presents the calculated ER as a function of slab thickness and core thickness combinations, with W_c , W_s , L_s , and N being fixed. The calculated ER is over 20 dB for a core thickness of $220 \text{ nm} \pm 2.5 \text{ nm}$ and for slab thickness of $60 \text{ nm} \pm 4 \text{ nm}$.

These analyses suggest that the PR design is sensitive to fabrication errors but works within reasonable fabrication deviations. A summary of optimized geometrical parameters is listed in Table 1.

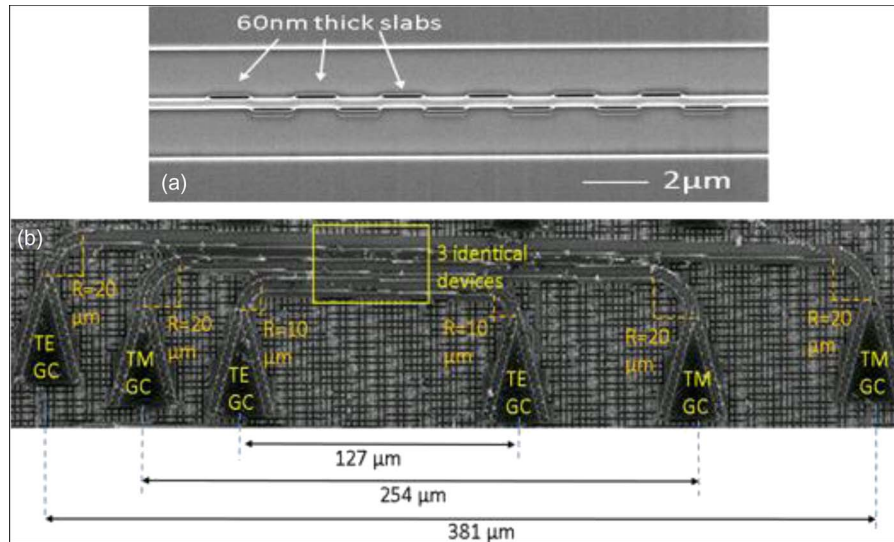


Fig. 6. (a) Topview of the fabricated device and (b) topview of the testing circuit for the fabricated design.

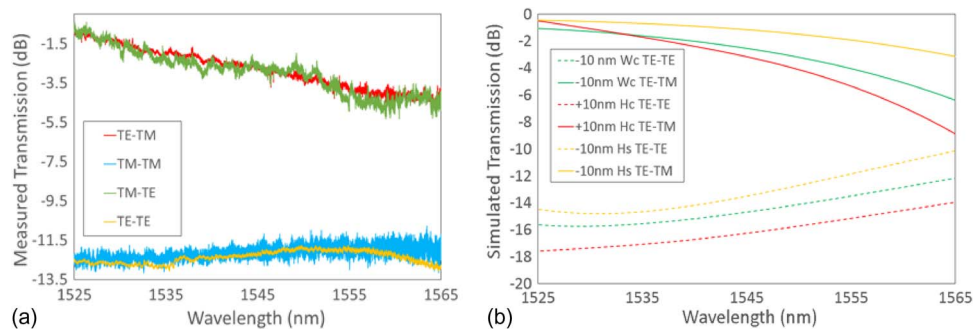


Fig. 7. Measured transmission spectra (a) and the simulated transmission spectra (b) considering fabrication deviations.

4. Fabrication and Experiment

The device was fabricated on a SOI wafer consisting of a 220 nm thick silicon layer with a 2 μm thick buried oxide layer. The fabrication was carried out using the 193 nm deep UV lithography by IMEC-ePIXfab and is completely CMOS compatible. A full etch is used to define the waveguide core and a shallow etch of 160 nm is used to fabricate the slabs.

Fig. 6(a) shows the scanning electron microscope (SEM) image of the topview of the fabricated device. Fig. 6(b) shows the SEM image of the testing circuit for this design, in which the grating couplers (GCs) are shown, along with the fabricated devices and dimensions. In the testing circuit, three identical devices were fabricated and connected to a pair of TE GCs, a pair of TM GCs and a pair consisting of 1 TE GC and 1 TM GC, respectively. A tunable laser covering a wavelength range of 1525–1580 nm is used to characterize the fabricated devices. The polarization of the input light source is calibrated by using an external polarization control paddle. The testing set-up is built using a six-channel polarization maintaining (PM) fiber array (FA) on an automated testing stage. The FA has three TE PM fibers and three TM PM fibers and is used for light injection and collection to and from the devices. An optical analyzer was used to perform the wavelength scans on the device.

The normalized measured transmission of the TE-TE, TE-TM, TM-TE, and TM-TM are presented in Fig. 7(a). We first estimated the insertion loss for the TE-TE and TM-TM coupling in

our reference waveguide circuits without PR structures, which includes system noise, the coupling loss of the GCs, and waveguide bending loss. The insertion loss (IL) of the PR itself is measured to be ~ 1.1 dB at the peak wavelength (1525 nm wavelength). Simulations show less than 0.5 dB loss for the device. We believe that the excess loss observed is mainly reflection loss and scattering loss. The slightly different performance in the TE-to-TM and TM-to-TE conversion is mainly due to the polarization dependent reflection/scattering loss. In addition, the exact optimized dimensions (W_c , W_s , H_c , H_s) are difficult to realize in fabrication.

By taking the fabrication tolerance into account, Fig. 7(b) shows the simulated transmission spectra over the operating wavelengths. The simulated transmission spectra demonstrate a similar trend as the measured data in Fig. 7(a). The transmission performance is wavelength dependent mainly due to the fact that L_s is wavelength sensitive [see (1)]. In addition, the grating couplers used for coupling in and out of the devices are also wavelength sensitive.

In simulations, we have predicted that the peak ER is at ~ 1550 nm wavelength for both the TE-TM and TM-TE conversion, and ER is over 10 dB covering the C-band wavelengths. Experimentally, the ER is over 8 dB for wavelengths range of 1525 nm to 1553 nm and is over 6 dB covering the entire C-band wavelengths for both TE-TM and TM-TE conversion. The peak ER is 11.8 dB at wavelength of ~ 1525 nm. By further investigation on the differences between the experimental and simulation results, we identified the three most critical design parameters are W_c , H_c , and H_s . It is clearly illustrated in Fig. 7(b) that the dimension deviations can result in peak wavelengths shifts and performance degradation. We believe the dimension deviations of these parameters in the fabricated devices are the main reason for the observed performance degradation. Moreover, the sidewall roughness and rounded corners [as can be seen in Fig. 7(a)] will further degrade the device performance. Compared to works demonstrated in [23]–[26], we have reduced the device footprint by 99.57% with CMOS compatible fabrication steps available in the standard foundry services. However, the device is sensitive to fabrication deviations; thus, the demonstrated PR performance is limited by the current fabrication technology.

5. Conclusion

In the paper, we have proposed and experimentally demonstrated a PR design based on asymmetrically periodic loaded structures on the standard 220 nm SOI technology platform. The fabricated device achieves a maximum polarization rotation extinction ratio of 11.8 dB with a compact device of 15.78 μm , while maintaining at least 6 dB extinction ratio across the entire C-band. The fabrication of this device is fully CMOS compatible, via a simple two-step etching process. Furthermore, we believe this work opens a new prospect of flexible, compact, and high efficient polarization rotator design on the SOI platform.

Acknowledgment

The authors would like to thank CMC Microsystems and the NSERC-SiEPIC program for their support in fabrication, which was done at the IMEC-ePIXfab; CMC Microsystems for providing access to the simulation and design software; and Schulz, R. Vandusen, and J. Upham for taking the SEM images.

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