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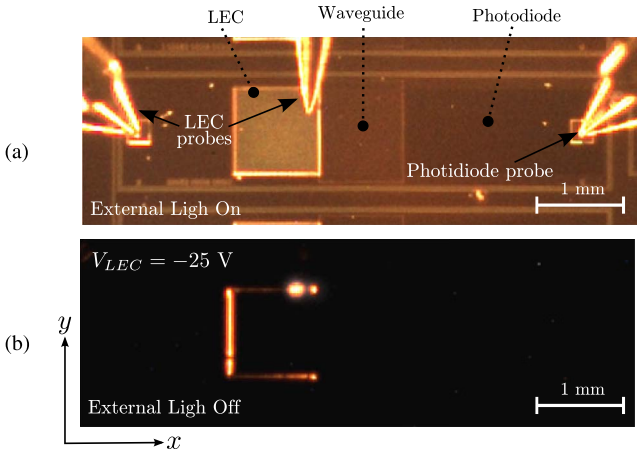

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Monolithic Integration of a Silicon-Based Photonic Transceiver in a CMOS Process

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Abstract: This work presents the design, fabrication, and characterization of a monolithic and complementary-metal–oxide–semiconductor (CMOS)-based integrated optical system, including the light emitter working in the visible range, waveguide, and photodetector. The presented system aims to be applied for the development of optochemical sensors. The work presents the proposed concept and the integration strategy, as well as the fabrication process. The individual elements of the system are theoretically evaluated to assure compatibility among them. Then, the fabrication and studies to the complete system are presented. The response of the light sensor is shown to be caused by optical stimulation of light originated in the integrated light source and transmitted through a dielectric waveguide, thus validating the integration procedure.

Index Terms: Integrated photonic systems, electro-optical systems, sensors, optoelectronic materials.

1. Introduction

Among the different types of existing chemical sensors, those based on optical transducers have received much attention due to their intrinsic advantages, such as the capability to do measurements without mechanical contact to the samples (based on free space propagation of light), higher sensitivities, and very low limits of detection, all of which are important issues for biosensing devices [1].

Chemical analyses based on waveguide or fiber optic sensing schemes have matured around the development of optical communications technology. Thus, in order to reduce costs and address mass-applications, silicon-based optical integrated transducers have evolved to cover the market needs.

The main optical components of an integrated sensor system are the light source, the waveguide (acting as propagation line and transducer), and the photo-detector, as the acquiring signal

element. Up until now, the main drawback to obtain a monolithically integrated opto-chemical sensor has been the difficulties in the direct integration of the light source. A solution to this problem would make possible the elimination of alignment problems, the improvement of portability, and the production of multiple sensor arrays.

In addition, all silicon based integrated optical systems fabricated using standard substrates and CMOS technology would allow to fully exploit the advantages of Si microelectronics directly coupled to optics, with a vast quantity of potential applications in the fields of chemical and biochemical analysis; such as light-based characterization lab-on-chips that would integrate the electronics and the measuring systems. Key parameters of this integrated optical systems would be the intensity delivered by the optical source, its stability, and the wavelength range that can be emitted. Data transmission rates, a key figure in communications transceivers, would not be necessarily important for chemical and biochemical sensing applications.

The first approaches to obtain monolithically integrated interferometers based in semiconductors were developed in GaAs [2] due to its suitability for optical applications. Nevertheless, the field of silicon photonics has experienced significant progress in the past years because of its CMOS compatibility. Most photonic components have been demonstrated in Si, including detectors, light sources [3], [4], electro-optic modulators, and waveguides [5]–[7]. However, while there are several demonstrations of the isolated elements needed for the obtainment of an all Si-based, CMOS compatible transmitter-receiver (or transceiver) system able to act as an integrated chemo-optical sensor, the main challenge remains the obtainment of a monolithically integrated system with all the elements in a single silicon chip.

In order to achieve such system, an efficient optical coupling between the light source and the transducers would be required. Different approaches have been proposed to solve this, including the use of coupling elements such as diffraction gratings [8] or the use of silicon avalanche diodes as the light source [9]–[11]. The first approach uses monochromatic light, constraining the range of applications suitable for sensor arrays. On the other hand, the avalanche diode produces a wider spectrum but delivers lower intensities, and the insertion to the waveguide is a challenge due to its off-plane emission nature.

Another scheme that has been tested in order to integrate light sources has been the development of electroluminescent devices consisting of nanostructures obtained by doping with rare earths dielectric layers used in CMOS technology, like silicon nitride or silicon oxide [12]. The use of nanostructured materials opens the possibility to increase the efficiency of the developed light sources [13] and allows for modulation of the emitted radiation [14] the latter being an important issue for sensor arrays with individual specific detection.

In this work, we demonstrate the monolithic integration of a nanostructured silicon based light source, a Si_3N_4 waveguide with SiO_2 cladding, and a silicon photodiode, all fabricated on a bulk silicon substrate using standard CMOS processes, precursors, and facilities. The problem of the sub-cladding for the waveguide was solved using a Local Oxidation of Silicon (LOCOS) process to obtain a buried Si oxide, avoiding the use of silicon on insulator (SOI), and allowing the self-aligning of the emitting sources to obtain a direct light insertion, taking advantage of a recently developed nanolayered light emitting device reported in [15], which is composed exclusively by silicon, oxygen, and nitrogen.

The integration strategy is presented, and the challenges involved in the fabrication of the devices will be discussed along with the results of their characterization. This is the first report of an electro-optical system including a light source directly aligned to the waveguide in a same plane and obtained using all Si-based materials and a fully compatible CMOS fabrication process without post processing, epitaxial growth of non Si-based materials, or use of rare earths. This opens the door to obtain sensing systems seamlessly integrated with driving electronics, and fabricated at much lower costs, due to the availability of the materials and the possibility of large scale mass production.

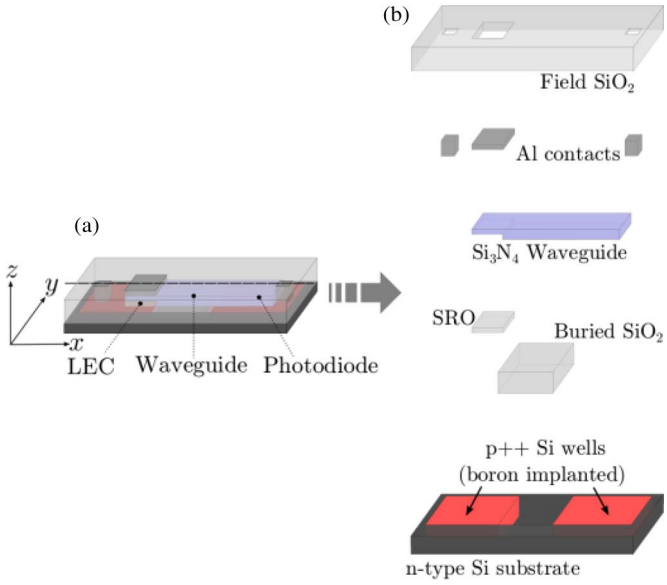

Fig. 1. Scheme and materials used in the planar configuration of the transceiver prototype (not to scale). (a) General layout and (b) breakdown of the structure.

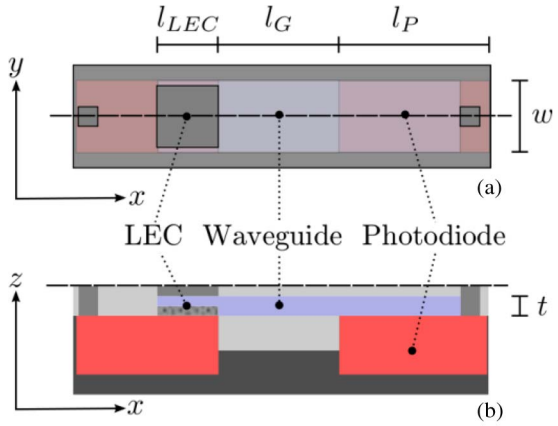

Fig. 2. (a) Top view and (b) transverse cut of the proposed architecture for the transceiver prototype (not on scale).

2. Experimental Details

2.1. General Concept and Integration Strategy

In order to achieve maximum compatibility to standard CMOS processes, the Integrated Optical System (IOS) must be conceived as fabricated by planar technology, avoiding the use of non-standard materials and techniques. Fig. 1 presents a 3-D representation of the proposed device and the materials in the stack structure, and Fig. 2 presents a top view and transverse cut of the proposed architecture.

In this scheme, the left part of the system consist of a nanolayered light emitting capacitor (LEC) made of a 30 nm-thick Si_3N_4 film on top of a 30 nm-thick Silicon Rich Silicon Dioxide (SRO) film, such as that introduced and reported in detail in [15]. The latter is directly embedded in a rectangular cross-section silicon nitride waveguide, which transmits the emitted light to the detector. Such waveguide can be obtained during the same step of the nitride layer deposition

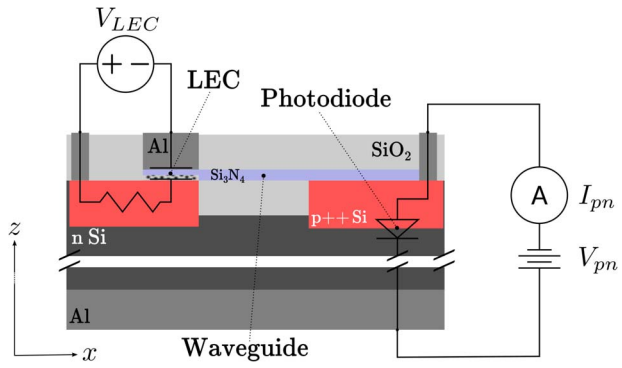

Fig. 3. Symbolic schematic of the electrical connections and devices embedded in the transversal cut of the transceiver as represented in Fig. 2(b).

for the bi-layer devices described in [15]. The guide cannot be directly deposited on the Si substrate, as the latter has a higher refractive index than the nitride. Instead, silicon dioxide is an appropriate material for the cladding of the waveguide, as long as its thickness is enough to prevent the electric field of the light reaching the substrate. However, a thick enough SiO_2 film cannot be simply deposited on the substrate, since it would isolate the bottom contact of the LEC if it is done in the whole wafer. Even if such film is patterned to remain only below the waveguide, it would misalign the center of the waveguide and the SRO-Si_3N_4 interface, in which a great part of the light is generated in such interface. Then, the proposed solution is to bury a SiO_2 well exactly below the waveguide, which can be obtained by silicon etching and LOCOS: a standard technique widely used in the fabrication of integrated circuits [16], [17].

The waveguide transmits the light from the LEC to a p-n junction photodiode placed below its end. The higher refractive index of the silicon substrate allows the evanescent coupling that generates the electron-hole pairs (e-h) to be detected as photocurrent in the terminals of the photodiode.

Two regions doped with opposite carrier type and degenerated concentration are implanted to electrically isolate the emitter from the sensor. One allows the electrical access the bottom terminal of the LEC. The other is the anode of the photodiode, while the back of the wafer is its cathode (or the other way around, depending of the substrate type). Then, the voltage of the signal to transmit V_{LEC} can be applied to the emitting device from the top of the wafer, while the transmitted information will be read through the current in the p-n junction I_{pn} using terminals in the top and the back of the wafer, as the electric schematic in Fig. 3 depicts. In this configuration, the p++ well used to connect the bottom terminal of the LEC forms a natural depletion region which electrically isolates this device from the rest of the wafer, hence, the emitter and the photodiode.

2.2. Design and Fabrication

In the following sections the components developed to build up the transceiver will be defined, and its viability verified. As mentioned, the main advantage of this approach is its CMOS compatibility and possibility to integrate. Because of the monolithic nature of the approach, the limitations of each element are not defined as those of an equivalent single standing emitter, waveguide, and detector, but as how the whole system would perform. Then, each element is evaluated as a function of the possibility of working in the whole system, as opposed to as a discrete element.

2.2.1. Emitter-Waveguide

Details on the characteristics, and results from studies of efficiency, reliability, and emission spectra of the latest fabricated LECs, are reported in [15] and [18]. For this work, the used

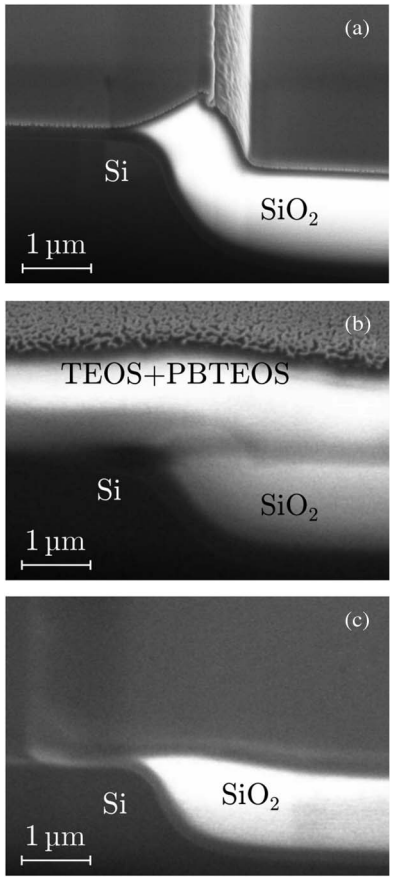

Fig. 4. Images of a transverse cut of the wafers in the lower cladding region obtained by FIB and TEM. Three steps are shown. The result (a) after LOCOS, (b) after the deposition and fluidification of the TEOS + BPTEOS film, and (c) after the dry etching of the former to obtain a cladding leveled to the Si substrate surface.

configuration and characteristics were those which showed the highest efficiency according to the mentioned publications, and this ruled the fabrication parameters of the IOS.

As mentioned, the emitter will be embedded in the waveguide. This way, assuming that the emission from the active material is isotropic, most of the part in the positive *x* direction as defined in Fig. 2 can be transmitted, and the emission in the rest of the directions within the critic angle can also contribute.

The lower cladding of the waveguide formed by the buried silicon dioxide presents a technological challenge, since it must be in the same level as the wafer surface in order to allow the waveguide to rest on top of the photodiode, while avoiding surface topography that may increase the propagation losses of the structure [see Fig. 2(b)]. Our approach solves this using a LOCOS process, which consists on the local growth of thermal silicon dioxide in a previously etched trench [16]. This technique presents a feature known as the bird's beak phenomenon [17], which introduces a perturbation in the transition from the dioxide well to the Si wafer. This can be observed in Fig. 4(a), which shows the result of the LOCOS in one test sample as observed with Scanning Electron Microscope (SEM) on a transverse cut obtained with a Focused Ion Beam (FIB).

Such perturbation is important in the case of the design here presented, since it may reduce significantly the light transmission efficiency. The solution proposed to minimize this effect is a process consisting on the deposition of successive films of tetraethyl orthosilicate film (TEOS) and boron phosphorous tetraethyl orthosilicate (BPTEOS), a thermal fluidification annealing to

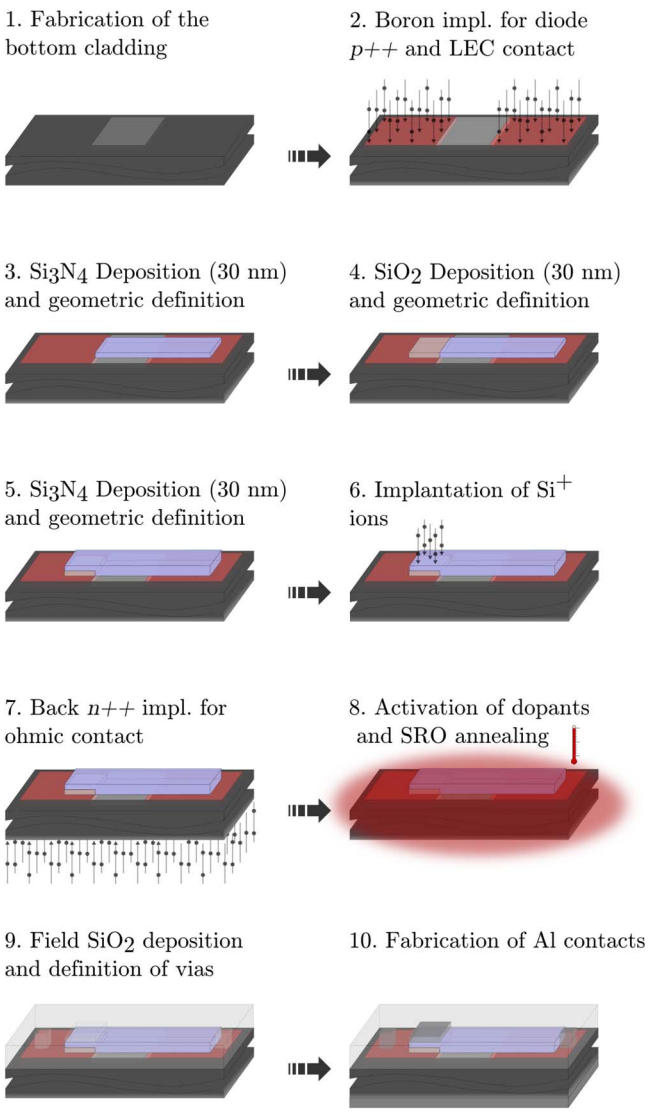

Fig. 5. Summarized fabrication process of the integrated optical system.

homogenize the surface, and a further dry etching of the silicate films to level it all to the original silicon substrate. Images for these two latter steps are presented in Fig. 4(b) and (c). As it can be observed, the final result is a planarized surface in which the top of the buried SiO_2 zone is at the level of the Si wafer surface.

While the SRO in the LECs previously developed was obtained by Si implantation in thermal SiO_2 [15], [18], in this case it is more convenient to use PECVD for its deposition, since this process does not need the thermal growth of oxide in the whole substrate. Otherwise, the processes for the dopant implantation to obtain the lower contact of the LEC, as well as the obtaining of the buried oxide would complicate significantly. The fabrication and characterization of a test run containing stand-alone LECs confirmed that the use of PECVD instead of thermal growth for the dioxide matrix does not change the device behavior.

The fabrication flow of the device is summarized in Fig. 5. After the lower cladding was obtained and the contact and photodiode p++ type Si wells were implanted, the fabrication continued with the deposition and the geometric definition by photo lithography of a 30 nm-thick silicon nitride film on top of the buried-dioxide cladding; it was then followed by the deposition of

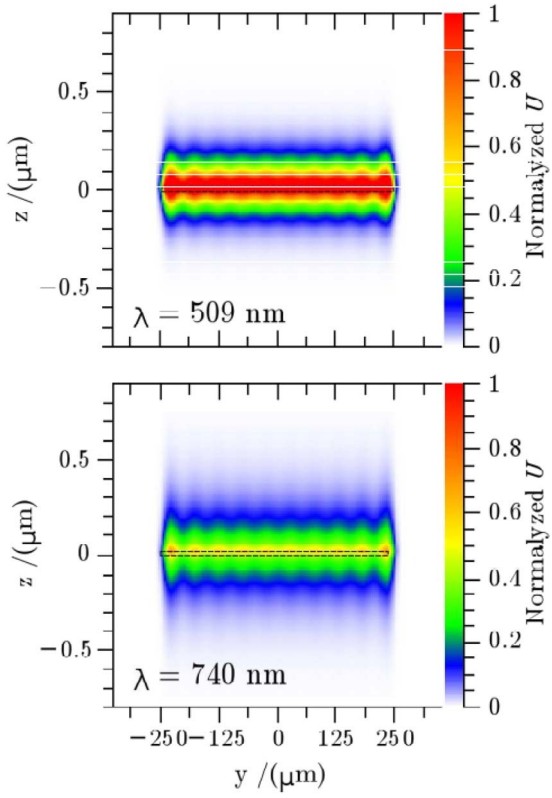

Fig. 6. Energy density profile of the propagated light for the first 20 modes of a specific wavelength in a transversal cut of the 60-nm-thick waveguide at $x = 500$ μm. The rectangle with discontinuous lines represents the interface between the Si_3N_4 waveguide and the SiO_2 cladding.

the matrix PECVD SiO_2 to form one layer of the LEC and the successive deposit of the other 30 nm of silicon nitride, for both the nitride layer of the LEC, and the rest of the waveguide. Finally, the Si implantation in the bi-layer region and the further thermal treatments needed for the generation of Si agglomerates in the SRO were performed [15].

Note that in the process here presented, the thickness of the waveguide t is defined by that of the emitter, which on its turn is limited by the voltage needed to obtain sufficient EL intensity. This is a potential limiting factor for the waveguide, and the simulation of its capability for transmitting light becomes relevant for this reason. For the here presented configuration, the waveguide will have a thickness $t = 60$ nm, as dictated by the used LEC [15].

In order to test the ability of the waveguides to transmit light under these limitations, simulations of the propagation modes were performed using the software FIMMWAVE. In [15] it is showed that the intrinsic EL spectrum is composed by two bands with respective peaks in 509 nm and 740 nm. Therefore, the simulations were performed for these two wavelengths. The light energy density U was evaluated for the first 20 transmitted modes found at the beginning of the waveguide, and at 500 μm in the x direction, assuming direct injection and defining a window with the same dimensions of the LEC cross-section, aligned to the bottom of the waveguide.

Fig. 6 presents the results for the distribution of the optical energy density propagated at the length $x = 500$ μm in a waveguide with $w = 500$ μm for the two main emission wavelengths. No significant differences in the values at $x = 0$ μm were found.

The simulations confirmed that only modes purely composed by E_y can propagate. This is due to the low or similar values for t (the dimension in z, see Fig. 2), as compared to the light wavelength. Nevertheless, light can still be transmitted in the emission wavelengths, which are

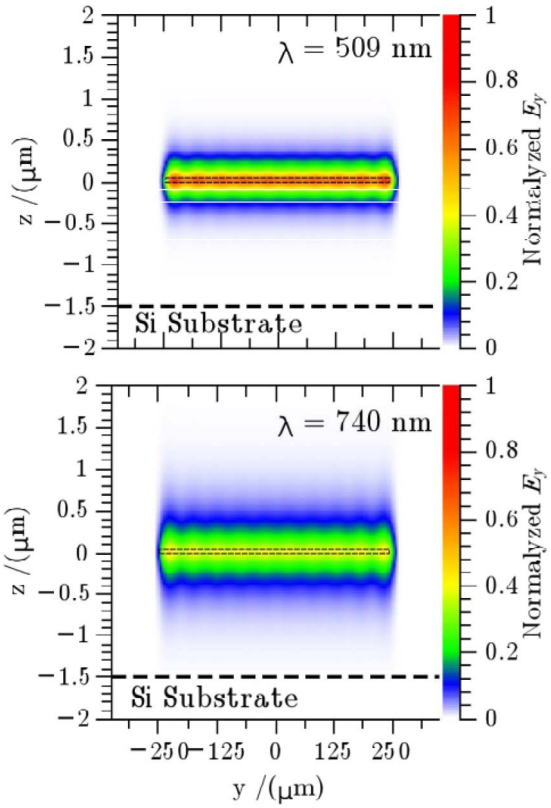

Fig. 7. Profile of the electric field component E_y for $\lambda = 509$ nm and $\lambda = 740$ nm at the length $x = 500$ μm. The discontinuous line at $z = -1.5$ μm represents the interface between the buried SiO_2 cladding and the Si substrate. The dotted rectangle represents the transverse cut of the 60-nm-thick nitride waveguide.

well suited for the detection by the Si photodiode, since its quantum efficiency is expected to be above 70% for wavelengths around 550 nm [16].

The cladding SiO_2 was designed to be 1.5 μm thick at its minimum. The electric field simulations for the E_y components evaluation at $x = 500$ μm are presented in Fig. 7. No important differences were observed when evaluating at $x = 0$ μm. The results show that 1.5 μm-thick buried cladding is sufficient to prevent the field reaching the Si substrate at $\lambda = 509$ nm, but in the case of $\lambda = 740$ nm, while the electric field value is low, it is not null, meaning that longer wavelengths need a larger cladding thickness.

2.2.2. Light Detector: Silicon Photodiode

The p-n junction proposed as detector is a simple, widely used, and compatible device. In addition, the reported quantum efficiency peak for Si photodiodes is between 600 nm and 1000 nm [16], which is in the range of the intrinsic emission of the materials here used [15]. The sensor can be obtained inverting the carrier type of the substrate in the desired region by the implantation of dopant elements, i.e., Boron if the substrate is *n*-type, or Phosphorous if it is *p*-type. In this case, since the thermal treatment restricted by the LEC fabrication, the insertion and activation of the dopants must be as controllable as possible. Then, it was decided to use an n-type substrate for the fabrication of the systems, as Boron is a better controlled element regarding its diffusion and reaction with Si than Phosphorous [19].

The electric access to the anode of the diode is a contact in the top of the wafer, while the cathode can be accessed using the back, as depicted in the electrical scheme of the system presented in Fig. 3.

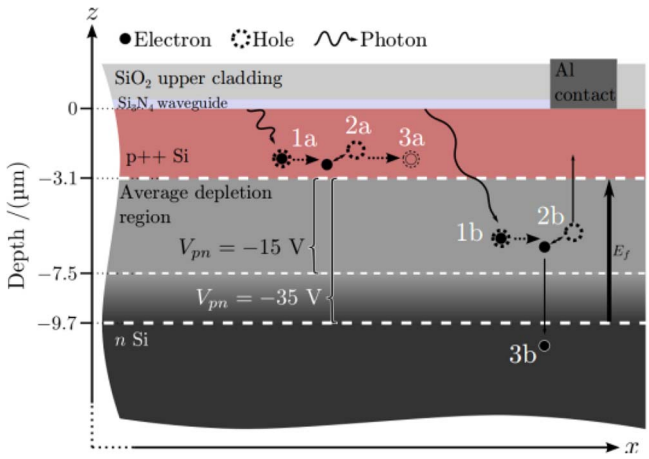

Fig. 8. Average depletion regions of the photodiode at Vpn $= -15$ V and Vpn $= -35$ V and depiction of photogeneration of e-h pairs that will recombine and not contribute to photocurrent (1a, 2a, and 3a) and, conversely, will be separated and contribute to photocurrent (1b, 2b, and 3b).

The back of the wafer received an n++ implantation, Al deposition, and the standard treatments to form an ohmic contact (see Fig. 5). Simulations with SRIM and ICECREM [20] were used to verify the results of dopant distributions for the necessary thermal treatments after implantation of Boron in the used substrates, which had an average resistivity of $(1.98 \pm 0.02)\ \Omega \times$ cm. As the implanted zone is degenerated because of its simultaneous fabrication with the bottom contact of the LEC, the junction is an abrupt one, and the depletion layer width Wd will mostly rely on the substrate. Its value can be calculated using the expression [16]

$$W_d = \sqrt{\frac{((2\varepsilon_s(V_{\text{bi}} - V))}{(qN_B)}} \tag{1}$$

in which ε_s is the silicon dielectric permittivity, N_B the doping concentration of the bulk Si, V the applied potential to the diode, and V_{bi} the built-in potential, which on its turn can be calculated with the equation

$$V_{\text{bi}} = \frac{kT}{q} \ln\left(\frac{(N_A N_B)}{(n_i^2)}\right) \tag{2}$$

where kT/q is the thermal voltage, N_A the acceptor concentration in the p region of the diode, and n_i the intrinsic carrier concentration of the Si.

Since the characteristics of the photo diode are tightly bound to the overall fabrication process of the transceiver, it is important to be aware of the value of the depletion layer position, as this is another potential limiting factor for the performance of the system, since if the light-induced e-h are generated outside this zone, they are likely to recombine again without contributing to the current, whereas if they are generated inside it, the electric field will separate the electron and the hole, and there will be a contribution to the current.

This process is illustrated in the Fig. 8, which also presents the average depletion layer behavior for different applied voltages V_{pn}, as calculated using the data obtained from the simulations.

According to the work by Green [21], the wavelengths shorter than 630 nm will be absorbed before reaching the depletion layer, even in the best-case scenario, in which it starts at $z = -2.9\ \mu$m.

The main emission wavelengths for the nitride and SRO related luminescence were found to be, respectively, centered 509 nm and 744 nm for the material selected for the fabrication of the IOS [18]. Then, only carriers generated by the band with longer wavelength peak will be

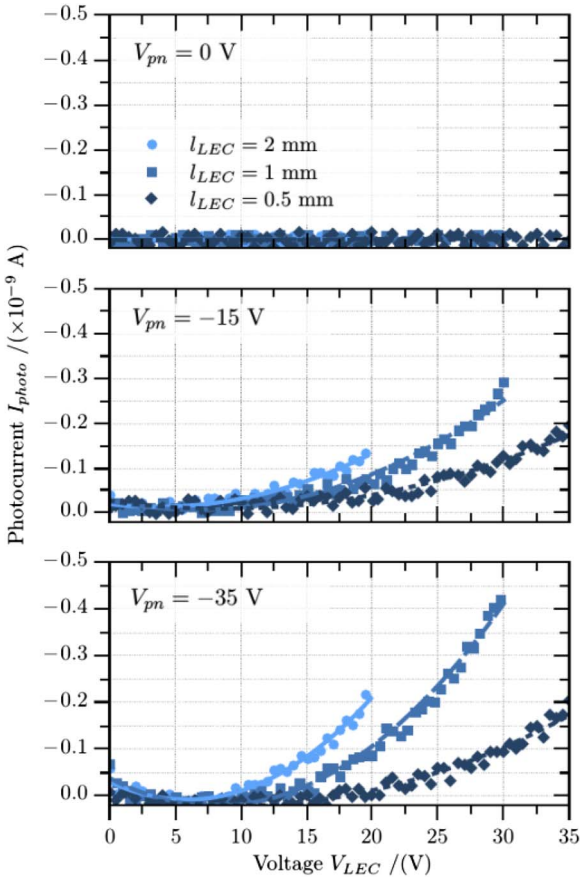

Fig. 9. Photocurrent detected in the photodiode I_{photo} versus voltage applied to the light-emitting device V_{LEC} for devices with side length $l_{LEC} = 2.0$ mm, $l_{LEC} = 1.0$ mm, and $l_{LEC} = 0.5$ mm. Data are presented for polarization voltages of $V_{pn} = 0$ V, $V_{pn} = -15$ V, and $V_{pn} = -35$ V.

significantly contributing to the current. While this is not fatal for the operation, it is not ideal, since the waveguide is better suited to transmit this part of the spectrum. This is an example of the possibility of improvement of this first approach.

On the other hand, the absorption depth for the light with wavelength of 744 nm is 7 μm [21], which means that part of these photons will likely surpass the depletion layer when absorbed. However, while in the present case the initial point of this region is fixed by the depth of the junction, W_d can be modified by the application of a voltage to the junction, as illustrated in the Fig. 8. In particular, a voltage of $V_{pn} = -35$ V would result in a depletion layer edge placed at an average maximum depth of -9.7 μm, which is enough to capture the carriers generated by the longer wavelengths.

The value of V can be varied to modulate W_d in order to sense a specific wavelengths range. This is particularly interesting in chemical sensing applications, providing high flexibility to the system.

3. Results

The transceivers were fabricated as schemed in the Figs. 1 and 2, with $l_{LEC} = w$ and three different l_{LEC} values, namely, 0.5 mm, 1.0 mm, and 2.0 mm. Fig. 9 shows the responses of the photocurrent detected in the photodiodes I_{photo} as the voltage applied to the emitting devices V_{LEC} is incremented. For each l_{LEC} fabricated, the results for three different photodiode polarization voltages are presented, namely, $V_{pn} = 0$ V, $V_{pn} = -15$ V, and $V_{pn} = -35$ V.

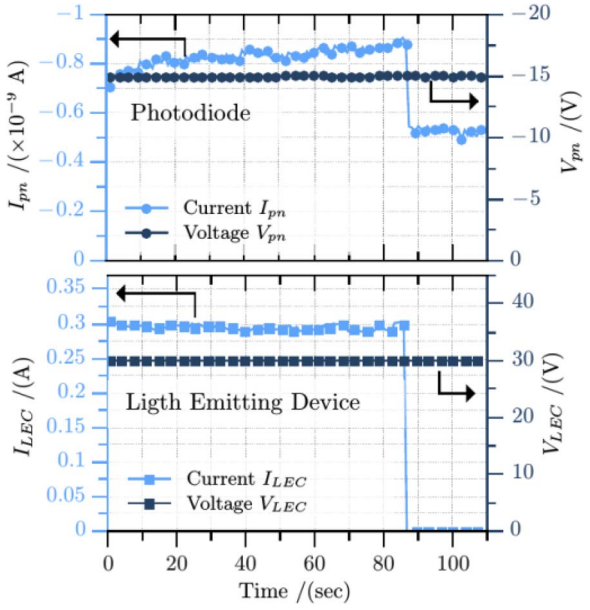

Fig. 10. Voltage and current in photodiode V_{pn} and I_{pn}, respectively, and voltage and current applied to the emitting device V_{LEC} and I_{LEC}, respectively; versus time of stimulation. The left axis corresponds to the values for the current data and the right axis to the values for the voltage data.

There is a clear response by the photocurrent to the stimulus of the LEC in all the cases in which the photodiode is reverse-biased. However, special attention must be paid to the possible responsibility of electronic cross talk in the readings, as it could significantly influence the signal, as opposed to only detecting the emitted and transmitted light. There are two possible ways in which the electric cross talk can occur: the leakage of current flowing to the back contact caused by the stimulus of the emitting device, and/or a modification in the effective voltage in the p-n junction.

In the first case, the leaked carriers would contribute to the detected current in the diode, causing increments or decrements in the value of I_{pn}. However, this should be independent of the polarization of the photodiode, meaning that the measurements when $V_{pn} = 0$ V would also be affected, which is not the case, as can be observed in the top plot of Fig. 9.

In general, the lack of variation in the readings when applying $V_{pn} = 0$ V regardless of the voltage and current in the emitter, is a very strong indication that the response in the photodiode does not come from electrical cross talk. On the contrary, it is consistent to the expected behavior for the light detection, since when no voltage is applied to the diode, the depletion width is not wide enough to capture the e-h pairs generated by the transmitted light.

Regarding the modification of the voltage relying on the junction by influence of V_{LEC}, the used source-meter prevents this from happening, since it is programmed to apply a particular voltage, while simultaneously measures and registers the real value in the device. The absence of modification in the junction voltage V_{pn} can be verified in Fig. 10, which presents the values along time of all the registered parameters: I_{pn}, V_{pn}, I_{LEC}, and V_{LEC}.

The plots in Fig. 10 present a particular case in which breakdown of the emitter was reached after applying a constant voltage $V_{LEC} = 30$ V for 130 seconds (it is important to point out that the device had already been tested in several ways, and the response shown in this figure is not representative of its lifetime or that of the systems in general). As it can be observed, the value V_{pn} remains constant at all times, regardless of the variations on the rest of the parameters, due to the action of the voltage source. It can also be observed how as soon as the current stops flowing through the LEC, the current registered along the diode drops to the dark condition

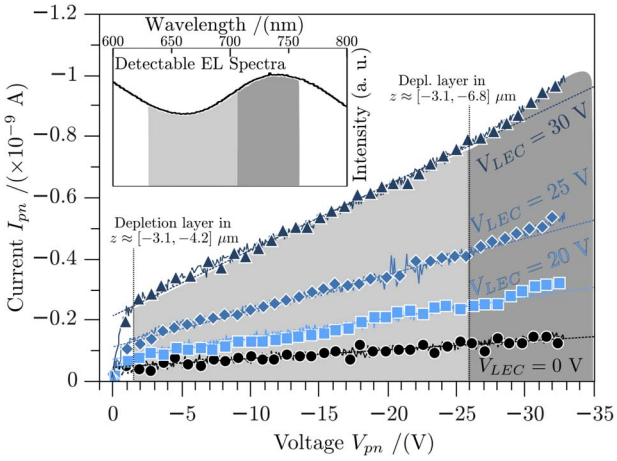

Fig. 11. Symbols: $I_{pn} - V_{pn}$ data for different V_{LEC} values. Dashed lines: linear fittings using the data between $V_{pn} = [-1.5, -26]$ V. Inset: Intrinsic light emission spectrum of the active materials in the LEC. The gray areas indicate each of the zones in which the emitted light is contributing to photo current.

value, because the LEC stops emitting light; hence, no more carriers are photo-generated in the detector.

Fig. 11, presents the I_{pn} vs. V_{pn} relation for reverse bias and different voltages applied to the emitter.

In the case of the curves in which the LEC is turned on $(V_{LEC} > 0$ V), three regions can be identified for its analysis: the first with V_{pn} between 0.0 V and –1.5 V, the second from –1.5 V to around –26.0 V, and the third with absolute voltage values above this. The regions are delimited in the figure by vertical dashed lines.

In the first zone of the plot (V_{pn} between 0 V and –1.5 V), the depletion region is between 3.1 μm and 4.2 μm-deep from the surface of the substrate, which is not wide enough to capture a significant amount of carriers generated by the arriving photons. As the diode bias voltage is increased, the depletion layer becomes wider, and more carriers can be captured to contribute to the current. When the second region of the plot is reached (light gray zone in Fig. 11, V_{pn} between –1.5 V and –26.0 V), the wavelengths between 630 nm and 705 nm generate carriers well within the depletion layer [21], and as its width is constantly increased by the increment of $-V_{pn}$, the value of $-I_{pn}$ increases linearly until around $V_{pn} = -26$ V.

Around this point, a third region is identified (dark gray zone in Fig. 11), in which the depletion layer is wide enough as to capture carriers generated by light with wavelengths longer than 705 nm [21]. Examining the intrinsic spectrum of the active layers extensively analyzed in [15] and [18], and presented here in the inset of Fig. 11, it can be observed that the light source has an emission peak around the 720 nm. The possibility of capturing the carriers generated by this emission translates into a change of the rate at which the current increases in the $I_{pn} - V_{pn}$ relation. This causes the separation between the linear projections and the experimental points after $V_{pn} = -26$ V that can be observed in the dark gray zone of Fig. 11.

The concordance between the known characteristics of the emitted light, and the modification of the I_{pn} response when changing the bias voltage, demonstrates the possibility of modulating the detected light controlling V_{pn}.

A very important result is the significantly lower slope and the lack of changes in the trend for the curve observed in Fig. 11 for $V_{LEC} = 0$ V (black circles). This confirms that the response in the current of the diode is due to only optical stimuli, and not an electrical one. In addition, it rules out the possibility of the variations in the slope being caused by a transport regime change in the leakage current of the diode.

4. Conclusion

The design and fabrication of a monolithic, fully Si-based, CMOS compatible, optical system, integrating the light emitter, were presented. Only Si-based materials and standard technologies were used, and emission spectra in the visible range is to be detected.

It was verified that there is an unequivocal relation between the stimuli to the emitter, and the readings of the sensors, meaning that the response is clearly due to optical stimulation in the photodiode, ruling out the electron-related crosstalk. This was supported by the theoretical projections on the response by the sensor according to the emitted light spectra, the known absorption depths of its bands, and the p-n junction characteristics and behavior. Then, the operation of the proposed system was tested and proven to work as intended. It was observed that it is possible to tune the receiver fabrication and applied voltage to choose specific wavelength bands to be detected, meaning there is an important potential for a diversity of applications involving specific wave-length detection. To the best of our knowledge, these results are the first demonstrating a functional Integrated Optical System for sensing applications using only standard Si-based CMOS technologies which includes a visible wide spectrum light emitter developed by films with nanostructures, based on silicon rich silicon dielectrics.

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