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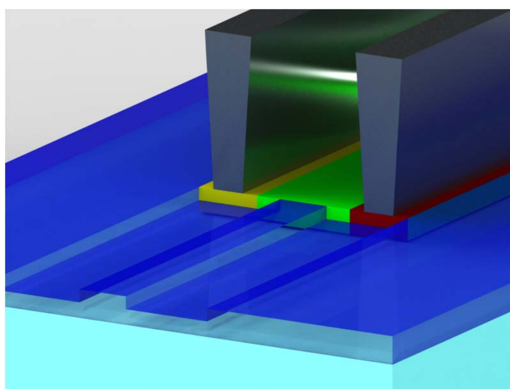

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Ge-on-Si Plasma-Enhanced Chemical Vapor Deposition for Low-Cost Photodetectors

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Abstract: The development of low-thermal-budget Ge-on-Si epitaxial growth for the fabrication of low-cost Ge-on-Si devices is highly desirable for the field of silicon photonics. At present, most Ge-on-Si growth techniques require high growth temperatures, followed by cyclic annealing at temperatures $> 800\ ^{\circ}$C, often for a period of several hours. Here, we present a low-temperature (400 °C) low-cost plasma-enhanced chemical vapor deposition (PECVD) Ge-on-Si growth study and, subsequently, fabricate a high-speed zero-bias 12.5-Gb/s waveguide integrated photodetector with a responsivity of 0.1 A/W at a wavelength of 1550 nm. This low-energy device demonstrates the feasibility of the PECVD method for the fabrication of low-cost low-thermal-budget Ge-on-Si devices.

Index Terms: Germanium, integrated optoelectronics, optical device fabrication, photodiodes, silicon photonics.

1. Introduction

Crystalline and poly-crystalline Ge-on-Si has many applications in the fields of complementary metal oxide semiconductor (CMOS) electronics [1], micro-electromechanical systems (MEMS) [2], and photonics [3]. Ge has both a higher electron and hole mobility than Si [1], and can therefore enable faster electronic devices such as transistors [4], [5], for example. Ge is aggressively etched by H_2O_2, or by a conventional RCA-one solution $(H_2O : H_2O_2 : NH_4OH)$, making it ideal for a sacrificial layer in MEMS applications. It has also become the preferred system for some near-infrared and mid-infrared photonic devices. For the near infrared, Ge is important for the fabrication of photodetectors [6], [7], quantum confined stark effect (QCSE) modulators and detectors [8], [9], and Franz-Keldysh modulators [10]. When extended to mid-infrared wavelengths, Ge-on-Si becomes one of the media of choice for waveguides [11], [12] and other passive devices [13]–[16], with optical transmission to beyond 10 μm [17]. In order to optimize device performance, high-quality Ge-on-Si growth is of the utmost importance.

A number of Ge-on-Si growth methods have been demonstrated including molecular beam epitaxy (MBE) [18] and a number of variations of chemical vapor deposition (CVD) [19]–[21]. The majority of these techniques use high temperatures ($> 600\ ^\circ C$) for Ge growth and subsequent annealing ($> 800\ ^\circ C$) to improve layer quality. However, such temperatures invariably increase the thermal budget, and therefore cost of fabrication, and risks adversely affecting devices already present on the substrate. Therefore a low temperature Ge-on-Si growth technique is desirable for certain applications.

The biggest challenge faced by all Ge-on-Si growth methods stems from the 4.2% difference between the lattice constants of Ge and Si. During epitaxial growth, this lattice mismatch leads to the formation of stress relieving lattice dislocations which propagate to the Ge surface as threading dislocations. Such dislocations inevitably inhibit the performance of resulting devices, by increasing dark current or introducing carrier recombination centers, for example. It is therefore desirable to minimize the threading dislocation density (TDD) in the Ge layer.

In this paper we use a low thermal budget, plasma-enhanced chemical vapor deposition (PECVD) technique to grow single crystal Ge-on-Si layers. The low costs associated with maintaining a PECVD tool, when compared with a reduced pressure chemical vapor deposition (RPCVD) tool, make this an attractive growth technique for low cost applications. The grown layer quality is examined using a range of techniques for a variety of growth temperatures and GeH_4 gas flows. The high quality Ge-on-Si is subsequently used to fabricate a high-speed, low-cost, low-energy, waveguide integrated photodetector.

2. Experimental Details

Ge growth was performed in an Oxford Instruments System 100 PECVD tool on 6 inch (100) Si wafers. The pre-growth cleaning process is of the utmost importance if a high quality Ge layer is to be achieved. It is vital that the substrate has a clean surface, free from both contamination and native SiO_2, for the epitaxial layer to seed correctly. There are two main methods of pre-growth cleaning; an HF dip, or a high temperature bake at approximately 850 °C [22]. The HF dip removes the native SiO_2 from the substrate surface, and forms a passivation layer with H terminated surface bonds, so that the wafer can be wet cleaned and handled in air. This enables the wafer to be transferred to the reaction chamber without the formation of a new native SiO_2, by reducing the substrates reactivity with air by 13 orders of magnitude [22]. Alternatively, a high temperature bake (typically $> 850\ ^\circ C$) desorbs the native SiO_2 from the substrate surface. However, such a high temperature bake exceeds the low temperature restriction. Therefore, prior to growth, the Si wafers were cleaned in 20:1 dilute HF acid, before immediate loading into the PECVD chamber. An Ar diluted GeH_4 (10%) precursor gas was used for all experiments. The chamber pressure was set to 500 mT for all experiments, with an H_2 gas flow of 100 standard cubic centimeters per minute (sccm), and a radio frequency (RF) power of 20 W. The temperature was varied between 250 °C and 400 °C, and the GeH_4 gas flow was varied between 1.5 sccm and 10 sccm, as described in Table 1. The role of H is very important in Ge-on-Si growth. Film crystal structure is primarily governed by the diffusion length of the precursors on the growing surface [23]. Crystallization is promoted by high H dilutions, such as those used for samples B-E, because H adsorption on the growing surface increases the diffusion length of the adsorbed Ge, resulting in the formation of crystallites. H may also act as an etchant that preferentially eliminates the energetically weakest Ge-Ge configurations associated with the amorphous phase, therefore leaving only the energetically stronger crystalline phases, similar to that observed with Si growth [24]. Additionally, H atoms may diffuse several layers into the growing film, which subsequently relaxes the Ge-Ge network, thereby enhancing the possibility of crystallite formation, again, similar to what is observed with Si growth [25].

When 20 W of RF power is applied across the two electrodes in the CVD chamber, the GeH_4 gas is broken down into Ge and H radicals. This has the benefit that the liberated H scavenges any oxygen in the chamber, therefore reducing oxide inclusions in the Ge film [26]. The 20 W of

TABLE 1

Summary of process variables and characterization results for the Ge-on-Si PECVD growth study. For all samples, the growth pressure was 500 mT, the RF power was 20 W, and the H_2 flow was 100 sccm. Poly = Poly–Crystalline, SC = Single crystal

Sample	GeH_4 flow (sccm)	Growth temp. (°C)	Thickness (nm)	Growth rate (nm/min)	Post growth anneal	% with voids	Crystal state	Ge (400) FWHM (arcsec)	RMS surface roughness (nm)
A	10	250	1250	4.17	/	75	poly	2620	14.0
					600°C 2 mins	60	poly	2150	13.7
B	2.5	250	980	1.09	/	0	SC	2545	10.5
					600°C 2 mins	0	SC	1115	5.6
C	2.5	400	922	1.01	/	0	poly	2538	36.6
					600°C 2 mins	0	poly	1109	32.2
D	1.5	400	625	0.52	/	0	poly	2513	26.9
					600°C 2 mins	0	poly	1089	22.3
E step 1	2.5	250	~15	~1.09	/	0	SC	2480	4.1
E step 2	1.5	400	690	0.52	600°C 2 mins	0	SC	1012	3.5

RF power was selected as a compromise between high growth rate and low void fraction [27]. After growth was complete and the wafers had been removed from the PECVD chamber, they were cleaved to enable a sample from each wafer to be annealed. This was carried out using a rapid thermal annealer (RTA) at 600 °C, in an inert N_2 atmosphere, for 2 min., in order to reduce the TDD of the layer, decrease the surface roughness, and improve layer quality. The layers, both as grown and annealed, were then characterized using scanning electron microscopy (SEM) imaging, X-ray diffraction (XRD) rocking curves, electron backscatter diffraction (EBSD) maps, atomic force microscopy (AFM) surface roughness measurements, and in the case of Sample E, transmission electron microscopy (TEM) to estimate TDD. A summary of these results is detailed in Table 1.

3. Results

As observed by Poulsen *et al.* [27], a high growth rate resulted in voids observable in 75% of the Ge layer [sample A—see Fig. 1(a)]. It is hypothesized that the lower portion of the layer is void free due to the relatively low stress levels. After approximately 426 nm voids begin to form in order to relieve the stress within the layer. In order to remove these voids, it was necessary to decrease the growth rate below 4 nm/min. This was achieved by increasing the dilution of the GeH_4 precursor gas by reducing its flow to 2.5 sccm [sample B—see Fig. 1(b)]. Once a void free layer had been realized, the temperature was increased to 400 °C (sample C) in an attempt to improve the layer quality by increasing the surface adatom mobility, similar to what is observed with Si epitaxial growth [28]. However, it was found that at this higher temperature a large number of stress relieving pyramidal hillocks were present on the layer surface. It is predicted that this higher temperature favors Stransky-Krastanov growth, resulting in the initial formation of 3D islands at the Ge-Si interface. The growth rate at this temperature was subsequently reduced by a further decrease in the GeH_4 flow to 1.5 sccm (sample D), but this resulted in a greater number of hillocks on the sample surface [see Fig. 1(c)]. In order to reduce the number of hillocks on the layer surface, a 2-step growth process (sample E), comprising a low temperature step (250 °C) followed by a high temperature step (400 °C) was used. This resulted in a dramatic reduction in the number of hillocks observed on the Ge surface, due to the presence of the initial low temperature wetting layer. Further analysis of sample E is presented in Figs. 2 and 3.

The Ge-on-Si growth (recipe E) is also non-selective to SiO_2 surfaces [see Fig. 1(d)], unlike other CVD growth methods [29], making it suitable for the initial growth for rapid melt growth (RMG) applications [30], and other applications that require growth on SiO_2. It is proposed that the presence of Ar (used to dilute GeH_4) limits the Ge adatom surface mobility [31] so that nucleation occurs on the SiO_2 surface as well as on the Si surface.

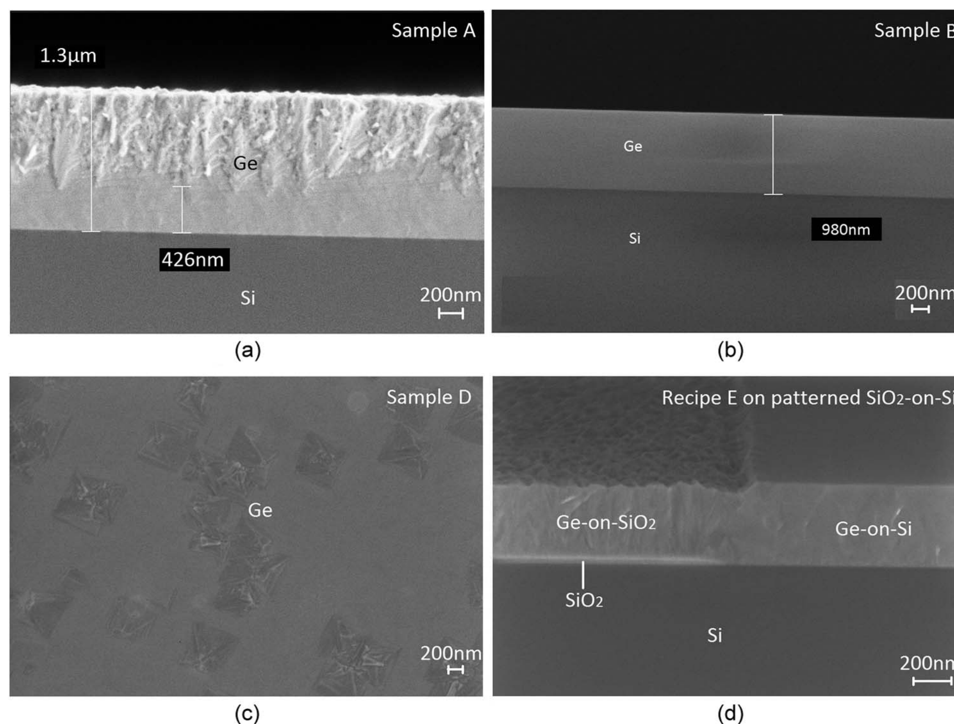

Fig. 1. SEM images of various Ge-on-Si PECVD growth recipes. (a) Cross-section of sample A, showing voids in layer due to high growth rate. (b) Cross-section of sample B, showing removal of voids by reducing the growth rate. (c) Plan view of sample D, showing a high number of stress relieving pyramidal hillocks. (d) Angled cross-section of recipe E, grown on a patterned SiO_2-on-Si wafer, showing non-selective growth and removal of stress relieving hillocks using a 2-step growth method.

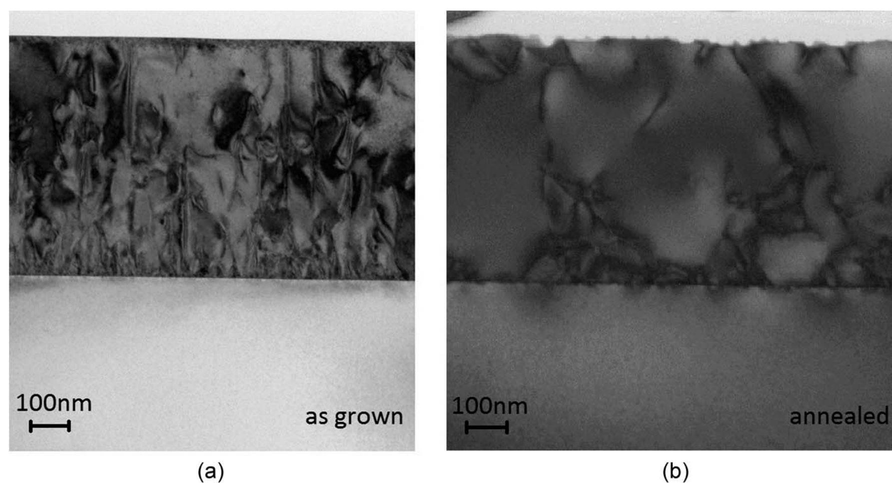

Fig. 2. TEM images of sample E showing the effects of annealing. (a) As grown. (b) After annealing at 600 °C for 2 min. in an inert N_2 atmosphere.

In order to estimate the TDD of sample E, TEM imaging was performed, on both the as grown [see Fig. 2(a)] and annealed [see Fig. 2(b)] samples. Prior to focused ion beam (FIB) milling, the samples were coated with carbon for protection and then imaged at 200 kV in bright-field TEM mode.

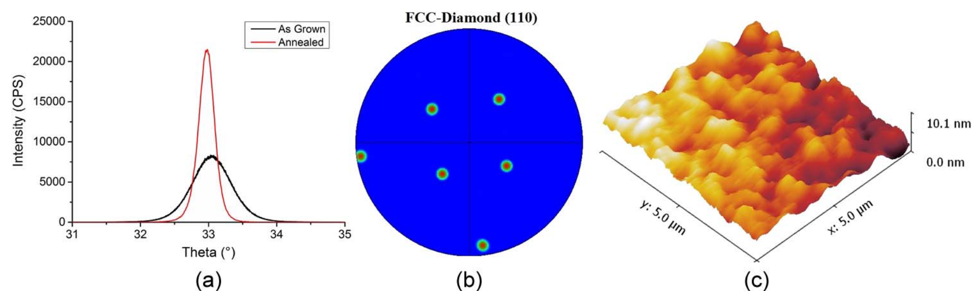

Fig. 3. Ge characterization showing the growth of a single crystal layer (sample E—annealed). (a) XRD rocking curve showing the improvement in material quality after annealing. (b) EBSD pole figure viewed from the (110) direction. (c) AFM surface roughness scan showing an RMS roughness of 3.5 nm.

From these images, it can be estimated by counting the threading dislocations, that the TDD is approximately 2×10^9 cm^{-2} prior to annealing, and approximately 3.3×10^8 cm^{-2} after annealing. This is a reduction in TDD of approximately one order of magnitude. It is proposed that the mechanism for defect reduction is thermal-stress induced dislocation glide and annihilation [32]. The anneal was performed at only 600 °C in order to maintain the low temperature process, in conjunction with a typical anneal temperature for dopant activation in Ge [33]. Therefore, a further improvement in TDD is expected with cyclic annealing at a higher temperature [34].

XRD rocking curve measurements were used as a measure of crystal quality [35]. The full width at half maximum (FWHM) of each peak is a measure of the mosaicity of the layer (i.e. the degree of mis-orientation from the perfect single crystal). As shown in Fig. 3(a) (sample E) and detailed in Table 1, the mosaicity is improved by thermal annealing for all samples. Theta-2theta scans were used to determine the number of preferred crystal orientations in the Ge layer, to therefore conclude whether the layer was poly-crystalline or single crystal (see Table 1).

EBSD maps were also used to determine crystal orientation and grain size. The EBSD maps were converted into pole figures, as shown in Fig. 3(b) (sample E—annealed), which illustrate stereographic projections of the orientation distribution of crystallographic lattice planes, in this case when viewed from the (110) direction. This pole figure confirms that the material is single crystal.

Finally, AFM maps were used to determine surface roughness, as shown in Fig. 3(c) (sample E—annealed), which indicates a root mean square (RMS) roughness of 3.5 nm for a Ge thickness of 690 nm. Other RMS roughness values are detailed in Table 1. It is important that surface roughness is reduced in order to limit surface leakage currents, and optimize integration. Chemical mechanical polishing (CMP) can be used as a method of reducing surface roughness [29].

The highest quality layer (sample E) was subsequently used to fabricate a low cost, waveguide integrated photodetector. Fabrication was carried out on 6 inch silicon-on-insulator (SOI) wafers, with a buried oxide (BOX) thickness of 2 μm, and a Si overlayer thickness of 400 nm. 350 nm deep trenches were etched into the Si overlayer using a 50 nm SiO_2 hard mask, after which blanket, non-selective Ge growth was performed to a thickness of 350 nm. The Ge layer was subsequently etched via an inductively coupled plasma (ICP) process, with the SiO_2 layer acting as an etch stop. This leaves Ge only in the trenches, enabling a butt coupled device configuration. No thermal annealing of the Ge layer was performed, as a 600 °C dopant activation anneal was performed after ion implantation. 450 nm wide, single mode waveguides and associated grating couplers were then etched into the Si overlayer to enable coupling of light into the devices. Ion implantation was used to obtain a lateral $p{-}i{-}n$ junction, which was then passivated with an SiO_2 layer. Vias were etched into this SiO_2 layer to enable Ti/Al metal contacts to be sputtered, which were defined by ICP etching. A schematic of the photodetector device and a cross-section FIB SEM image is shown in Fig. 4. The intrinsic region dimensions were $L = 5$ μm and $W = 1.5$ μm.

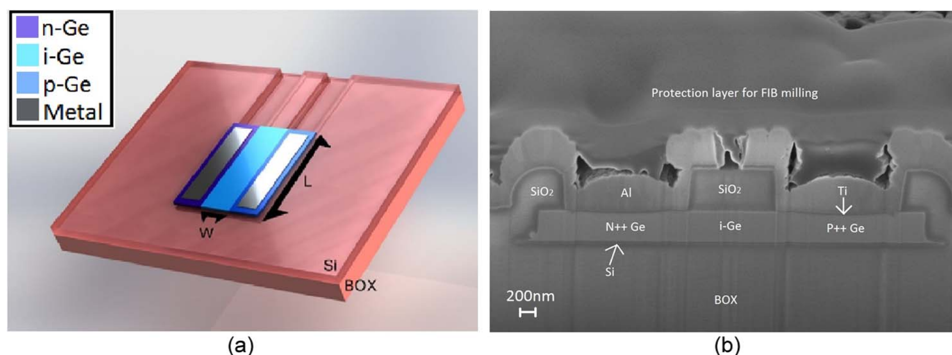

Fig. 4. Waveguide integrated, butt coupled photodetector layout. (a) Device schematic showing intrinsic region dimensions. (b) Cross section FIB SEM image of the fabricated device. The layer on top of the Al is a protective layer added prior to FIB milling for protection of the device.

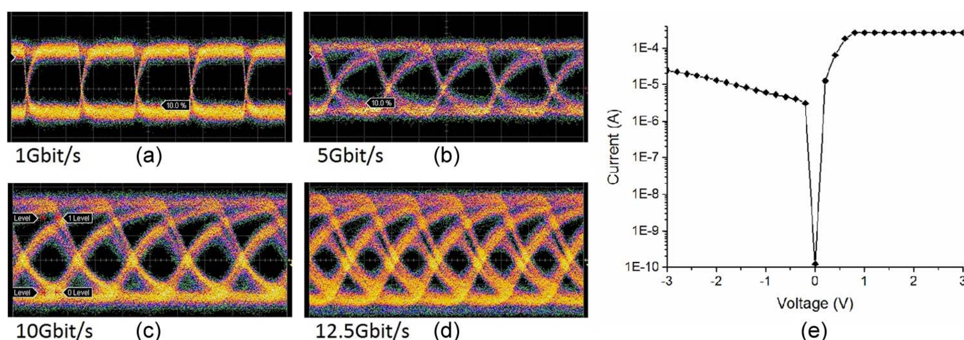

Fig. 5. Photodetector performance analysis showing eye diagrams at various data rates with zero volts applied bias and IV characteristics. (a) 1 Gbit/s, (b) 5 Gbit/s, (c) 10 Gbit/s, (d) 12.5 Gbit/s, and (e) IV characteristics. Device intrinsic dimensions: $W = 1.5\ \mu$m, $L = 5\ \mu$m, and $\lambda = 1550$ nm.

In order to measure the high-speed performance of the photodetectors, a modulated optical signal was generated using an electrical pseudo-random binary sequence (PRBS) source, driver amplifier, and commercial $LiNbO_3$ modulator. This signal was amplified using an erbium doped fiber amplifier (EDFA), and subsequently coupled to the device using an optical fiber and a grating coupler. The resulting open eye-diagrams for data rates in the range 1 Gbit/s to 12.5 Gbit/s at 0 V DC bias are shown in Fig. 5(a)–(d). These diagrams show that the device is capable of working with no applied bias. This demonstrates the built-in electric field is sufficient to collect the generated carriers. Due to high surface leakage current from some devices, the IV curves are rather variable, so detailed analysis may not be representative of all devices, and is the subject of future work. One of the better IV curves is shown in Fig. 5(e).

The DC characteristics were measured by directly coupling light from a tunable wavelength laser into the photodetectors via an optical fiber and grating coupler. A responsivity of 0.1 A/W at 1550 nm was measured, with no applied bias. There are a number of potential reasons why the responsivity is fairly low. Firstly, it was observed during fabrication that there was a slight misalignment between the input waveguide and the central, intrinsic region of the photodetector. Therefore, some of the optical signal may be leaking into the doped regions, where any photogenerated carriers are likely to recombine before they are swept out of the device. Secondly, the high defect density of the Ge layer could lead to a small recombination time, even in the electric field, intrinsic region. Surface recombination is also prevalent in thin layers such as this. As a result, it is possible that not all of the photogenerated carriers are swept out of the device before they recombine, and therefore they do not contribute to the measured current. In addition, the surface leakage path effectively provides a parallel resistance to the current meter

used to measure the photogenerated current. Therefore, the measured current may be lower than the actual photogenerated current due to some current flow through this leakage path.

4. Conclusion

In conclusion, the low temperature PECVD Ge-on-Si growth method demonstrated here is suitable for low cost Ge devices such as photodetectors, for example, and can be performed using a commonly accessible tool. This is demonstrated by the fabrication of a 12.5 Gbit/s, zero bias, waveguide integrated photodetector.

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