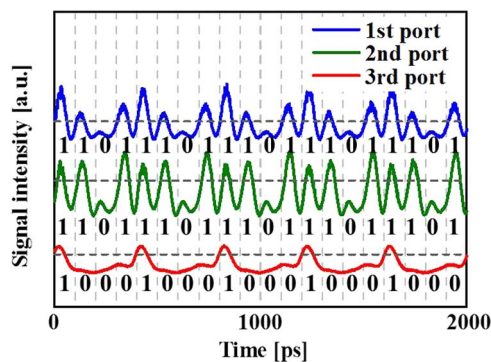


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Abstract: We experimentally realize seamless operations with below 100-fs timing jitter in a 10-GSample/s 3-bit photonic analog-to-digital converter (ADC) with an input 2.5-GHz sinusoidal electrical signal. To address the energy efficiency, it is necessary to explore some serial approaches to get most operations in a photonic ADC done before serial-to-parallel conversion to save the number of devices. To press forward with the work on subsequent operations after optical sampling in a photonic ADC, we have investigated optical quantization and coding and demonstrated their performances. The experimental results successfully demonstrated seamless operations in a photonic ADC, i.e., sampling, quantization, and coding, while keeping its parallel-configuration-free characteristics and low timing jitter below 100 fs. This demonstration could address the energy efficiency by reduction of the number of devices, including electrical ADCs for subsequent operations after optical sampling in existing high-performance photonic ADCs.

Index Terms: Photonic analog-to-digital conversion, optical sampling, optical quantization, optical coding, SSFS.

1. Introduction

Recent tremendous growths in ultra wide-bandwidth applications, such as digital coherent optical communication encourage high-performance analog-to-digital converters (ADCs) for high-speed and flexible signal processing [1]–[3]. Although current electrical ADCs have achieved excellent performance, there is a limitation due to a trade-off issue between sampling rate and resolution induced by electrical jitter of the sampling aperture and ambiguity of the comparator. The trade-off issue demands sacrifice of resolution for upgrade of sampling rate in electrical ADCs. Since, nevertheless, any applications require a certain level resolution, the sampling rate of electrical ADCs cannot unlimitedly upgrade due to electrical jitter. In general, the lower limit of electrical jitter is estimated to 100 fs and it is the significant line to overcome for development of high-performance ADCs. Very low jitter comes from mode-lock pulse lasers have an attractive potential to solve the jitter issue and optical sampling and serial-to-parallel conversion have achieved remarkable results with very low jitter below 100 fs [4], [5]. In particular, serial-to-parallel conversion technique has attracted much attention to connect optically-sampled broadband signals to electrical ADCs by bandwidth matching between them. On the other hand, the higher the sampling rate becomes, the more electrical ADCs are required because parallel use of electrical ADCs are indispensable after

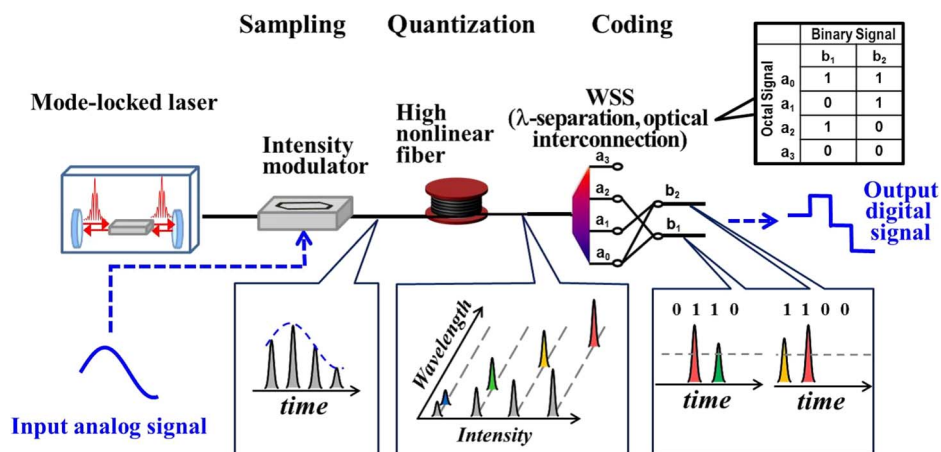


Fig. 1. Schematic diagram of photonic analog-to-digital converter.

serial-to-parallel conversion. Since too much use of high-performance ADCs could lead to power consumption issue, parallel use of high performance electrical ADCs could have concern for much further upgrade of sampling rate of a photonic ADC. To address the energy efficiency, it is necessary to explore some serial approaches to get most of operations in a photonic ADC done before serial-to-parallel conversion to save power consumption. To press forward with the work on subsequent operations after optical sampling in a photonic ADC, we have investigated optical quantization and coding and demonstrated their performances [6]–[10].

In this paper, to the best of our knowledge, we experimentally demonstrate, for the first time, a whole operation, i.e., sampling, quantization, and coding, of a 10-GSamples/s, 3-bit photonic ADC under the condition of low timing jitter below 100 fs.

2. Principle of Photonic Analog-to-Digital Converter

To substitute spatially-parallel processing with spatially-serial approaches, one of the promising architectures would be wavelength division multiplexed (WDM-MUXed) one because WDM-MUXed data keep a parallel form in spectral domain although data propagate through a single line. It suggests that we can treat parallel data in a single line without increasing the number of devices such as electrical ADCs. We have investigated such a parallel configuration free architecture for photonic ADC based on the WDM-based approach.

Fig. 1 shows the schematic diagram of the proposed photonic ADC [6]–[10]. In an optical sampling part, sampling pulses and an input ultrawide-bandwidth analog signals are entered into a lithium niobate intensity modulator (LN-IM). The input analog signal is superimposed on an optical sampling pulse train and fed to a subsequent optical quantization part. An input analog signal is optically sampled and fed to a high nonlinear fiber (HNLF) for optical quantization. Since soliton self-frequency shift (SSFS) in a HNLF can generate a different color signal proportional to an input peak power, a peak power of each optically-sampled signal can be identified by an output signal color after SSFS. Once each input peak power is identified by each color, an arrayed waveguide grating (AWG) can separately split each different colored signal into a different port as a level identification signal and optical quantization can be realized by power-to- λ conversion. The additionally-subsequent self phase modulation (SPM)-based spectral compression in a fiber can improve the resolution of the color separation because it enables to compress the bandwidth of each level identification signal. This approach can be easily connected to any optical coding subsystems such as pulse shaping or optical interconnection so as to generate a binary pulse signal for a desired digital signal output. For example, an appropriate optical interconnection can provide multiple-bit binary codes in a bit-parallel format based on the octal-to-binary conversion table as shown in Fig. 1. The optical interconnection

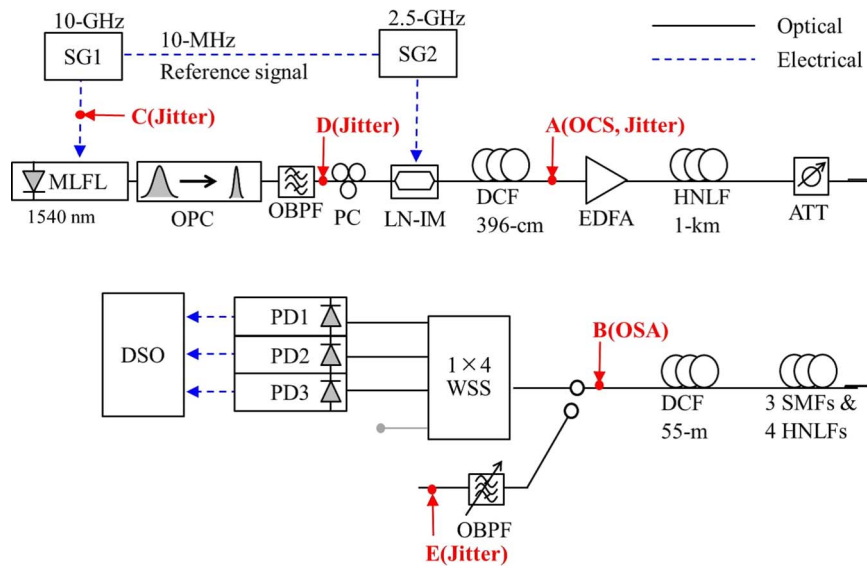


Fig. 2. Experimental setup.

in Fig. 1 is that for a 2-bit ADC. The level identified signals a_0 - a_3 after wavelength separation and the outputs b_1 - b_2 are octal signals and binary signals, respectively. Consequently, each bit in a 2-bit binary code b_1 - b_2 is formed by combination of level identification signals a_0 - a_3 . Through a whole operation from optical sampling to coding, a system can almost keep its parallel-configuration-free characteristics just before the bit parallel coding part.

3. Experimental Demonstration

3.1. 10-GSamples/s, 3-bit Photonic ADC

The experimental setup is shown in Fig. 2. A mode-locked fiber laser (MLFL: PriTel Inc., UOC-5-14G), which produces pulses of 1.62-ps full width at half maximum at 1540 nm center wavelength and has a repetition rate of 10-GHz, is used as the source of the sampling pulses. The MLFL is driven by a signal generator (SG: HP, 8673B). The sampling pulses are compressed using an optical pulse compressor (OPC: PriTel Inc., FP-300) to 350-fs full width at half maximum for inducing SSFS efficiently. For optical sampling, we use a LN-IM with a 2.5-GHz electrical sinusoidal signal from another SG (Anritsu, MG3692A).

Fig. 3(a) show the waveform of the sampled signal which are measured with a 50-GHz photodetector (PD: U2T, XPD2120R) and a 50-GHz digital sampling oscilloscope (DSO: Tektronix, 11801C SD-32). The waveform of the sampled signal after 10-GSamples/s sampling operation for input 2.5-GHz sinusoidal analog signal is well consistent with the original waveform. After optical sampling, the power of the sampled signals is amplified up to 15 dBm using an erbium-doped fiber amplifier (EDFA: Alnair Labs, HPA-200C). A 396-cm dispersion compensation fiber (DCF) is used for pre-dispersion compensation of EDFA.

At the quantization part, the sampled signals are propagated in an HNLF (length: $L = 1000$ (m), nonlinearity: $\gamma = 25$ ($\text{W}^{-1}\text{km}^{-1}$), dispersion: $D = 6.6$ ($\text{ps}/\text{nm}/\text{km}$), and dispersion slope: $S = 0.026$ ($\text{ps}/\text{nm}^2/\text{km}$)) to induce SSFS, as well as three single-mode fibers (SMFs) and four HNLFs to compress the output spectra. The quantized signals were propagated in a set of SMFs and HNLFs for SPM-based spectral compression [11]. The spectral compression part was composed of 3 SMFs and 4 HNLFs and they were connected in the following order: 10-m SMF ($D = 17$, $S = 0.06$, $\gamma = 1.5$), 110.5-m HNLF ($D = -0.226$, $S = 0.0268$, $\gamma = 9.3$), 30-m

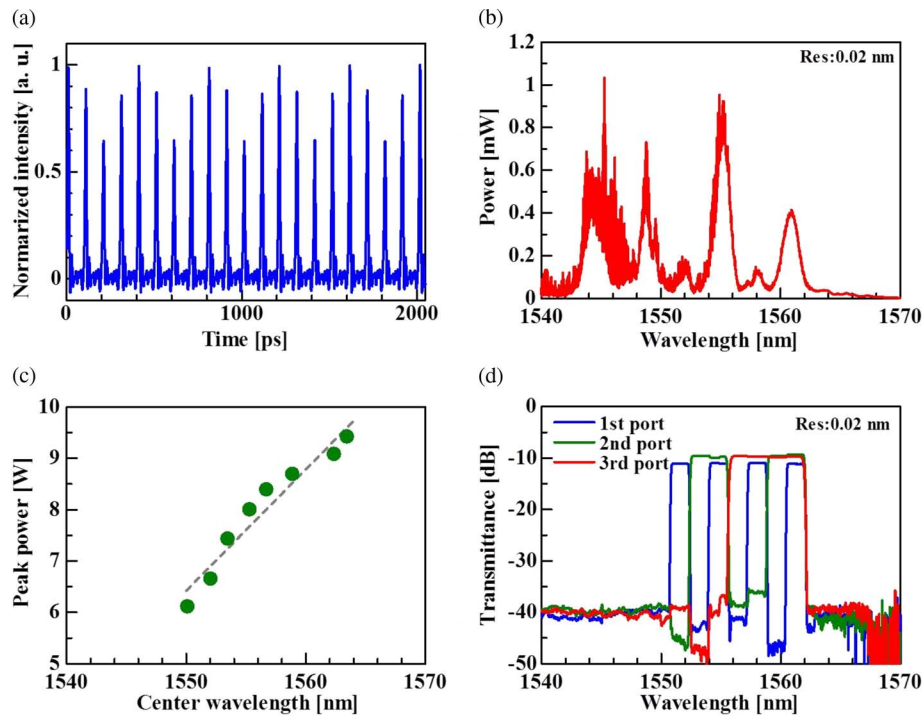


Fig. 3. (a) Measured waveform of sampled signal at point A. (b) Measured optical spectrum after optical quantization at point B. (c) Relation between measured center wavelength at point B and input peak power of sampled signal for 1-km HNLF. (d) Transfer function of wavelength selective switch for optical coding.

SMF ($D = 17$, $S = 0.06$, $\gamma = 1.5$), 400-m HNLF ($D = 0.044$, $S = 0.029$, $\gamma = 20$), 100-m SMF ($D = 17$, $S = 0.06$, $\gamma = 1.5$), 500-m HNLF ($D = 0.044$, $S = 0.0029$, $\gamma = 20$), and 116.851-m HNL-DSF ($D = 0.325$, $S = 0.031$, $\gamma = 6.2$).

Fig. 3(b) shows the output spectrum of the optically sampled signal of Fig. 3(a). It is measured with an optical spectrum analyzer (OSA: Advantest, Q8384). In the measured optical spectrum, there are 3 strong peaks between 1549 nm and 1561 nm and the second peak at 1555 nm is twice as high as other two peaks due to two SSFS signals induced by the same intensity two pulses in Fig. 3(a). From Fig. 3(a), we can see a set of four pulses repeats in the signal and two pulses in the set have the same intensity and these two pulses induce the same wavelength shift at 1550 nm in Fig. 3(b). At the coding part, we used a wavelength selective switch (WSS: Finisar, WaveShaper 4000 s) for wavelength separation and optical interconnection. Fig. 3(c) shows the relation between measured center wavelength at point B and input peak power of a sampled signal for 1-km HNLF. We can find almost linear relationship between them.

Fig. 3(d) shows the three coding transfer functions of WSS. The shape of each function is a super-Gaussian profile of 200-GHz, 400-GHz, and 800-GHz full width at half maximum with spacing 400-GHz, 800-GHz, and 1600-GHz. Resolution of coding is limited by C-Band (1530–1565 nm) operation bandwidth of WSS. If WSS were operating up to 1625 nm, the expected resolution would increase to 5 bits.

Three coded signals from WSS are fed to 10-GHz photo-detectors (PD: Nortel, PP-10G). Fig. 4(a) shows the waveforms of three coded signals from WSS. These waveforms are measured with 20-GHz sampling heads (Tektronix, SD-26). Output digital signals are acquired by setting threshold voltage for the waveforms after optical coding. Fig. 4(b) shows the waveforms of an input analog signal and an output digital signal. From these waveforms, we can see the waveform of the output digital signal after 10-GSamples/s, 3-bit photonic ADC is well consistent with the original waveform.

Fig. 5(a) and (b) show measured SSB phase noise spectra with frequency offset range of 100-Hz to 100-kHz. Fig. 5(a) shows the SSB phase noise of signal generator at point C, sampling pulse at point D, and sampled signal at point A. Fig. 5(b) shows the SSB phase noise of quantized signal with center wavelength range of 1550 nm to 1580 nm at point E. Phase noise can be readily converted into a measure of timing jitter σ in a RMS sense

$$\sigma = \frac{1}{2\pi f_m} \sqrt{2 \int_{f_l}^{f_h} L(f) df} \quad (1)$$

where f_m and f are the laser repetition rate and the frequency offset measured from the laser repetition rate, and f_l and f_h are, respectively, the low and high limits of integration [12]. Timing jitter (integration range: 100-Hz to 100-kHz) of a signal generator, a sampling pulse, a sampled signal are accumulated, respectively, 80 fs, 77 fs, 74 fs. Timing jitter figure of quantized signal were from 93 fs to 104 fs depending on a center wavelength. Fig. 5(c) shows the center wavelength dependence of timing jitter figure. Below 100 fs timing jitter was accomplished up to 1570 nm center wavelength of quantized signal. Increasing timing jitter with wavelength shift was reported before [13].

4. Conclusion

We experimentally realized seamless operations with below 100 fs timing jitter in a 10-GSamples/s, 3-bit photonic analog-to-digital converter with input 2.5-GHz sinusoidal electrical signal. The experimental results successfully demonstrated a whole operation; sampling, quantization, and coding, with keeping its parallel-configuration-free characteristics as well as low timing jitter below 100-fs. This demonstration could address the energy efficiency by reduction of the number of devices including electrical ADCs for subsequent operations after optical sampling in existing high performance photonic ADCs. One of our future works will cover the integration using silicon photonics with the chalcogenide technology [14], and it is expected to enhance the energy efficiency furthermore.

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