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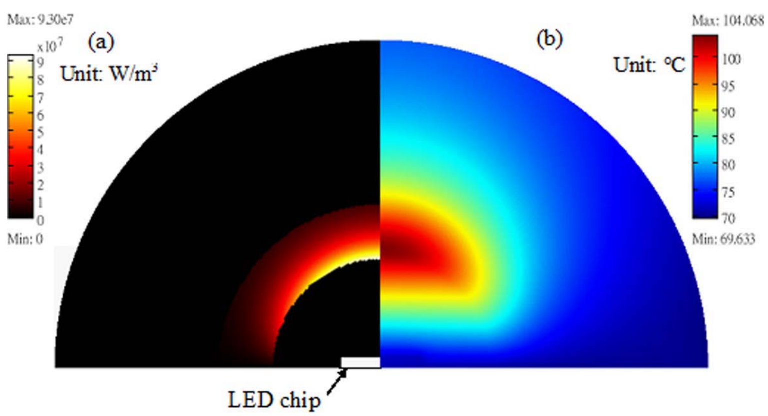

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Te-yuan Chung, Shih-Chen Chiou, Yu-Yu Chang, Ching-Cherng Sun, Tsung-Hsun Yang, and Szu-Yu Chen

Department of Optics and Photonics, National Central University, Taoyuan 32001, Taiwan

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Abstract: Both theoretical and simulation approaches were used to obtain the thermal power and temperature distribution in phosphor-converted white LEDs (pc-WLEDs) using a remote-dome phosphor package (RDPP). Different material and geometric parameters were systematically and thoroughly studied. An experiment was performed to measure the temperature distribution in an RDPP pc-WLED, which confirmed the simulation results. Given practical limitations of the material parameters, the most feasible method to reduce the phosphor temperature is to extend the dome radius and the thickness of the phosphor region.

Index Terms: Solid-state lighting, phosphor, temperature.

1. Introduction

The efficiency of phosphor converted white LEDs (pc-WLED) has been greatly improved thanks to significant progress in the technology involved in epitaxy, packaging, phosphor, and thermal management. As a consequence, pc-WLEDs are currently utilized for various general lighting products [1]. However, the performance of blue LED chips is known to be highly temperature dependent [2]. The emission peak wavelength and the wall plug efficiency are both functions of the LED junction temperature, making improved thermal management one of the most important issues for LED applications [3]. The performance of phosphors in pc-WLEDs is also temperature dependent [4], [5]. Obviously, the phosphor is also a heat source since the conversion of higher energy photons into lower energy photons leads to heat generation. The phosphor is commonly mixed with a silicone matrix which has poor thermal conductivity [6]. If the phosphor region does not have a short thermal conduction path to the cooling mechanism, there may be heat build-up in that region leading to a high temperature during operation. However, the temperature issues of phosphor in pc-WLEDs have not often been considered. Meneghini *et al.* reported that high temperature stress or even a high storage temperature will lead to degradation of the yellow light emission in yellow pc-LEDs [7]. Luo *et al.* observed silicone carbonization in the phosphor region of pc-WLEDs and suggested that phosphor self-heating is responsible for such a phenomenon. They established an approximated stair-like thermal load model to estimate the temperature distribution in the phosphor region [8]. Fulmek *et al.* carried out a simulation to study the

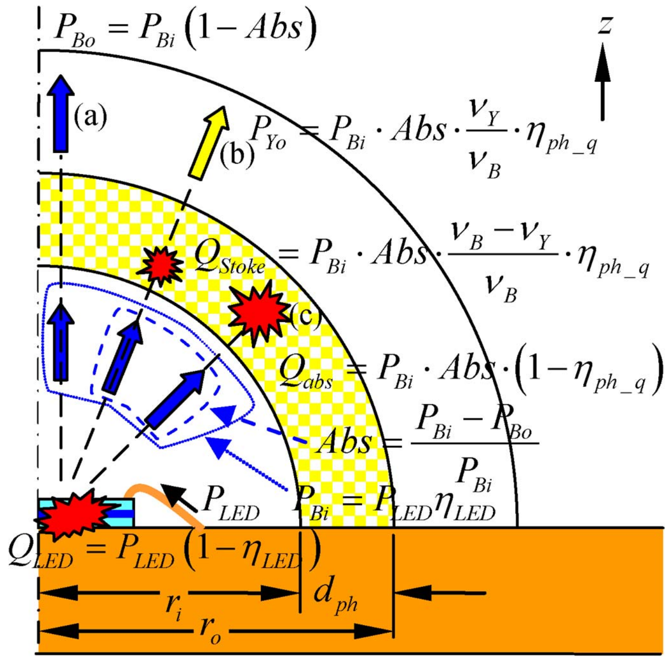

Fig. 1. Power budget and geometry of a pc-WLED. (a) Mechanism in which a blue photon directly passes through the phosphor region and (b) the mechanism in which a blue photon is absorbed by the phosphor region and converted into a yellow photon. The energy difference turns into thermal energy in the phosphor region. (c) Mechanism in which a blue photon is absorbed by the phosphor region and all the energy turns into thermal energy in the phosphor region.

thermal load in pc-WLEDs fabricated using a plate-shaped phosphor geometry and suggested that the highest temperature is located in the phosphor region [9]. Wenzl *et al.* reported on a simulation study of the thermal behavior of plate-shaped phosphor pc-WLEDs under direct current (DC) and various pulse width modulation (PWM) driving conditions [10]. In this work, a remote dome phosphor package (RDPP) pc-WLED is thoroughly studied. Both theoretical and simulation approaches are used to evaluate the thermal power and temperature distribution within the pc-WLED. The influences of the different material and geometric parameters are also discussed in detail.

2. Thermal Power in a pc-WLED

The simplified power flow of a pc-WLED is depicted in Fig. 1 without considering the substrate surface absorption, LED chip re-absorption, phosphor re-absorption, or boundary Fresnel reflection of the silicone matrix. The electrical, thermal and optical powers are involved and entangled. Here, Q indicates the thermal power and $\dot{q}$ indicates thermal power density; P_{LED} indicates the input electric power. The other symbol P indicates the optical power. The subscripts B and Y indicate blue and yellow photon/light, respectively; subscripts i and o indicate the initial power and final output, respectively. The thermal power generated by the LED chip is

$$Q_{\mathrm{LED}} = P_{\mathrm{LED}} \cdot (1 - \eta_{\mathrm{LED}}) = \int_{\mathrm{chip}} \dot{q}_{\mathrm{LED}}(x, y, z)\, dV \tag{1}$$

where η_{LED} is the light generation energy efficiency of the LED chip, and $\dot{q}_{\mathrm{LED}}(x, y, z)$ is the thermal power density distribution of the chip. The optical power of the blue photon generated by the chip is $P_{0B} = P_{\mathrm{LED}} \cdot \eta_{\mathrm{LED}}$. The generated blue photons then interact with the phosphor region. Three mechanisms of photon-phosphor interaction should be considered. The first mechanism is pure absorption in which the blue light is absorbed but all the energy is transferred into heat. The second mechanism is which the blue photons are absorbed and transferred into an equal number of yellow photons. Due to Stokes loss, part of the absorbed energy is transferred into heat. The third mechanism is that the blue light passes through the phosphor region without any loss. The first two mechanisms make the phosphor region the secondary heat source in the pc-WLED. The fraction of blue light power absorbed in the first two mechanisms is defined as the *Abs*, or the absorbance of the phosphor region. The outgoing blue light power can then be written as

$$P_{Bo} = P_{0B}(1 - Abs) \tag{2}$$

and the outgoing yellow light power is

$$P_{Yo} = P_{Bi} \cdot Abs \cdot \frac{\nu_Y}{\nu_B} \cdot \eta_{ph\_q} \tag{3}$$

where v_B and v_Y are the effective blue and yellow photon frequencies which can be solved using the LED chip and phosphor emission spectra; η_{ph_q} is the quantum conversion efficiency of the phosphor. The total generated thermal power within the phosphor region can be written as

$$Q_{ph} = P_{Bi} \cdot Abs \cdot \frac{\nu_B - \eta_{ph\_q}\nu_Y}{\nu_B} = \int\limits_{\substack{\text{phosphor}\\ \text{region}}} \dot{q}_{ph}(x, y, z)\, dV \tag{4}$$

where $\dot{q}_{ph}(x, y, z)$ is the thermal power density within the phosphor region. The temperature distribution $T(x, y, z)$ within the pc-WLED can be solved using the heat diffusion equation [11]

$$k\nabla^2 T + (\dot{q}_{\text{LED}} + \dot{q}_{ph}) = \rho c_p \frac{\partial T}{\partial t} \tag{5}$$

where k is the thermal conductivity, ρ is the density, and c_p is the specific heat. In other words, as long as the material properties, geometry and boundary conditions are given, only $\dot{q}_{ph}(x, y, z)$ needs to be determined. However, $\dot{q}_{ph}(x, y, z)$ depends on not only the chip emission light pattern but also the absorption coefficient, geometry, scattering, and particle density of the phosphor.

Various phosphor package geometries have been proposed and their packaging efficiencies have been thoroughly studied [1], [12]. The RDPP geometry, which is shown in Fig. 1, reduces the backward light scattering which can be absorbed by the substrate and LED chip. Therefore, lower package loss is expected with such a packaging geometry [1]. Also, the isotropic nature of the phosphor region with respect to the light source may lead to a more uniform angular correlated color temperature (CCT) distribution. In the remainder of this work, only this package will be evaluated and discussed. Since the phosphor region is away from the LED chip, LED light pattern using far-field approximation may be applicable. However, the validity of the far-field approximation should be verified. If an LED chip with a Lambertian light pattern is located at the center of the dome, the irradiance of the blue light in space can then be written as

$$I(r, \theta) = \frac{P_{Bi}\cos\theta}{\pi r^2} \exp\left[-\alpha_{ph} \cdot (r - r_i)\right] \tag{6}$$

where θ is the angle to the substrate surface normal, α_{ph} is the effective absorption coefficient of the phosphor region, r_i is the inner radius of the phosphor dome, and r_o is the outer radius of the phosphor dome. The absorbed power density within the phosphor region can then be derived by

$$P_{ph\_abs}(r, \theta) = \begin{cases} \alpha_{ph} \cdot \frac{P_{Bi}\cos\theta}{\pi r^2} \exp\left[-\alpha_{ph} \cdot (r - r_i)\right], & r_i \le r \le r_o \\ 0, & \text{otherwise.} \end{cases} \tag{7}$$

TABLE 1

Simulation parameters used in this work

Category	Description	Notation	Value [unit]
LED chip parameters	LED input power	P_{LED}	1 W
	LED wall plug efficiency	η_{LED}	0.35
Phosphor parameters	Effective absorption coefficient	α_{ph}	2944 m^{-1}
	Quantum conversion efficiency	η_{ph}	0.9
Optical parameters	Effective blue wavelength	λ_B	450.00 nm
	Effective yellow wavelength	λ_Y	565.85 nm
	Phosphor refractive index	n_{ph}	1.83
	Silicone matrix refractive index	n_{lens}	1.41
Geometric parameters	LED chip volume	$V_{LED} = L \times W \times H$	660×660×100 μm^3
	Phosphor region inner radius	r_i	1.0 mm
	Phosphor region thickness	$d_{ph} = r_o - r_i$	0.5 mm
	Substrate volume	$V_{sub} = 2\pi \times R^2 \times H$	$2\pi \times 10^2 \times 2$ mm
	Silicone matrix lens radius	R_{lens}	3 mm
Thermal parameters	LED chip thermal conductivity	k_{LED}	130 W/m·K
	LED chip density	ρ_{LED}	6150 kg/m^3
	LED chip specific heat capacity	C_{LED}	490 J/kg·K
	Phosphor region thermal conductivity	k_{ph}	0.18 W/m·K
	Silicone matrix thermal conductivity	k_{lens}	0.18 W/m·K
	Silicone matrix density	ρ_{lens}	1100 kg/m^3
	Silicone matrix specific heat capacity	C_{lens}	1175 J/kg·K
	Substrate thermal conductivity	k_{sub}	400 W/m·K
	Substrate density	ρ_{sub}	8700 kg/m^3
	Substrate specific heat capacity	C_{sub}	385 J/kg·K

Considering the quantum conversion efficiency of the phosphor, the thermal power density distribution can then be obtained as follows:

$$\dot{q}_{ph}(r,\theta) = \begin{cases} \alpha_{ph} \cdot \frac{\nu_B - \eta_{ph}\nu_Y}{\nu_B} \cdot \frac{P_{Bi}\cos\theta}{\pi r^2} \exp\left[-\alpha_{ph} \cdot (r - r_i)\right], & r_i \le r \le r_o \\ 0, & \text{otherwise.} \end{cases} \tag{8}$$

3. Simulation

In this work, a series of simple RDPPs are studied. Table 1 lists all the parameters used if no further specific description is given. These parameters are set based on a pc-WLED with an averaged CCT of 6500 K. The phosphor is assumed to be Ce:YAG and the phosphor concentration in the phosphor region is about 15 wt.%. The LED chip is considered to be a uniform volume heat source whose thermal power density can be directly obtained by

$$\dot{q}_{\mathrm{LED}} = \frac{P_{\mathrm{LED}}(1 - \eta_{\mathrm{LED}})}{V_{\mathrm{LED}}}. \tag{9}$$

The absorbed and thermal power distributions in the phosphor region can be evaluated using (8). An alternative way to obtain the absorbed and thermal power density distributions is to use ray-tracing. In this study, the commercially available ray-tracing software, ASAP, is utilized to evaluate the thermal power density distribution for comparison with the theoretical approach. A total of 1 million rays are traced to simulate the blue light emitting from the LED chip with finite size and a Lambertian light pattern instead of the point source assumed in the theoretical approach. In other words, the ray-tracing approach does not use the far-field approximation. Fig. 2 shows the $\dot{q}$ plots obtained with the theoretical approach and the ray-tracing approach. Both results agree well with each other, although the ray tracing result is less smooth than the theoretical result due to the

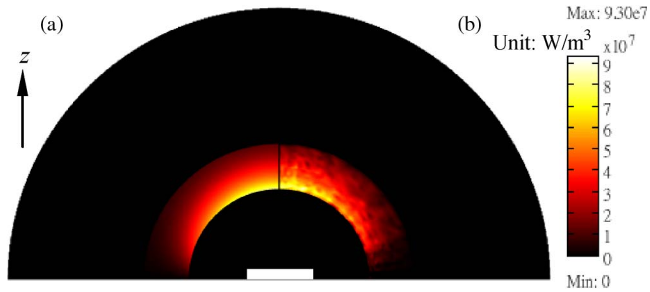

Fig. 2. Calculated thermal power density distribution obtained using the (a) theoretical approach and (b) ray-tracing approach. Both plots share the same color scale as shown on the right in units of W/m^3.

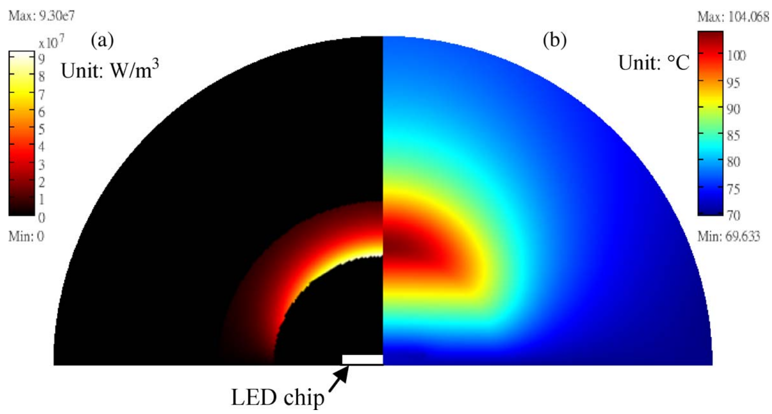

Fig. 3. (a) Thermal power density distribution in units of W/m^3 and (b) temperature distribution in °C obtained in the pc-WLED simulation. LED chip's thermal power density is about 1.49×10^{10} W/m^3 and is not shown in the color scale.

discrete nature of ray-tracing. The Q_{ph} obtained by the ray-tracing approach is about 2% more than the theoretical approach because of the slightly longer absorption path in the phosphor region for the rays emitted from the off-axis points on the LED chip. Therefore, the theoretic approach is acceptable for the phosphor region with inner radius larger than 1 mm.

With $\dot{q}(x, y, z)$, finite element analysis (FEA) can be utilized to evaluate $T(x, y, z)$ within the pc-WLED. The back surface of the substrate is set to have a constant temperature of 70 °C for simplicity. The remaining surfaces are set to have free convection cooling with a heat transfer coefficient of 10 W/m$^2 \cdot$ K. At this point, $\dot{q}(x, y, z)$ and $T(x, y, z)$ within the pc-WLED can be obtained and are shown in Fig. 3. Clearly, $\dot{q}(x, y, z)$ is limited to the phosphor region and the LED chip, and is contributed to by the Lambertian light pattern of the light source. Therefore, the highest $\dot{q}(x, y, z)$ in the phosphor region is located on the z-axis and right above the LED chip. However, this location does not have the highest temperature. Instead, the highest temperature in the entire pc-WLED occurs at a position on the z-axis slightly further away from the LED chip and will be referred to as the hotspot in the following paragraphs. Although the thermal power density at the hotspot is about 40 times less than the LED chip, the temperature is about 50 °C higher than that of the LED chip, which is not much different from the back temperature of the substrate. By varying different parameters in the simulation, the hotspot position, hotspot temperature, and LED chip temperature can be obtained.

3.1. Influence of Different Material Parameters

Several material-related parameters have an essential influence on the hotspot temperature. In this section, a systemic study on variation in the electric driving power P_{LED}, LED wall plug

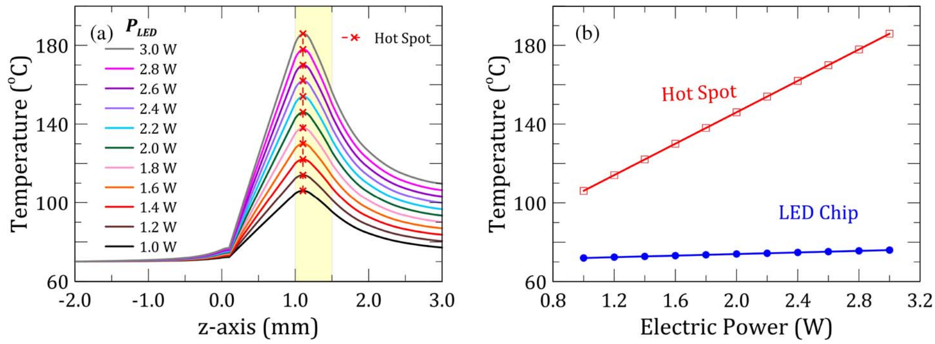

Fig. 4. (a) Temperature distribution along the z-axis and (b) hotspot temperature and LED chip temperature as P_{LED} changes.

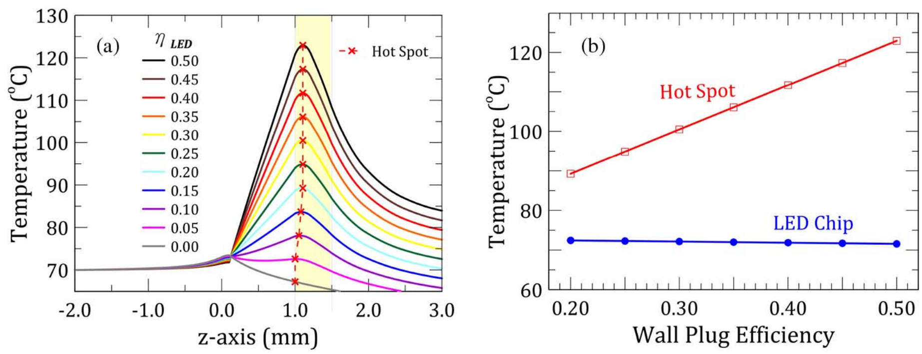

Fig. 5. (a) Temperature distribution along the z-axis and (b) hotspot temperature and LED chip temperature as η_{LED} changes.

efficiency η_{LED}, phosphor quantum conversion efficiency η_{ph}, and silicone matrix thermal conductivity k_{lens} are thoroughly discussed.

The hotspot temperature increases linearly with increments of P_{LED} as in Fig. 4. The LED chip temperature also increases linearly but the slope is much less. In other words, even if the operating temperature of the LED chip is acceptable, the temperature of the phosphor region may be much higher than the chip.

If η_{LED} increases as in Fig. 5, less heat will be generated by the LED chip itself which leads to a lower LED chip temperature. On the other hand, more blue light output implies more absorption and more heat generation within the phosphor region which results in a higher hotspot temperature.

η_{ph} directly influences the thermal power generation within the phosphor region. Therefore, a lower η_{ph} leads to the generation of more heat and a higher temperature within the phosphor region as shown in Fig. 6. Since η_{ph} can reach to more than 0.9 [13]–[15], the scanning range in the simulation is from 0.8 to 1.0.

k_{lens} is the most important material parameter influencing the temperature of the phosphor region (see Fig. 7). In practice, k_{lens} can reach 3 W/m·K with the addition of high thermal conductive fillers [6]. However, such silicone matrix is not transparent so it does not serve an optical purpose as a lens in pc-WLEDs. A transparent silicone matrix usually has a k_{lens} of less than 0.2 W/m·K which makes a high temperature in the phosphor region inevitable. The phosphor particles can be considered as the filler in the silicone matrix. The thermal conductivity of the phosphor region, k_{ph}, should be slightly higher than the transparent silicone matrix, as suggested in [9]. The thermal conductivity of the phosphor region calculated with the phosphor concentration used in this work is still less than 0.20 W/m·K which makes the hotspot temperature

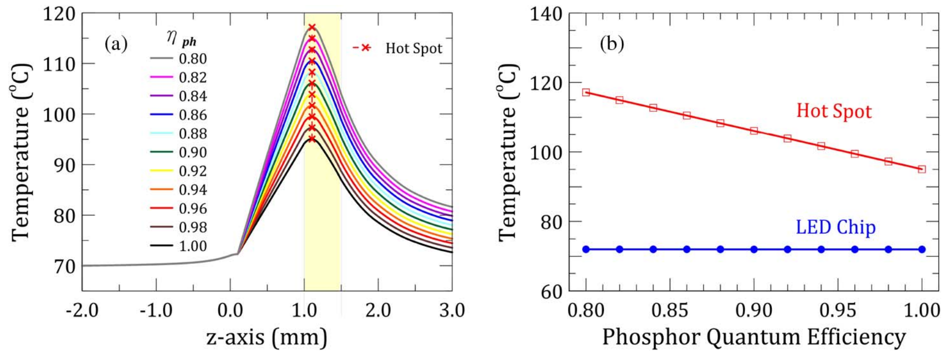

Fig. 6. (a) Temperature distribution along the z-axis and (b) hotspot temperature and LED chip temperature on as η_{ph} changes.

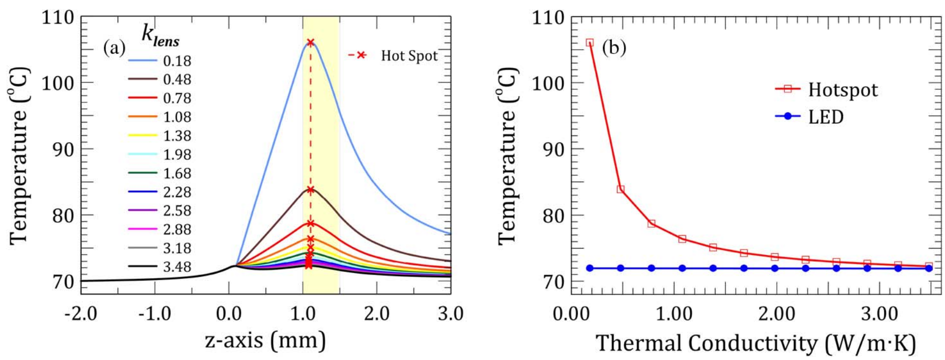

Fig. 7. (a) Temperature distribution along the z-axis and (b) hotspot temperature and LED chip temperature as k_{lens} changes.

only about 1 °C lower than that obtained in previous simulations using the parameters given in Table 1. Therefore, the simulation results are still valid and plausible.

The hotspot is located on the z-axis, slightly higher than the inner radius of the phosphor dome and does not change noticeably with these parameters.

Using (8) and (5), the heat diffusion equation in the phosphor region can be written as

$$k_{ph}\nabla^2 T + \alpha_{ph}\cdot\frac{v_B-\eta_{ph}v_Y}{v_B}\cdot\frac{P_{\text{LED}}\eta_{\text{LED}}\cos\theta}{\pi r^2}\exp\left[-\alpha_{ph}\cdot(r-r_i)\right] = \rho c_p\frac{\partial T}{\partial t}. \tag{10}$$

Clearly, the maximum temperature in the phosphor region is proportional to P_{LED}, η_{LED}, $(v_B-\eta_{ph}v_Y)/v_B$, and $1/k_{ph}$ under a steady-state condition, which agrees well with the simulation results.

3.2. Influence of the Geometrical Parameters

In the RDPP geometry, the thickness, d_{ph}, and the inner radius of the phosphor dome, r_i, are the two parameters that can be changed. To make a fair comparison, the total absorbed blue light is fixed in the simulation. In other words, the product of α_{ph} and d_{ph} is set to be 1.50, which roughly corresponds to an output CCT of 6500 K. This condition also implies that Q_{ph} is a constant, regardless of the change of geometry parameters. Fig. 8 shows the hotspot temperature versus the hotspot position for different d_{ph} from 0.1 to 0.5 mm and different r_i. Since r_i can be less than 1 mm, ray-tracing approach was use to obtain $\dot{q}(x,y,z)$. As the previous simulation shows, the hotspot position can roughly be considered as the r_i of the phosphor region. With the same r_i, a smaller d_{ph} gives a higher hotspot temperature due to the higher $\dot{q}(x,y,z)$. As r_i increases, the hotspot temperature drops because of the gradual reduction of $\dot{q}(x,y,z)$ in the

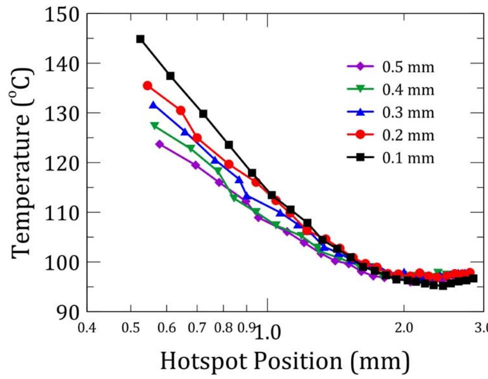

Fig. 8. Hotspot temperature versus hotspot position for different thicknesses of the phosphor dome.

phosphor region since less light is absorbed by the unit phosphor volume. In short, increasing the volume of the phosphor region can effectively reduce $\dot{q}(x, y, z)$ and result in a lower hotspot temperature. The hotspot temperature levels off when r_i reaches half of the radius of the silicone lens R_{lens}. However, the hotspot temperature is still about 25 °C higher than that of the LED chip. When the phosphor region moves to the very edge of the silicone lens, the major cooling mechanism for the phosphor region is free convection from the exterior surface of the silicone lens. Therefore, a smaller d_{ph} keeps the hotspot closer to the exterior surface and results in better cooling. However, the temperature difference is not significant. The drawback of moving the phosphor region further away from the LED chip is that the total amount of phosphor needed increases roughly proportional to r_i^2 for a fixed d_{ph}.

These simulation results suggest that the highest temperature in an RDPP pc-WLED fabricated using typical material and physical parameters is almost always in the phosphor region. The hotspot temperature can easily be several dozen degrees higher than that of the LED chip temperature. From the material stand point, the most effective way to reduce the hotspot temperature is to increase k_{lens}. However, the transparent silicone does not have high thermal conductivity. Changing the phosphor and silicone matrix to phosphor glass or ceramic [16] may be an alternative solution to increase k_{lens} and k_{ph}. Increasing η_{ph} can also reduce the hotspot temperature. However, η_{ph} has reached more than 0.9 which makes further improvement of η_{ph} rather limited. Geometrical parameters can be practically adjusted much more easily. Increasing d_{ph} can effectively reduce $\dot{q}(x, y, z)$, which results in a lower hotspot temperature. Moving the phosphor region away from the LED chip can also reduce $\dot{q}(x, y, z)$ within the phosphor region since less light is absorbed by the unit phosphor volume.

3.3. Temporal Behavior of the Hotspot Temperature in pc-WLEDs

With the knowledge of the specific heat capacity and density of each material, the temporal behavior of $T(x, y, z, t)$ in pc-WLEDs can also be evaluated using an FEA simulation. Fig. 9 shows the temperature at the surface of the LED chip and the hotspot in the phosphor region as functions of time if the initial temperature of the entire pc-WLED is set to be 70 °C. Clearly, the LED chip reaches thermal equilibrium after 0.02 sec. However, the phosphor region takes about 1 min to reach a steady state. If the initial temperature is 25 °C, the final substrate temperature is 100 °C, and the P_{LED} is 1.5 W, and a similar temperature curve can be obtained, as shown in Fig. 10. The pc-WLED requires about 3 min to reach thermal equilibrium.

4. Experiment

To the best of our knowledge, the $T(x, y, z)$ within a pc-WLED has yet to be measured directly in any practical way. To validate the simulation results, an experiment which allows direct measurement of $T(x, y, z)$ is required. Thus, in this study, a pc-WLED in RDPP was built using the

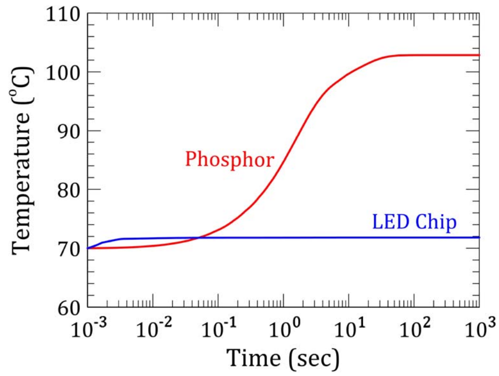

Fig. 9. Temperature of the LED chip and phosphor hotspot varies as a function of time. LED chip temperature reaches thermal equilibrium after less than 0.02 sec, yet the phosphor region takes about 1 min.

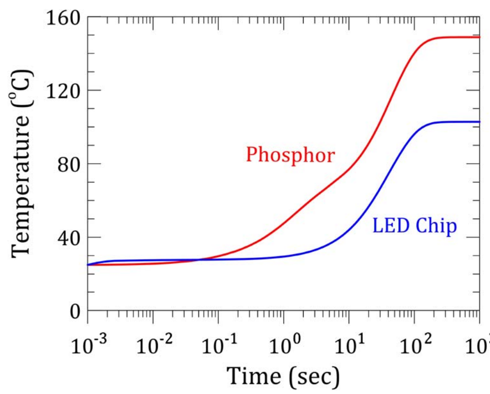

Fig. 10. pc-WLED has a P_{LED} of 1.5 W and an initial temperature of 25 °C. Temperature of the LED chip and the phosphor hotspot varies as a function of time after turn on. The entire pc-WLED takes about 3 min to reach thermal equilibrium.

parameters in Table 1. The phosphor used in the phosphor region was Ce:YAG with 15 wt.%. The average CCT of this pc-WLED is about 6500 K when operated at a substrate temperature of 25 °C with a driving current of 50 mA. When the operating current of this pc-WLED is higher than 450 mA with the corresponding input electric power of 1.5 W, the substrate temperature rises to 100 °C and the average CCT reaches 7900 K. The later operating condition matches those used in the simulation as shown in Fig. 10. The entire pc-WLED took more than 5 min to reach thermal equilibrium which roughly agrees with the aforementioned simulation. However, the temperature within the RDPP pc-WLED could not be measured directly. Therefore, the entire silicone lens, including the phosphor region, was cut in half along the symmetry plane of the entire package, as shown in Fig. 11(a). A side view image of the sample is shown in Fig. 11(b). This pc-WLED then served as the sample for testing. As shown in Fig. 11(c), the temperature distribution on the cut surface of the sample was measured by a thermal camera (NEC Avio TVS-500EX) with a close-up lens (TVM-7025U) which has spatial resolution of 18.5 μm. The emissivity was set to be 0.95 which was calibrated by a silicone thin plate with temperature measured by a thermocouple calibrator (Fluke 714). The LED chip temperature is about 48 °C. A simulation using the theoretical approach and the FEA method is performed utilizing the same parameters as those mentioned above, except that P_{LED} is set to 1.5 W and the substrate temperature is set to 48 °C to match the experimental conditions. The simulated $T(x, y, z)$ of the sample is shown in Fig. 11(d). The simulation results match the experimental results very well.

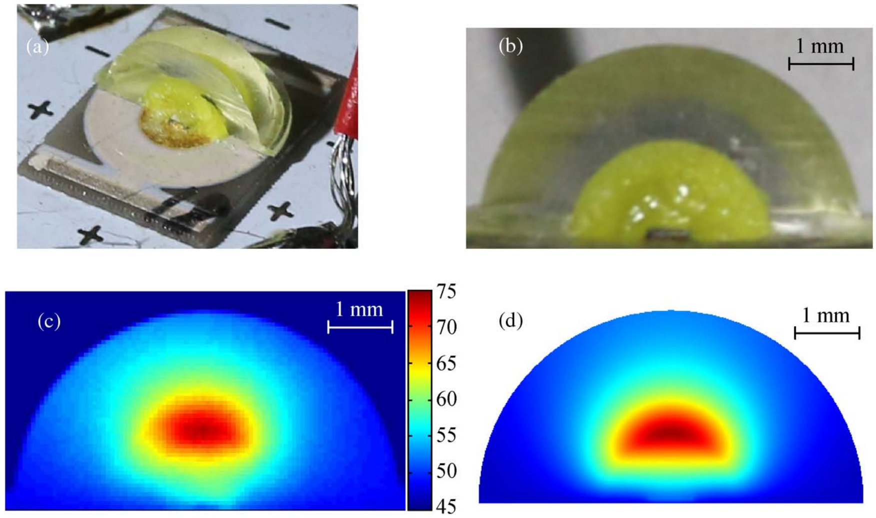

Fig. 11. Sample tested is a cut-in-half RDPP pc-WLED. (a) Angled visible image of the sample. (b) Image of the cut surface of the sample. (c) Thermal image of the cut surface of the sample. (d) Simulated temperature distribution of the sample. (b)–(d) are in scale and the length scale, indicates 1 mm. (c) and (d) share the same temperature color scale with in units of °C.

5. Optical Effects and Discussion

Thermal quenching is an inevitable effect for phosphors [17], and η_{ph} decreases as the phosphor temperature increases. Using the data in Fig. 2 of [17], the η_{ph} of YAG:Ce^{3+} phosphors can be estimated. Thermal quenching of the phosphor region will lead to a reduction in the number of converted photons in the phosphor which results in a drop in the luminescence and an increase in the CCT in pc-WLEDs. The high temperature region coincides with the phosphor region with larger blue irradiation. Therefore, the CCT of this region will gradually increase after the pc-WLED is turned on. As predicted in Fig. 10, the pc-WLED requires 3 min to reach thermal equilibrium, as do the output optical properties. Furthermore, $T(x, y, z)$ of the phosphor region will also lead to angular CCT deviation (ACCTD). The simulation results illustrated in Fig. 10 show that the temperature difference between the LED chip and the phosphor hotspot can reach about 50 °C after reaching thermal equilibrium. As can be seen in Fig. 11(c) and (d), the phosphor region directly in contact with the substrate has the same temperature as the substrate. In other words, the temperature difference within the phosphor region also reaches about 50 °C. For a pc-WLED with a chip temperature of 100 °C, the yellow light output due to the nonuniform $T(x, y, z)$ of the phosphor may vary by about 5% over the observation angle. Such variation can cause an ACCTD in a 6500 K pc-WLED to reach 66 K. For pc-WLEDs using other phosphors with larger thermal quenching, a much larger CCT variation may be observed. Regardless of the influence on the CCT, there is a drop of the total output power and lumens as the phosphor heats up. However, the wall plug efficiency of the LED chip is also a function of temperature. The complete spectral-thermal behavior of a pc-WLED is nonlinear and is beyond the scope of this work.

If carbonization or discoloration happens in the phosphor region [8], [18], α_{ph} will increase, but η_{ph} will drop dramatically in the phosphor region. A preliminary simulation suggests the hotspot temperature could easily reach 150 °C higher than the LED chip. Such an effect may lead to severe cracking and/or even more severe discoloration. According to a supporting document from Cree Inc. it is suggested that discoloration is caused by the intrusion of incompatible volatile organic compounds (VOCs) in the pc-WLED operation environment and the discoloration is reversible [19]. How the discoloration relates to temperature requires further investigation.

6. Conclusion

The phosphor region is a non-negligible heat source in pc-WLEDs. Theoretical and simulation approaches are used to obtain the temperature distribution within the phosphor region of remote dome phosphor packaged pc-WLEDs. Good agreement between these and test results have been reached. Due to the small thermal conductivity of the silicone matrix, the highest temperature in this type of pc-WLED is almost always in the phosphor region and could reach several dozen degrees higher than in the LED chip. The influence of different material and geometric parameters is also studied thoroughly. An experiment was performed to measure the temperature distribution in a pc-WLED. The results agree well and confirm the simulation results. As the phosphor temperature increases, the phosphor quantum conversion efficiency drops, leading to changes in the output spectrum with time and with the observation angle. Temperature variation over the pc-WLED may also introduce stress which could even result in mechanical failure of the silicone matrix. Choosing the phosphor and silicone matrix with higher thermal conductivity or using phosphor with better quantum conversion efficiency can effectively reduce the temperature of the phosphor of a pc-WLED from the stand point of material. Extending the inner radius or the thickness of the phosphor region in a remote dome phosphor packaged pc-WLED can also reduce the phosphor temperature. Therefore, the thermal management of the phosphor region should be considered for advanced pc-WLED packages.

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