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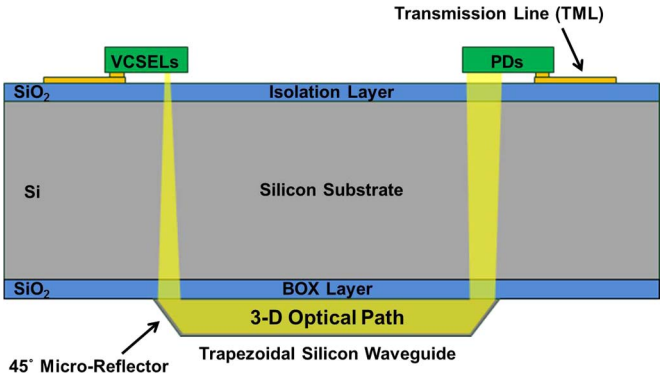

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Implementation of Chip-Level Optical Interconnect With Laser and Photodetector Using SOI-Based 3-D Guided-Wave Path

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Abstract: A chip-level optical interconnect module combined with a vertical-cavity surface-emitting laser (VCSEL) chip, a photodetector (PD) chip, a driver integrated circuit (IC), and an amplifier IC on a silicon-on-insulator (SOI) substrate with 3-D guided-wave paths is experimentally demonstrated. Such an optical interconnect is developed for the signal connection in multicore processors or memory-to-processor interfaces. The 3-D guided-wave path, consisting of silicon-based 45° microreflectors and trapezoidal waveguides, is used to connect the optical signal between transmitter and receiver. In this paper, the VCSEL and PIN PD chips are flip-chip integrated on a SOI substrate to achieve complete chip-level optical interconnects. Due to the unique 3-D guided-wave path design, a higher laser-to-PD optical coupling efficiency of -2.19 dB and a larger alignment tolerance of ± 10 μm for the VCSEL/PD assembly are achieved. The measured laser-to-PD optical transmission efficiency can reach -2.19 dB, and the maximum optical power and threshold current of VCSEL is 3.27 mW and 1 mA, respectively. To verify the data transmission, the commercial driver IC and amplifier IC are assembled upon the silicon chip, and the error-free data transmission of 10 Gbps can be achieved when the VCSEL is operated at the driving current of 9 mA.

Index Terms: Optical interconnects, optical waveguides, micromirrors, 3-D guided-wave path.

1. Introduction

The data rate of chip-level interconnects, in multi-core processor and memory-to-processor interfaces, is increasing rapidly. Chip-level electrical interconnects face challenges in increasing wire density and limitations in bandwidth density, energy dissipation, and crosstalk noise due to the nature of metal wires [1]–[3]. Optical interconnects based on silicon-on-insulator (SOI) substrate is expected to be a potential alternative for solving these bottlenecks due to the benefits in interconnect density, energy dissipation, and timing [4]. Over recent years, there have been extensive investigations in chip-level optical interconnects [5]–[14], including laser light sources [5]–[7], modulators [8]–[10], waveguides [11], [12], and photodetectors (PDs) [13], [14].

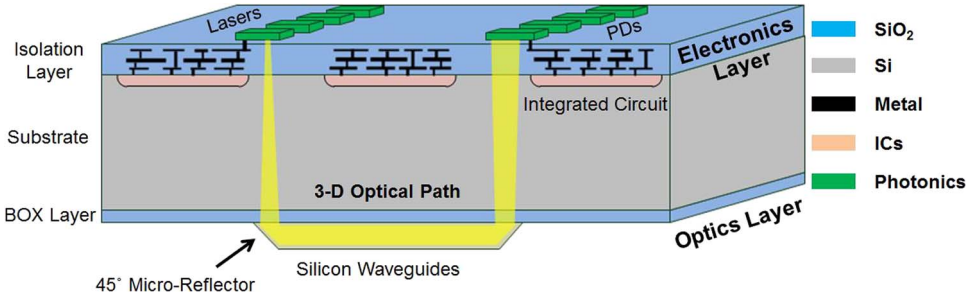

Fig. 1. The concept of SOI-based chip-level optical interconnect module with lasers and photodetectors using 3-D guided-wave path for multi-core processor or memory-to-processor interface.

However, the major drawback of silicon-based optical interconnects is the lack of efficient, compact, and cost-effective light sources and PDs due to the indirect bandgap of silicon [15], [16].

To achieve complete and efficient chip-level optical interconnects with laser sources and PDs, silicon photonics combined with III/V material-based lasers and PDs is a viable option because of the benefits of III/V materials in light emission, higher speeds, and efficient light detection at near-infrared wavelengths. Heterogeneous integration [17], [18] and off-chip assembly [19]–[21] methods are generally used to integrate III/V materials on the silicon chip. In the heterogeneous integration, III/V material is heterogeneously integrated on the silicon chip using molecular wafer bonding or divinylsiloxane-benzocyclobutene (DVS-BCB) adhesive wafer bonding. The photonics device can be fabricated on a silicon chip and placed in close proximity to the silicon waveguides without critical alignment [22]. The evanescent wave coupling is typically used to couple lightwaves between the III/V material and waveguides. Several chip-level optical interconnects using III/V material heterogeneous integration have been investigated [17], [18]. However, in these approaches, the power consumption and laser optical power would be a concern for real chip-level optical-interconnects. In the off-chip assembly, the laser diode possesses low power consumption, high laser output power and stable lasing operation at high temperatures. It can be assembled upon silicon chip using active or passive alignment technique [23]. Generally, the butt-joint coupling with spot-size converters (SSC) [19], [21] or micro-lens [20] is used to couple lightwave between off-chip devices and waveguides. However, the small alignment tolerance and optical coupling efficiency would be a concern for cost-effective and mass produced chip-level optical interconnects. Therefore, an efficient approach to integrate the lasers and PDs into chip-level optical interconnects is demanded, especially in the viewpoint of power consumption, optical coupling efficiency, and device assembly.

In order to improve the performance of chip-level optical interconnects, the 3-D guided-wave path is developed to integrate laser and PD into a silicon chip. Such 3-D guided-wave path can be used in multi-core processor or memory-to-processor interface, as shown in Fig. 1. Such SOI-based optical interconnect module consists of 3-D guided-wave paths, electronics layer, and optics layer components. In the electronics layer, integrated circuits (ICs) can be fabricated using a standard CMOS process, and the III/V material device, such as directly modulated lasers and PDs, is flip-chip bonded upon electronics layer. The off-chip photonics device can significantly reduce the power consumption of whole systems due to the lower operation current and higher laser optical power. In the optics layer, the silicon-based 45° micro-reflectors and trapezoidal waveguides are fabricated using a single-step wet-etching process [24], [25]. The 3-D guided-wave path is utilized to connect the optical signal between transmitter and receiver. It provides a large alignment tolerance and a high optical coupling efficiency for the device assembly. Moreover, the 3-D guided-wave path also simplifies and facilitates the chip-level optical interconnect of devices located on a SOI substrate, even the optical interconnection realized within a very compact region. In this paper, we experimentally demonstrate the complete chip-level optical interconnect integrated with laser and PD. Furthermore, driver IC and amplifier IC chips are assembled upon the electronics layer using die-attach process to demonstrate the

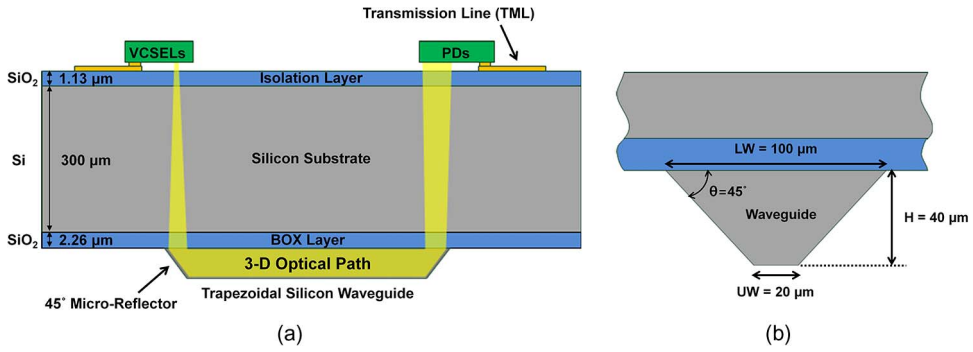

Fig. 2. (a) The schematic cross-section of 3-D guided-wave path for the proposed chip-level optical interconnect. (b) The schematic cross-section of silicon trapezoidal waveguide.

data transmission at 10-Gbps. The optical and electrical characteristics are given to verify the performance of the proposed chip-level optical interconnects.

2. Optical Design of Chip-Level Optical Interconnect With VCSEL and PD

In this paper, we focus on the development of 3-D guided-wave path to integrate the laser and PD into the chip-level optical interconnects. A schematic cross section of the 3-D guided-wave path is given in Fig. 2(a). The 1310-nm single-mode VCSEL, manufactured by BeamExpress, is adopted as a light source, and a PIN PD with responsivity of 0.9 A/W at 1310-nm, manufactured by Albis, is utilized to receive the optical signals. In the transmitter, the laser beam emitting from VCSEL chip passes through the SiO_2 isolation layer, silicon substrate, SiO_2 buried oxide (BOX) layer, and then deflects into the trapezoidal silicon waveguide by 45° micro-reflector. In the receiver, the laser beam impinges upon the 45° micro-reflector and reflects into the sensing area of PD chip. From the interference theory, the thickness of isolation layer and BOX layer is designed as 1.13 μm and 2.26 μm, respectively, to enhance the transmittance at 1310 nm. In practice, the silicon substrate is thick enough so that the front and rear plane of silicon substrate are not perfectly parallel due to the CMP process and wafer warp. Furthermore the laser beam has a divergent angle of 2.6° in silicon substrate. When the laser beam propagates three trips of silicon substrate, the spot size of laser beam is expanded from 15 μm to 96 μm, which is larger than the silicon waveguide dimension. Based on these reasons, the interference effects caused by the silicon substrate could be ignored, and the laser beam in the silicon substrate may be treated in the limit of simple geometrical optics [26]. Therefore, the thickness of isolation layer and BOX layer can be separately designed to reduce reflection. In the transmitter, the total transmittance for these two dielectric thin films is -0.29 dB theoretically. In order to increase the optical coupling efficiency between the device and waveguide, the thickness of silicon substrate is polished to 300 μm. Fig. 2(b) shows the cross-section of silicon trapezoidal waveguide. The silicon waveguides and 45° micro-reflectors are simultaneously fabricated using a single-step wet-etching process, which causes the trapezoidal shape and 45° sidewall angle (θ). A waveguide height (H) of 40 μm was determined by the waveguide layer thickness of SOI substrate. The upper waveguide width (UW) and lower waveguide width (LW) are designed as 20 and 100 μm, respectively.

Fig. 3 shows the simulation result of light-propagation in the proposed optical interconnects by ray-tracing method. In this simulation model, the refractive indices of Si and SiO_2 are 3.5072 and 1.4468, respectively. A Gaussian-distributed laser beam with a wavelength of 1310 nm, spot size of 15 μm in diameter, and half divergent-angle of 9° serves as single-mode VCSEL light source at the transmitter. The laser beam emits into the SiO_2 isolation layer and passes through silicon substrate. In the silicon substrate, the half divergent angle of laser beam is reduced from 9° to 2.6° due to the refractive index difference between air and silicon. The shorter optical path and smaller divergence angle in the silicon substrate allow most of the laser beam

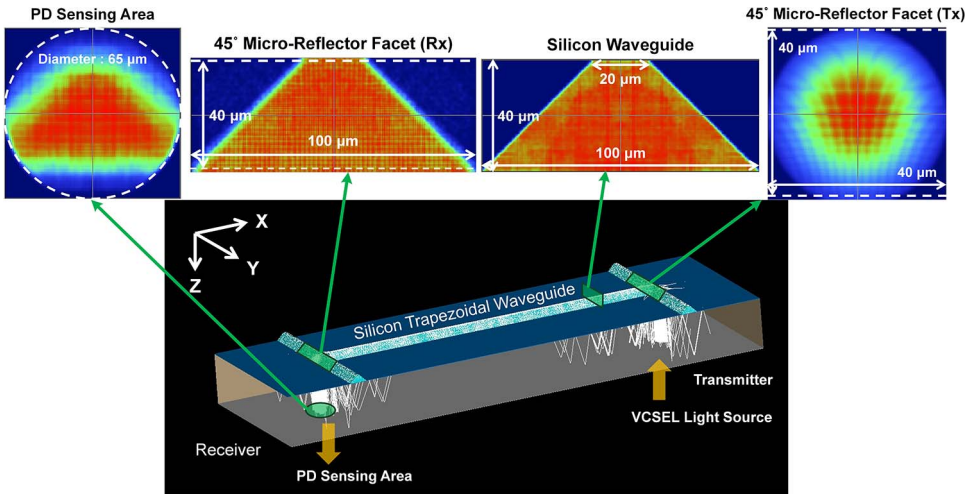

Fig. 3. The simulated light-propagation in the proposed SOI-based chip-level optical interconnect by ray-tracing method.

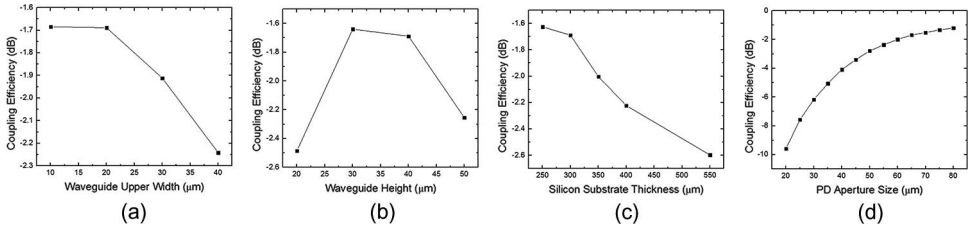

Fig. 4. The simulated VCSEL-to-PD optical coupling efficiency for the proposed chip-level optical interconnect. (a) The optical coupling efficiency as a function of waveguide upper width. (b) The optical coupling efficiency as a function of waveguide height. (c) The optical coupling efficiency as a function of silicon substrate thickness. (d) The optical coupling efficiency as a function of PD sensing area.

to be deflected into the silicon trapezoidal by the 45° micro-reflector. The laser beam is confined within the trapezoidal waveguide due to the large refractive index difference between core and cladding. In the receiver, the laser beam is reflected into the output port by the 45° micro-reflector, and a sensing area with an aperture diameter of 65 μm is located at the output port to receive the optical power. From the simulation result, the VCSEL-to-PD optical coupling efficiency is -1.69 dB without any lens element. In the transmitter, the total transmission loss of two dielectric layers, including isolation layer and BOX layer, is 0.29 dB. The waveguide coupling loss is 0.17 dB. In the receiver, the total transmission loss of two dielectric layers is also 0.29 dB, and the PD coupling loss is 0.94 dB. In this calculation, we didn't consider the waveguide propagation loss. Based on the above breakdown of total transmission loss, the largest transmission loss is come from the geometrical size mismatch between the trapezoidal waveguide and PD sensing area.

For the 3-D guided-wave path, the waveguide height (H), waveguide upper width (UW), silicon substrate thickness, and the size of PD sensing area are simulated to study the effect of these parameters on the VCSEL-to-PD optical coupling efficiency. The impact of the waveguide upper width on the optical coupling efficiency is examined, as shown in Fig. 4(a). In this simulation, the silicon substrate thickness and waveguide height are defined as 300 and 40 μm, respectively. The coupling efficiency decreases from -1.68 dB to -2.24 dB when upper width is adjusted from 10 μm to 40 μm, and there is a rapidly decay when upper width is larger than 20 μm. Fig. 4(b) shows the VCSEL-to-PD optical coupling efficiency as a function of waveguide

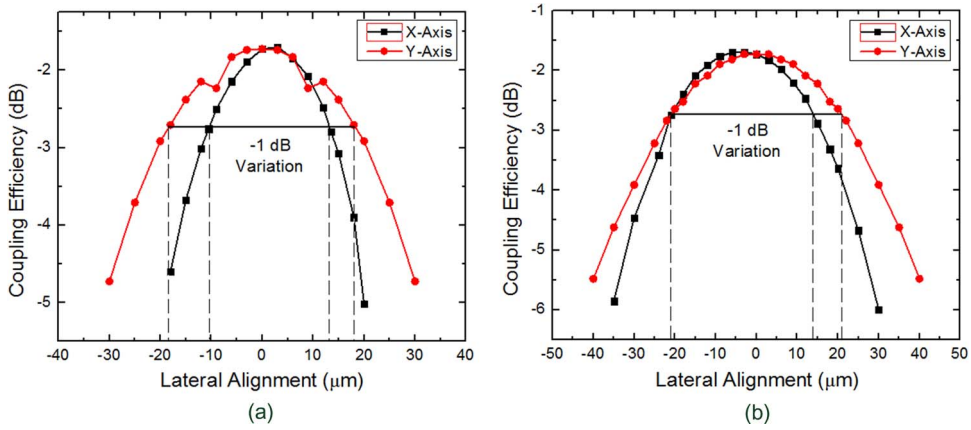

Fig. 5. The simulated VCSEL-to-PD optical coupling efficiency for proposed chip-level optical interconnect. (a) Alignment tolerance of the VCSEL. (b) Alignment tolerance of the PD.

height. The substrate thickness and waveguide upper width are 300 and 20 μm, respectively. A coupling efficiency of -1.64 dB can be observed at waveguide height of 30 μm. Fig. 4(c) shows the optical coupling efficiency as a function of silicon substrate thickness. In this simulation, the waveguide height and upper width are fixed as 40 μm and 20 μm, respectively. The optical coupling efficiency decreases from -1.63 dB to -2.6 dB when the substrate thickness increases from 250 μm to 550 μm. The coupling loss is come from the mode size mismatch between devices (VCSEL/PD) and waveguides. Fig. 4(d) shows the VCSEL-to-PD optical coupling efficiency as a function of PD sensing area in diameter. Considering the commercial 25-Gbps PIN PD with an aperture diameter of 25 μm and responsivity of 0.9 A/W, the VCSEL-to-PD optical coupling efficiency can keep around -7.57 dB, and the corresponding photocurrent is 0.29 mA when VCSEL output optical power is 1.82 mW. Such magnitude of photocurrent is still enough to achieve error-free data transmission at 25-Gbps. From these simulation results, larger waveguide height and upper width have larger optical coupling efficiency in transmitter, but it leads to more rapidly decrease in receiver due to mismatch of geometrical size between waveguide and PD sensing area. However, it can be improved by tapering the waveguide upper width down at receiver side so that the waveguide size can match with the PD sensing area.

Considering the optical power loss due to misalignment of VCSEL/PD assembly, the alignment tolerance of VCSEL and PD flip-chip bonding is investigated, as shown in Fig. 5(a) and (b). Without any misalignment in the device assembly, the simulated VCSEL-to-PD optical coupling efficiency is -1.69 dB. In the transmitter, the alignment tolerances of 1 dB excess loss for VCSEL assembly are ± 10 and ± 18 μm, respectively, at the X- and Y- directions. In the receiver, the alignment tolerances of 1 dB excess loss for PD assembly are ± 14 and ± 21 μm, respectively, at the X- and Y- directions. From the simulation results, the proposed 3-D guided-wave path has wide alignment tolerance for the off-chip device assembly and higher VCSEL-to-PD optical coupling efficiency of -1.69 dB. It is suitable for cost-effective and mass-production chip-level optical interconnects.

3. Realization of Chip-Level Optical Interconnect With VCSEL and PD

Fig. 6 shows the complete chip-level optical interconnect. It consists of a 3-D guided-wave path, VCSEL, PD, driver IC, and amplifier IC components. Such optical interconnect are realized on the (100) orientation-defined SOI wafer in which the thicknesses of silicon substrate and waveguide layer are 550 and 40 μm, respectively. Four fabrication steps including 3-D guided-wave path, transmission line, VCSEL/PD flip-chip bonding, and IC assembly are described as follows.

In the fabrication process of the 3-D guided-wave path, the silicon-based 45° micro-reflectors and trapezoidal waveguides are simultaneously fabricated on the waveguide layer of SOI wafer

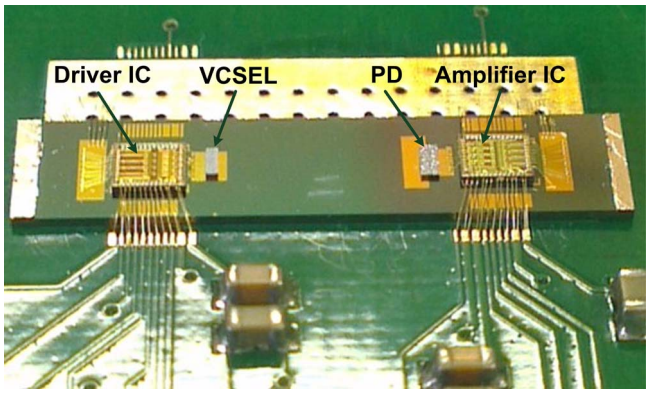

Fig. 6. The photograph of complete chip-level optical interconnect, including 3-D guided-wave path, VCSEL, PD, driver IC, and amplifier IC. The whole system is assembled on a PCB to demonstrate the data transmission.

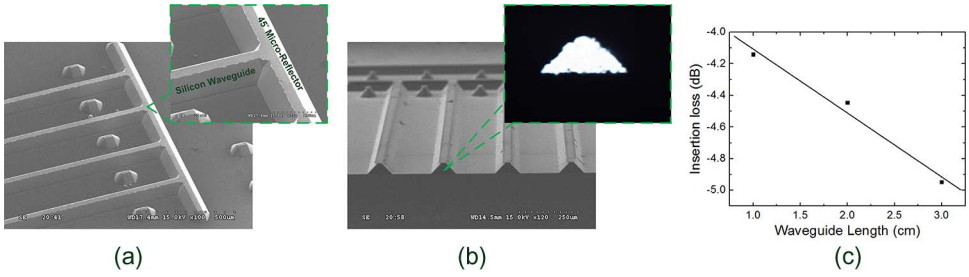

Fig. 7. (a) The SEM image of fabricated 45° micro-reflectors and trapezoidal waveguides. (b) The cross-section of silicon trapezoidal waveguides, the inset shows the light pattern at end facet of trapezoidal waveguide. (c) The measured propagation loss of straight trapezoidal waveguide using cut-back method.

using a single anisotropic wet etching process in a potassium hydroxide (KOH) and isopropyl alcohol (IPA) solution [24]. Fig. 7(a) shows the scanning electron microscopy (SEM) image of the fabricated 45° micro-reflectors and trapezoidal waveguides. The root-mean-square (RMS) surface roughness of silicon 45° micro-reflector and trapezoidal waveguides sidewall can be less than 30 nm as a high-quality optical mirror for the 1310-nm lightwave. The cross-section of the silicon trapezoidal waveguides is also demonstrated in the Fig. 7(b). The BOX layer, with thickness of 2.26 μm, serves as lower cladding. The measured trapezoidal waveguide height (H), upper width (UW), lower width (LW), and sidewall angle (θ) are 40.1, 20.1, 99.6 μm, and 45.25°, respectively. The total waveguide length is 6 mm. The inset of Fig. 7(b) shows the measured light pattern at end facet of the trapezoidal waveguide. The laser beam can be well confined within trapezoidal waveguide due to large refractive index difference between waveguide core and cladding. Fig. 7(c) shows the insertion loss versus waveguide length. A propagation loss of 0.404 dB/cm is achieved at 1310 nm. Considering the waveguide length of 6 mm, the waveguide loss is approximately 0.242 dB. In order to reduce the thickness of silicon substrate from 550 to 300 μm, the chemical-mechanical-polishing (CMP) process is used to polish the rear side of silicon substrate. After the polish process, the measured silicon substrate thickness is 313 μm, and the surface roughness of silicon substrate can be controlled within ± 2 μm.

In the fabrication processes of transmission line and VCSEL/PD flip-chip bonding, a SiO_2 thin-film with thickness of 1.12 μm is deposited upon the rear side of silicon substrate as an isolation layer by inductively coupled plasma chemical vapor deposition (ICP CVD). In order to connect the electrical signal between IC and VCSEL/PD, the Au transmission line with thickness of 2.23 μm is deposited upon the isolation layer using electron-gun (E-gun) evaporation, and

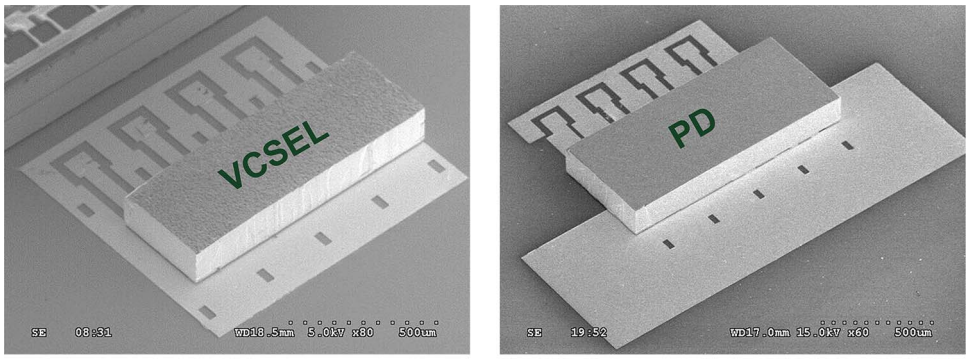

Fig. 8. (a) The SEM image of (a) VCSEL and (b) PD chip flip-chip bonded upon the Au transmission line using a high-accuracy flip-chip bonder.

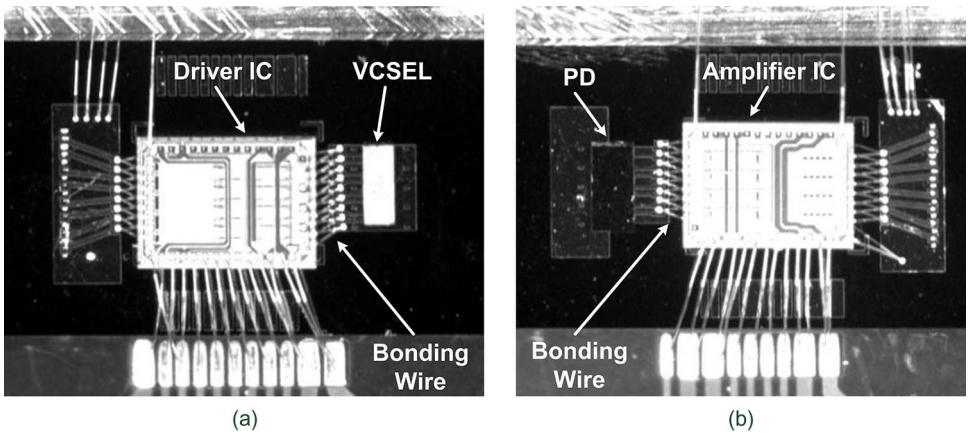

Fig. 9. The microphotograph of (a) transmitter and (b) receiver. The driver IC and amplifier IC are assembled onto the silicon chip using die-attach process. The bonding wire is used to connect the electrical signal between IC and transmission line.

the double side aligner is used to align the transmission line with 45° micro-reflectors. For the VCSEL/PD flip-chip bonding, the Au/Sn solder bump with a thickness of 2.85 μm is patterned on the transmission line to connect VCSEL/PD and transmission line. Then, the VCSEL/PD chip is aligned with matching Au/Sn solder bumps and bonded upon the transmission line using a high-accuracy flip-chip bonder, as shown in Fig. 8.

To demonstrate the data transmission, a commercial driver IC and amplifier IC are assembled onto the silicon chip using die-attach process, as shown in Fig. 9. The IC and Au transmission line are linked together through the bonding-wires with minimum bonding wire length. It helps to reduce electrical reflection loss at high frequency. Finally, the whole optical interconnect chip is assembled on a printed circuit board (PCB) using chip-on-board (COB) package technique, and the pads for driver IC and amplifier IC are wire bonded to a PCB with DC bias and control signals.

4. Characterization of Chip-Level Optical Interconnect With VCSEL and PD

4.1. Optical Characterization of Chip-Level Optical Interconnect With VCSEL and PD

The optical characterization of proposed chip-level optical interconnect is measured, including L-I-V curves of VCSEL and PD as well as VCSEL-to-PD optical coupling efficiency. Fig. 10(a)

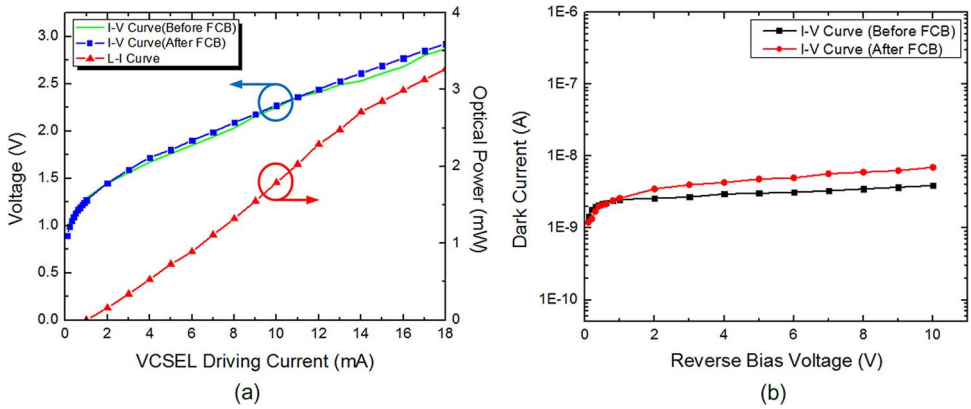

Fig. 10. (a) The measured L-I-V curve for VCSEL chips after flip-chip bonding (FCB). (b) The measured I-V curve for flip-chip bonded PD chips with responsivity of 0.9 A/W.

shows the measured L-I-V curve for VCSEL chips after flip-chip bonding (FCB), the threshold current and slope efficiency is 1 mA and 0.2 W/A, respectively, and the maximum optical power from VCSEL is 3.27 mW. Comparing the performance of I-V curve before and after flip-chip bonding, there is no obviously degradation in threshold current and slope efficiency by flip-chip bonding. Fig. 10(b) shows the measured I-V curve for flip-chip bonded PD chips with responsivity of 0.9 A/W. The measured dark current is 2.57 nA at reverse bias voltage of 1.7 V. Comparing the dark current before and after flip-chip assembling, the dark current increases from 2.57 to 3.2 nA at reverse bias voltage of 1.7 V due to the flip-chip bonding process. However, the slightly increasing in dark current is negligible compared to the signal level of several microampere in the proposed chip-level optical interconnect.

In order to measure the VCSEL-to-PD optical coupling efficiency, the flip-chip bonded VCSEL is biased at 10 mA and the corresponding laser output power is 1.82 mW. In the flip-chip bonded PD, the reverse bias voltage is 1.7 V, and the received photocurrent is 0.99 mA. Considering the PD responsivity of 0.9 A/W, the VCSEL-to-PD optical coupling efficiency is -2.19 dB.

4.2. Dynamic Characterization of Chip-Level Optical Interconnect With VCSEL and PD

To confirm the dynamic characterization of proposed optical interconnect with VCSEL and PD, the small-signal frequency response as a function of VCSEL bias currents ranging from 6 to 14 mA is measured without any driver IC and amplifier IC. In this measurement, the reverse bias voltage of the PD is fixed at 1.7 V. The modulated signal from the vector network analyzer (VNA) is applied to VCSEL via a GSG coplanar probe. The other GSG coplanar probe is used to receive the signal at the PD and fed back into the VNA. The measured small-signal frequency response is shown in Fig. 11. The resonant oscillation frequency caused from the VCSEL increases as the driving current increases. The resonant oscillation gradually becomes saturation when VCSEL driving current is larger than 10 mA. A maximum 3-dB bandwidth of 7 GHz is observed when VCSEL driving current is 10 mA. The frequency bandwidth is mainly limited by the off-chip VCSEL and PD.

The high-speed data transmission of the proposed optical interconnect with the VCSEL, PD, driver IC, and amplifier IC is verified. In the transmitter, the non-return-to-zero (NRZ) high-speed data with a pseudo-random bit sequence (PRBS) of 2^{31}-1 is applied to the driver IC via a GSG coplanar probe. Then, the driving current and modulated current from the driver IC are fed into the VCSEL. In the receiver, the data from the PD chip is amplified by the amplifier IC and fed into the sampling oscilloscope with a bandwidth of 50 GHz. The clear eye diagram at 10-Gbps is experimentally obtained, as shown in Fig. 12(a). In this measurement, the driving current and peak-to-peak modulation current of the driver IC is 9 mA and 12.5 mA, respectively, and the reverse bias voltage of the PD is 1.7 V.

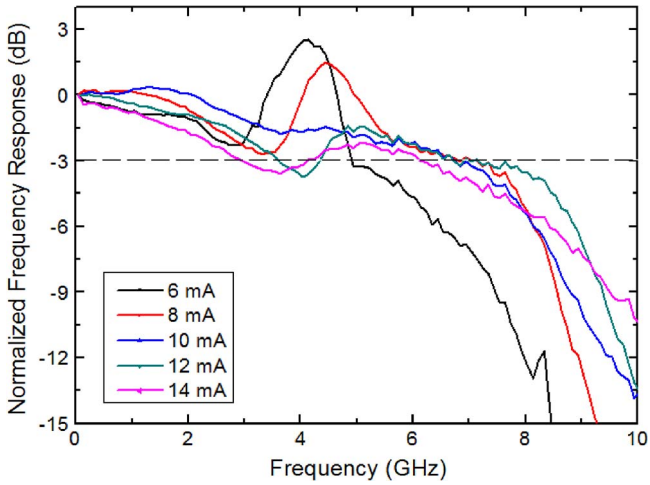

Fig. 11. The measured small-signal frequency responses for the chip-level optical interconnect with VCSEL and PD under different VCSEL driving currents. The driver IC and amplifier IC are not considered in this measurement.

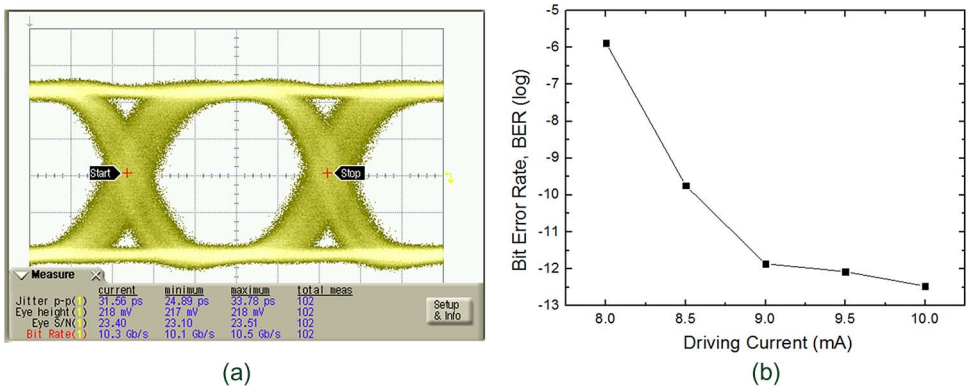

Fig. 12. (a) The measured eye diagrams of proposed chip-level optical interconnect at 10-Gbps when VCSEL driving current is 9 mA. (b) The BER testing at 10-Gbps as a function of VCSEL driving current. The BER is smaller than 10^{-12} when VCSEL driving current is larger than 9 mA.

For the bit error rate (BER) testing at 10-Gbps data rate, an error detector (ED) is used to evaluate the data-transmission. The BER testing as a function of VCSEL driving current is shown in Fig. 12(b). Compared with the different VCSEL driving currents, a BER better than 10^{-12} can be achieve when the VCSEL driving current is larger than 9 mA. According to the measured eye diagram and BER testing, the proposed chip-level optical interconnect possesses the capability to transmit data at 10-Gbps with lower laser driving current and higher laser-to-PD optical coupling efficiency. However, the data rate of the proposed optical interconnect is limited by the off-chip VCSEL and PD, it could be improved by changing to a laser/PD with a higher data rate.

5. Conclusion

In this paper, a chip-level optical interconnect combined with VCSEL and PD chips as well as driver and amplifier ICs on a SOI substrate with 3-D guided-wave paths has been experimentally demonstrated. Its optical transmission loss of −2.19 dB and a 3-dB bandwidth of 7 GHz are achieved as the VCSEL is biased at 10 mA. The clear eye diagram and error-free data transmission at 10-Gbps are also demonstrated as the VCSEL is biased at 9 mA. Those measurement

results verify that the on-chip optical interconnect could be operated with a high data rate and at a low power consumption using the proposed SOI-based 3-D guided-wave paths.

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