IEEE Photonics Journal
An IEEE Photonics Society Publication

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Volume 6, Number 5, October 2014

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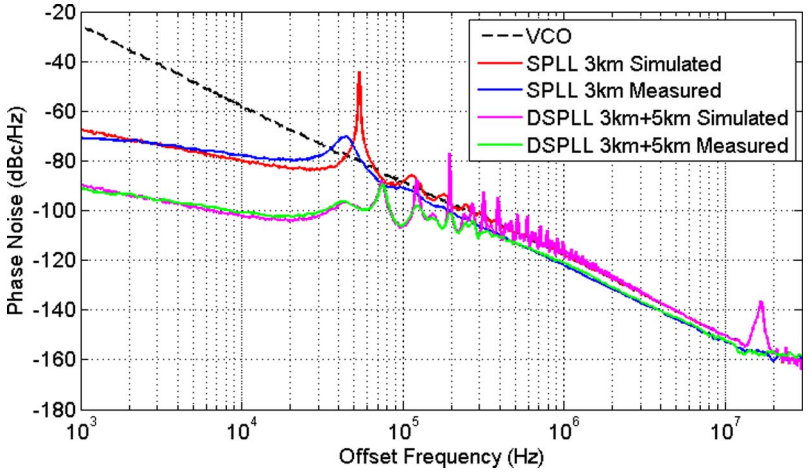

DOI: 10.1109/JPHOT.2014.2360294
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Comparison of Optical Self-Phase Locked Loop Techniques for Frequency Stabilization of Oscillators

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DOI: 10.1109/JPHOT.2014.2360294

Manuscript received August 5, 2014; revised September 4, 2014; accepted September 7, 2014. Date of publication September 25, 2014; date of current version October 7, 2014. Corresponding author: A. Daryoush (e-mail: daryoush@coe.drexel.edu).

Abstract: Self-phase locked loop (SPLL) through long optical delay lines is investigated for improving the phase noise of the optoelectronic oscillator (OEO) and the voltage-controlled oscillator (VCO). This paper features analytical modeling of close-in to carrier phase noise of oscillators employing SPLL technique using single and multiple delay loops. Experimental results are also provided to verify the analytical modeling and explore critical circuit design parameters to achieve substantial phase noise reduction. Performance comparison is presented for SPLL using electrical phase shifter, Mach–Zehnder modulator (MZM)-based phase shifting, and electrical VCO. Phase noise reduction of 65 dB at 1-kHz offset is achieved for an electrical VCO employing a dual-loop SPLL with 3- and 5-km optical fiber delay lines, whereas the phase locking based on MZM and electrical phase shifter provided 20- and 38-dB reductions at 1-kHz offset for an OEO, respectively.

Index Terms: Optoelectronic oscillator (OEO), phase locked loop (PLL), self-phase locked loop (SPLL), dual loop SPLL (DSPLL), fiber optic link (FOL), voltage controlled oscillator (VCO), spurious side-modes.

1. Introduction

Photonic generation of spectrally pure microwave signals has drawn great attentions in the past decades. Due to the wide bandwidth and extremely low loss characteristics, photonic techniques are capable of generating stable microwave signals up to 100 GHz [1]–[3]. For example, optoelectronic oscillator (OEO) that achieves an unprecedented phase noise performance of −163 dBc/Hz at 10 kHz offset from a 10 GHz carrier has been reported [4]. In a typical OEO configuration, the output of a laser is externally modulated by an electro-optic modulator (EOM), and the modulated output passes through an optical fiber delay line and is detected by a photodetector. The photodetector output is then amplified and is sent to a microwave band pass filter (BPF) which approximately determines the oscillation frequency. Output from the BPF is fed back into the EOM to form a closed loop system for self-sustained oscillation after satisfying Barkhausen criteria. The low phase noise of OEO is due to the high quality (Q) factor provided by the long length and low loss optical fiber delay line. In addition to signal generation, photonic techniques have been also used for frequency stabilization of oscillators as well. For

example, we have recently demonstrated self-injection locking (SIL) employing long optical fiber delay lines [5], [6] by taking advantage of the high Q factor from long length and low loss optical fiber. Our approach provides substantial phase noise reduction, as opposed to SIL employing electrical delay lines [7].

The concept of optical delay line SIL can also be applied to self-phase locked loop (SPLL). SPLL was first proposed by Underhill [8] using a phase alternating line (PAL) delay line for a low frequency oscillator working in 3–6 MHz. Shortly after, Aitchison and Batliwala [9] built a stabilization circuit using WG16 waveguide to provide the delay and demonstrated that the principle established by Underhill could be extended to microwave frequencies. Contrary to conventional PLL where error signal is obtained by comparing against an external reference, error signal in SPLL is generated from a delay line frequency discriminator (DLFD) [10]. Longer delay provides higher discriminator sensitivity that is crucial for substantial phase noise reduction. However in [8] and [9], the delay is limited due to the loss of the cable and the dimension of the waveguide, therefore the overall reduction is limited. Recently, Pillet *et al.* [11] demonstrated frequency stabilization of a microwave signal generated from the beatnote of a dual-frequency laser, where a DLFD employing long optical fiber delay is used in an optical SPLL to stabilize laser frequency for better spectral purity of the microwave beatnote. Phase noise reduction of 46 dB as opposed to free-running case is reported, reaching -110 dBc/Hz at 10 kHz offset for a 4 GHz carrier. Alemohammad *et al.* [12] also reported optical SPLL of two electro-optic microchip lasers, where -120 dBc/Hz at 10 kHz offset for 11.7 GHz carrier is reported.

In this paper we propose a novel structure where SPLL using optical delay has been applied for phase noise reduction of microwave oscillations in an OEO and an electrical VCO. To fulfill the SPLL function, a tunable element is required to provide the frequency adjustment. Conventional approach for frequency tuning of OEO can be achieved by inserting electrical phase shifter in the loop to change the electrical phase [13]. In this paper, frequency tuning of OEO is achieved by changing the operation point of the MZM away from quadrature biasing point to achieve phase shifting. Phase noise performance of SPLL OEO using the electrical phase control and optical phase control is compared and evaluated for the first time. Other unique features of this paper presented are i) A comprehensive modeling of phase noise for oscillators employing SPLL by modifying the modeling previously reported [11]; ii) an OEO is realized using a low Q BPF and short delay (100 m) to achieve a wide tuning range, phase noise of OEO employing different SPLL topologies of single and dual loop are experimentally and analytically compared for the first time; iii) SPLL technique is also applied to electrical VCO to demonstrate experimentally the phase noise reduction in electrical VCO employing SPLL technique. Phase noise reduction of 65 dB is achieved at 1 kHz offset for the electrical VCO, this is the highest achieved reduction to the best of our knowledge. This paper is organized as follows: Section 2 presents the analytical modeling of phase noise for oscillators employing SPLL techniques. Experimental results for SPLL OEO with BPF control and MZM control are rendered in Section 3. Section 4 provides experimental results of SPLL in VCO using the MZM based fiber optic link. Section 5 discusses potential performance improvement of current SPLL system to achieve phase noise of -150 dBc/Hz at 10 kHz offset and summarizes the paper achievements.

2. Phase Noise Analysis of Self-Phase Locking

In this section the modeling of phase locking mechanism is discussed for an oscillator. This model then is extended to self-phase locked loop system of a particular OEO, but the same modeling can also be applied to other types of oscillators.

2.1. Conventional PLL

A system level modeling is derived using control theory. This approach is preferred as it can also be used to model injection locked oscillators [5], [6] and eventually provide a unified theory for oscillators incorporating injection locking and phase locked loop (ILPLL) [14].

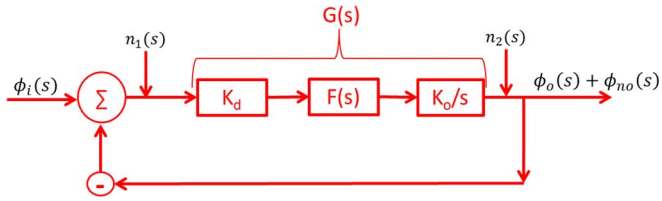

Fig. 1. Control theory representation of conventional PLL. $\phi_i(s)$ and $\phi_o(s)$ are the phases of the input and output signal, respectively. $\phi_{no}(s)$ is the output phase error due to $n_1(s)$ and $n_2(s)$.

Derivation of the modeling is based on the general time domain equation for a PLL, and it is given in [15] as

$$\frac{d\phi_o(t)}{dt} = K_d K_o[f(t) * \sin(\phi_i(t) - \phi_o(t))] \tag{1}$$

where $\phi_i(t)$ and $\phi_o(t)$ are the phases of input signal and output signal respectively, and then, the phase error is expressed as $\phi_i(t) - \phi_o(t)$; K_d is the phase detector gain in V/rad, K_o the VCO tuning sensitivity in rad/V, and $f(t)$ the impulse response of the low-pass filter. The symbol $*$ represents the convolution product. The phase error $\phi_i(t) - \phi_o(t)$ can be assumed to be a small quantity without loss of generality, then (1) can be linearized as

$$\frac{d\phi_o(t)}{dt} = K_d K_o f(t) * [\phi_i(t) - \phi_o(t)]. \tag{2}$$

The above time domain equation is converted into s-domain by performing Laplace transform on both sides of (2), resulting in

$$s\phi_o(s) = K_d K_o F(s)(\phi_i(s) - \phi_o(s)). \tag{3}$$

Then the transfer function of the PLL is derived as

$$H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{G}{1+G} \tag{4}$$

where $G = K_d K_o F(s)/s$. From the system transfer function, we can represent the PLL system in frequency domain in a control theory based block diagram, as shown in Fig. 1. Assuming that noise is a small perturbation to the steady state solution, thus the superposition principle of linear system could be used to estimate the overall output phase error ϕ_{no}. Let's first find out the phase error ϕ_{n1} due to the input noise n_1, as depicted in Fig. 1. In conventional PLL scheme, the input noise n_1 consists of phase noise from reference oscillator n_r and system residual phase noise n_i.

Using basic loop analysis, relationship between the phase error ϕ_{n1} and input noise n_1 can be found as

$$\phi_{n1}(s) = -G\phi_{n1}(s) + Gn_1(s). \tag{5}$$

Rearrange (5) by expressing ϕ_{n1} in terms of n_1 to obtain

$$\phi_{n1}(s) = \frac{G}{1+G} n_1(s) = H(s)n_1(s). \tag{6}$$

Similarly, we can find the output phase error ϕ_{n2} due to oscillator noise n_2 as follows:

$$\phi_{n2}(s) = -G\phi_{n2}(s) + n_2(s) \tag{7}$$

$$\phi_{n2}(s) = \frac{1}{1+G} n_2(s) = (1 - H(s))n_2(s). \tag{8}$$

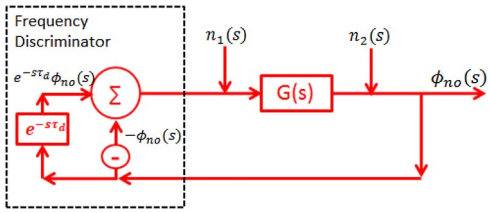

Fig. 2. Control theory block diagram representation of SPLL using a delay line that results in a time delay of τ_d. Components of K_d, $F(s)$, and K_o/s are lumped into a single block $G(s)$.

Then the overall phase error ϕ_{no} due to both n_1 and n_2 is given by

$$\phi_{no}(s) = \phi_{n1}(s) + \phi_{n2}(s) = \frac{G}{1+G} n_1(s) + \frac{1}{1+G} n_2(s). \tag{9}$$

Finally, the overall output noise spectrum becomes

$$S_{pll}(\omega_m) = |H(s)|^2 S_{n_1}(\omega_m) + |1 - H(s)|^2 S_{n_2}(\omega_m) \tag{10}$$

where ω_m is the offset Fourier frequency. In (10), $S_{n2}(\omega_m)$ represents the oscillator phase noise; $S_{n1}(\omega_m)$ represents the input phase noise to the system including reference oscillator phase noise and system residual phase noise.

2.2. SPLL

The control theory representation of SPLL is shown below in Fig. 2. A portion of the VCO output is being delayed by a time τ_d and the phase of the delayed signal is compared against the phase of the current signal. Again the superposition principle of linear systems is applied to find out the overall noise of the SPLL system. We first find out the output phase error ϕ_{n1} due to the input noise n_1. In the case of SPLL, external reference oscillator is not needed, hence the input noise n_1 is just the residual noise n_i. For consistency and simplicity, n_1 is used throughout the paper rather than n_i. Using standard loop analysis, the transfer function of output phase error ϕ_{n1} due to noise n_1 is given as

$$\phi_{n1}(s) = -G\phi_{n1}(s) + e^{-s\tau_d} G\phi_{n1}(s) + Gn_1(s). \tag{11}$$

Rearrange (11) and it becomes

$$\phi_{n1}(s) = \frac{G}{1 + G(1 - e^{-s\tau_d})} n_1(s). \tag{12}$$

Output phase error ϕ_{n2} due to oscillator noise n_2 can be found in a similar fashion as

$$\phi_{n2}(s) = \frac{1}{1 + G(1 - e^{-s\tau_d})} n_2(s). \tag{13}$$

Then the overall phase error ϕ_{no} due to both n_1 and n_2 is given by

$$\phi_{no}(s) = \phi_{n1}(s) + \phi_{n2}(s) = \frac{G}{1 + G(1 - e^{-s\tau_d})} n_1(s) + \frac{1}{1 + G(1 - e^{-s\tau_d})} n_2(s). \tag{14}$$

Hence the noise spectrum at offset of ω_m becomes

$$S_{spll}(\omega_m) = |H_a(s)|^2 S_{n_1}(\omega_m) + |H_b(s)|^2 S_{n_2}(\omega_m). \tag{15}$$

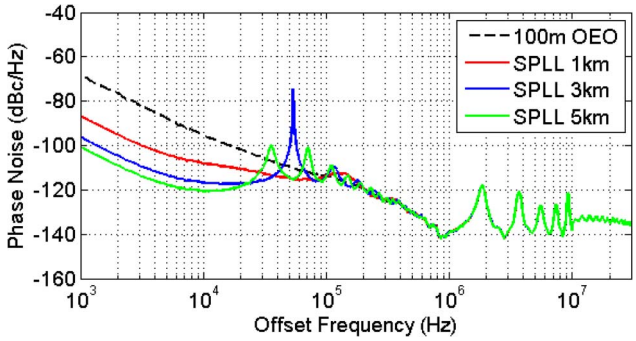

Fig. 3. Simulated phase noise of SPLL with Board 1 (medium loop BW) for different lengths of optical fiber delay line. $K_d = 0.01$ V/rad, and $K_o = 2\Pi \times 200$ kHz/V.

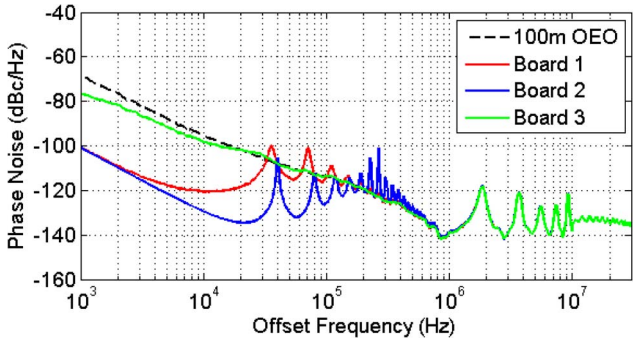

Fig. 4. Simulated phase noise of SPLL with 5 km optical fiber delay line for different 'Mixer+LPFA' boards. $K_d = 0.01$ V/rad, and $K_o = 2\pi \times 200$ kHz/V.

where

$$H_a(s) = \frac{G}{1 + G(1 - e^{-s\tau_d})}, \quad H_b(s) = \frac{1}{1 + G(1 - e^{-s\tau_d})}.$$

The input noise n_1 in SPLL is expressed in [17] as

$$S_{n_1}(\omega_m) = S_{n_i}(\omega_m) = \frac{kTBF}{2P_s}\left(\frac{f_c}{f_m} + 1\right) \tag{16}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant; $T = 290$ °K is the room temperature in Kelvin; $B = 1$ Hz is the noise bandwidth being considered; F is the system noise figure; P_s is the carrier power level; $f_c = 1$ MHz is the flicker corner frequency.

Simulation results of SPLL OEO using (15) are shown below in Fig. 3. The black dashed curve is measured phase noise of an OEO with 100 m delay in the free running case (cf. Section 3.1). Colored curves represent phase noise of OEO with SPLL for different delays from 1 km to 5 km. From the simulation results, phase noise decreases as the delay in SPLL increases. In this paper, $K_o = 200$ kHz/V obtained from the measured tuning sensitivity of the OEO (see Section 3.1) and $K_d = 0.01$ V/rad estimated from the mixer conversion gain (cf. Appendix) and RF power from the fiber optic link (cf. Section 3.1) are used for all the practical simulations.

Numerical simulation is also performed to investigate the impact of different filter components of the "Mixer+LPFA" boards presented in the Appendix. In the simulation, SPLL delay is fixed at 5 km while different "Mixer+LPFA" boards are used. We can see from Fig. 4 that board 2 provides best phase noise reduction due to its large filter bandwidth. It should also be noted

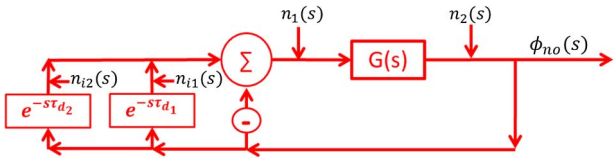

Fig. 5. Control theory representation of DSPLL.

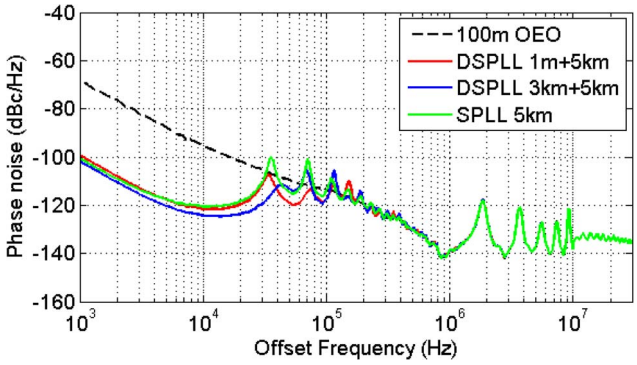

Fig. 6. Simulated phase noise of DSPLL with Board 1 (medium loop BW) for different length combinations of optical fiber delay lines.

that when constructing SPLL, loop stability is of practical concern. A combination of large filter bandwidth and a long fiber delay may result in an unstable loop as the long fiber delay will introduce additional poles (sidemodes) in the system.

2.3. DSPLL and Multiple SPLL

Control theory representation is shown in Fig. 5 for DSPLL. Phase noise expression of DSPLL can be found using loop analysis in a similar fashion to single loop SPLL, and is given as

$$S_{DSPLL}(\omega_m) = |H_c(s)|^2 S_{n_1}(\omega_m) + |H_d(s)|^2 S_{n_2}(\omega_m) \tag{17}$$

where

$$H_c(s) = \frac{G}{1 + G(1 - e^{-s\tau_{d_1}}) + G(1 - e^{-s\tau_{d_2}})}, \quad H_d(s) = \frac{1}{1 + G(1 - e^{-s\tau_{d_1}}) + G(1 - e^{-s\tau_{d_2}})}.$$

In the DSPLL system, $n_1 = n_{i1} + n_{i2}$ where n_{i1} and n_{i2} are the noises associate with the first and second delay paths, respectively. We can assume the noises are identical in each path without loss of generality, and then we can express the noise using (16).

Phase noise simulation of DSPLL using (17) is shown in Fig. 6. From the simulation results, DSPLL provides similar phase noise reduction compared to SPLL, but the side-mode level is greatly reduced in DSPLL due to additional loop.

Impact of different filter components on DSPLL phase noise is simulated for a length combination of 3 km and 5 km to identify the optimum filter parameters, simulation results are shown in Fig. 7. Once again, we can see that the best phase noise is provided by board 2. However, in terms of physical implementation, loop stability has to be considered in order for the PLL to function properly.

We can easily extend the modeling of dual loop topology to multiple loops using control theory, as shown in Fig. 8. The multi-loop SPLL has the phase noise of

$$S_{MSPLL}(\omega_m) = |H_e(s)|^2 S_{n_1}(\omega_m) + |H_f(s)|^2 S_{n_2}(\omega_m) \tag{18}$$

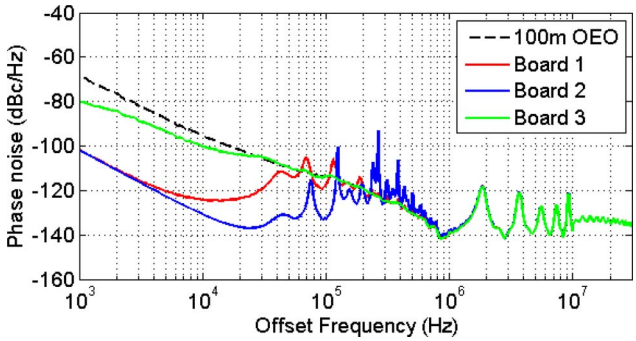

Fig. 7. Simulated phase noise of DSPLL with delay combination of 3 km and 5 km using optical fiber delay line for different 'Mixer+LPFA' boards.

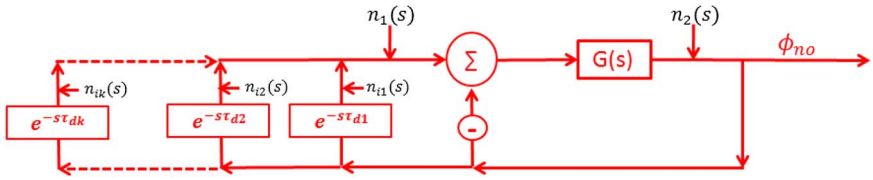

Fig. 8. Control theory representation of multiple SPLL.

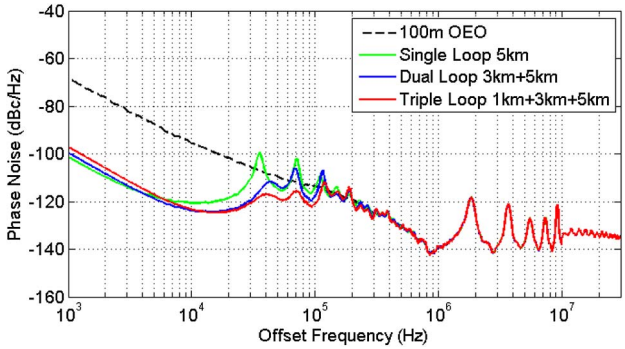

Fig. 9. Comparison of simulated phase noise of SPLL, DSPLL, and TSPLL with Board 1 (medium loop BW) using optical fiber delay line for fiber optic link loss of 42 dB and SPLL loop parameters of $K_d = 0.01$ V/rad and $K_o = 2\Pi \times 200$ kHz/V.

where

$$H_e(s) = \frac{G\sum_{k=1}^{N} n_{ik}}{1 + G\sum_{k=1}^{N}(1 - e^{-s\tau_{dk}})}, \quad H_f(s) = \frac{1}{1 + G\sum_{k=1}^{N}(1 - e^{-s\tau_{dk}})}.$$

Simulation of triple loop SPLL (TSPLL) using (18) is also performed to explore the potential performance improvement. The simulation results are shown in Fig. 9. The red curve shows the performance of SPLL OEO with triple loop of "1 km + 3 km + 5 km." For comparison, single loop SPLL of 5 km and dual loop SPLL of "3 km + 5 km" are also shown in green and blue curve respectively. From the simulation results, TSPLL provides additional side-mode suppression with only a slight phase noise degradation in close-in to carrier offset region.

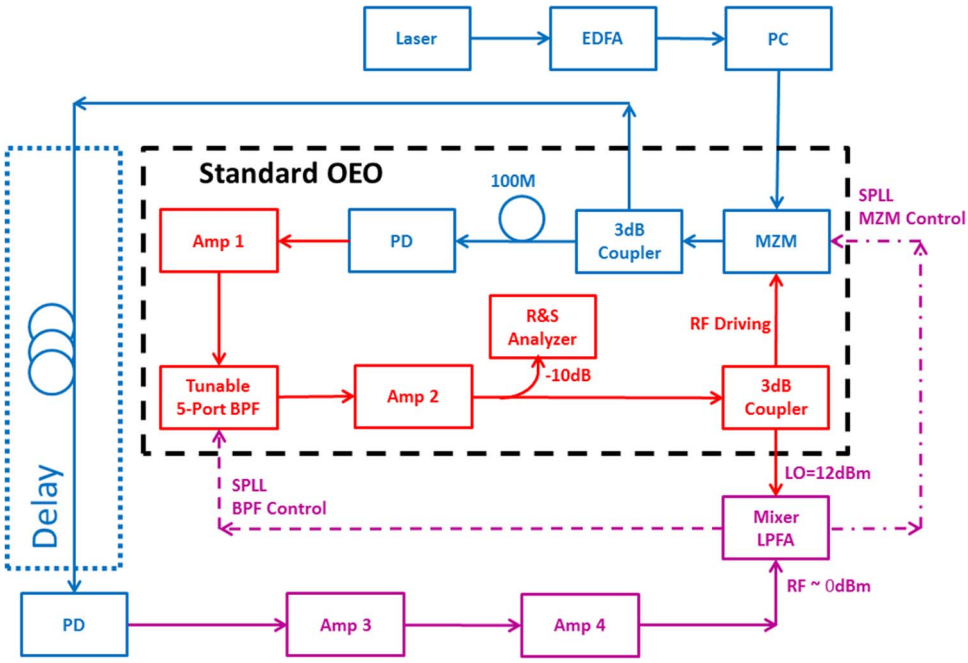

Fig. 10. Experiment Setup of SPLL OEO based on two separate control paths of either BPF control, shown as a dashed line, or the MZM control, which is shown as a dash-dot line. The red lines shows RF signal as part of closed oscillation path and the purple paths are for self-phase lock loop (SPLL).

3. Experimental Evaluation of SPLL in OEO

3.1. Experimental Setup of SPLL OEO

The fiber optic link for 100 m OEO is shown in Fig. 10 with the block components represented in blue color. Output of a DFB laser (Mitsubishi FU-68PDF) is amplified by an EDFA (NuPhoton NP2000) that is followed by a polarization controller (PC). The polarized light is provided as input to an MZM (JDSU MN21024083) with a 1 dB compression point of about 16 dBm. The MZM output is split into two paths and received by two high-speed photodetectors (Discovery Semiconductors DSC50S). The measured fiber optic link loss is 42 dB and the noise figure (NF) of the link is about 50 dB.

The block diagram for standard OEO configuration is depicted in the dashed black box of Fig. 10, where a 5 port BPF is employed as a tunable band-pass filter (cf. Section 4.1 for filter implementation) that determines the OEO oscillation frequency. Amplifier blocks of “Amp1” and “Amp2” are required in the OEO loop to compensate for the fiber optic link loss of 42 dB. Output of the “Amp2” is fed back to the MZM through a 3 dB coupler to close the OEO loop. A portion of the “Amp2” output is coupled out to an R&S FSUP signal analyzer for the most accurate phase noise measurement available from all commercially available test equipment [17]–[19]. To construct the SPLL functionality, a portion of the optical power is coupled out and passes through a longer optical fiber delay, shown in the dashed blue box of Fig. 10. The delayed signal is received by a photodetector and is amplified by amplifier blocks of “Amp3” and “Amp4.” The delayed signal is then compared with the non-delayed OEO output at the “Mixer+LPFA” board to generate a phase locking error signal for OEO frequency control. The control function can be fulfilled either using a tunable BPF or the MZM as an optical phase shifter. Control signal is used to change DC bias of varactor diodes in tunable BPF filter, which adjust the electrical phase of the OEO required for meeting Barkhausen oscillation criteria; the latter relies on changes in the DC bias of the MZM, which adjust the optical phase of the OEO. The advantage of MZM control over BPF control is that the optical phase deviation introduced by MZM will be increased as the light

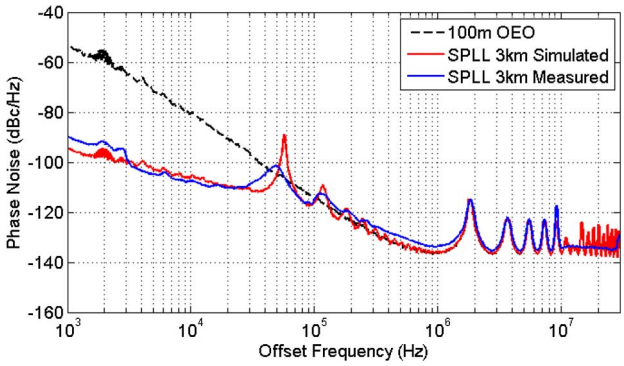

Fig. 11. Comparison of SPLL phase noise between measured and simulated using 3 km optical fiber delay line for fiber optic link loss of 42 dB and the SPLL loop parameters of $K_d = 0.01$ V/rad, and $K_o = 2\Pi \times 200$ kHz/V.

propagates along the fiber, hence resulting in a more tuning sensitivity. Moreover, the MZM has much wider tuning bandwidth as opposed to a narrowband electrical BPF.

3.2. Phase Noise of SPLL OEO and Performance Comparison

3.2.1. SPLL OEO Using Tunable BPF Control

In the standard OEO realization (cf. Fig. 10), a low noise amplifier (Kuhne Electronic 101A) and a power amplifier (B&Z BZ3) are placed in "AMP1" and "AMP2" blocks in Fig. 10. Optical fiber delay line of 100 m long is selected for the OEO. The measured oscillation is at 8.5 GHz and output power of this standard OEO is 6 dBm. Tuning sensitivity of the OEO using tunable BPF control is 200 kHz/V. Phase noise performance is shown in the black curve in Fig. 11. The measured phase noise of the free running OEO is -53 dBc/Hz and -81 dBc/Hz at 1 kHz and 10 kHz offset, respectively.

For the SPLL function, a 3 km fiber delay line is used and the delayed signal is received by a high power photodetector (Discovery Semiconductors DSC50S). A low noise amplifier (Kuhne Electronic 101B) and a power amplifier (Miteq AMF-3D) are used in blocks "Amp3" and "Amp4" in Fig. 10 to boost the signal level. The measured phase noise of SPLL OEO using BPF control is provided in blue curve of Fig. 11. The phase noise at 1 kHz offset is -91 dBc/Hz, which is 38 dB lower than free running OEO; and at 10 kHz, -108 dBc/Hz is achieved corresponding to a 27 dB reduction. Simulated phase noise of SPLL OEO using (17) is also provided in red curve of Fig. 11. An excellent agreement is observed between the analytical modeling and the experimental results. The fiber optic link (expressed in Section 3.1) is used in all the experiments throughout this paper.

3.2.2. SPLL OEO Using MZM Control

High gain power amplifiers are used to replace the amplifiers used in the previous SPLL OEO realization. Power amplifiers with 30 dB gain between 8.5–9.6 GHz from Avantek (AMT 9634) are used in blocks of "Amp1," "Amp2," and "Amp3"; another power amplifier (B&Z BZ3) is used in "Amp4" block. The measured oscillation is at 9.6 GHz with output power of 6 dBm. Phase noise performance for this standard OEO is shown in the black curve in Fig. 12. The measured phase noise is -69 dBc/Hz and -96 dBc/Hz at 1 kHz and 10 kHz offset, respectively.

In contrast to BPF control, the error signal is applied to the MZM bias port to achieve the frequency control of the OEO. Tuning sensitivity of the OEO using MZM control is 580 kHz/V for MZM DC bias of 1.2 V. However, this improved tuning sensitivity is not utilized in the SPLL operation because the "Mixer+LPFA" board outputs a DC offset around 5 V in locked state and tuning sensitivity drops to 200 kHz/V for MZM DC bias of 5 V. Experimental phase noise of

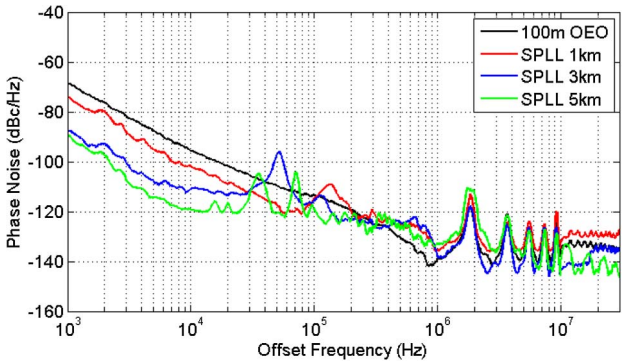

Fig. 12. Measured phase noise of SPLL with Board 1 (medium loop BW) for different lengths of optical fiber delay line for fiber optic link loss of 42 dB and the SPLL loop parameters of $K_d = 0.01$ V/rad, and $K_o = 2\Pi \times 200$ kHz/V. Black curve: phase noise of free running 100 m OEO; Red curve: phase noise of SPLL with 1000 m delay; Blue curve: phase noise of SPLL with 3000 m delay; Green curve: phase noise of SPLL with 5000 m delay.

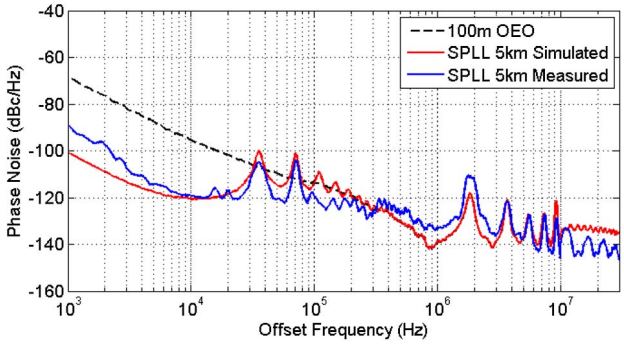

Fig. 13. Comparison of SPLL phase noise between measured and simulated using 5 km optical fiber delay line for fiber optic link loss of 42 dB and the SPLL loop parameters of $K_d = 0.01$ V/rad, and $K_o = 2\Pi \times 200$ kHz/V.

SPLL OEO with MZM control is shown in Fig. 12 for various SPLL delay length. The phase noise reduces as the SPLL delay lengths increases, which is expected from the analytical modeling. Best result is obtained using a 5 km delay in SPLL, and the noise level is reduced by 20 dB reaching -89 dBc/Hz at 1 kHz offset and by 23 dB reaching -119 dBc/Hz at 10 kHz offset. Note that in Section 3.2.1 where a BPF control is used, 5 km delay results in an unstable loop operation. In contrast, SPLL is functioning with 5 km delay in MZM control and provides lower phase noise. Fig. 13 shows an excellent agreement between simulation (red curve) and measured (blue curve) results of SPLL OEO using MZM control for 5 km delay.

3.3. Impact of Different "Mixer+LPFA" Boards on Phase Noise for a Fixed Delay

Different "Mixer+LPFA" boards (cf. Appendix) are used to investigate the impact of PLL loop bandwidth on phase noise when a 3 km optical fiber delay line is used. Experimental setup is the same as depicted in Fig. 10. From the measurement results shown in Fig. 14, the best phase noise performance is provided by Board 1 with a loop bandwidth of about 100 kHz rather than Board 2 with a loop bandwidth of about 1 MHz, which contradicts the analytical prediction. Possible reason for the discrepancy is that the 3 km delay introduces too many side-modes within the PLL loop bandwidth, and the interaction between the side-modes degrades the performance of SPLL. Measured phase noise performance is tabulated in Table 1 for comparison.

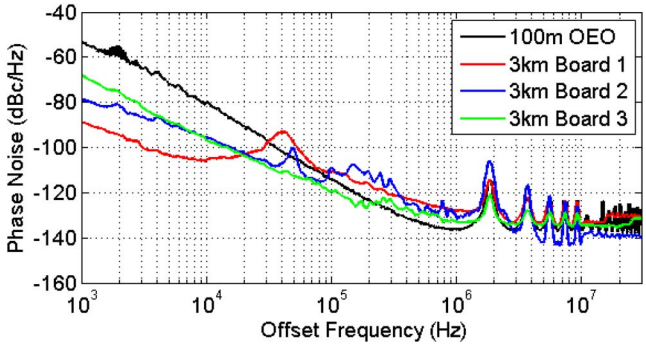

Fig. 14. Measured phase noise of SPLL OEO with different "Mixer+LPFA" Boards using 3 km optical fiber delay line for fiber optic link loss of 42 dB and the SPLL loop parameters $K_d = 0.01$ V/rad, and $K_o = 2\Pi \times 200$ kHz/V.

TABLE 1

Comparison of measured close-in to carrier phase noise for different boards using a fixed optical fiber delay line of 3 km

	dBc/Hz @1kHz	dBc/Hz @10kHz
Board 1	-89.2	-105.5
Board 2	-78.9	-95.7
Board 3	-68.1	-96.9

4. Experimental Evaluation of Optical SPLL in VCO

4.1. VCO Realization

The VCO circuit is shown in Fig. 15, where it consists of a tunable filter and an amplifier (Avantek AMT 9634) with small signal gain of 28 dB and output 1 dB compression of 12 dBm. The tunable filter is constructed using an open circuit microstrip line loaded with two varactor diodes (Aeroflex MGV125-08). The tunability of the filter is achieved by changing the reverse bias voltage of the varactor diodes. The VCO free running frequency is at 8.5 GHz with an output power of 0 dBm, and the tuning sensitivity is about 200 kHz/V at 5 V reverse bias voltage. The measured phase noise is shown in the black dashed curve of Fig. 17. The phase noise slope is about 30 dB/decade up to 10 MHz offset which indicates a flicker noise dominated system. This high flicker noise is usually associated with an FET based amplifier, and flicker noise could be reduced when HBT based amplifiers are employed.

4.2. Optical SPLL and DSPLL in VCO

Experiment setup of SPLL and DSPLL are depicted in Fig. 16. Output of the VCO is amplified and used to drive the MZM. The modulated optical signal passes through a long fiber delay of 3 km and is converted to electrical signal by a photodetector (Discovery Semiconductors DSC50s). The delayed signal is used as a reference to the RF port of the "Mixer+Filter" board 1 for comparison with the non-delayed signal coupled directly from the VCO output. The circuit diagram of DSPLL is similar to that of SPLL. The difference is output of the MZM is split into two separate delay paths: one passes through a 5 km delay while the other passes through a 3 km delay. The two delayed signals are received by two photodetectors (Discovery Semiconductors DSC50s) independently, and are combined in a 3 dB coupler. The combined signal is amplified and sent to the "Mixer+Filter" board to be compared with a non-delayed signal from the VCO output.

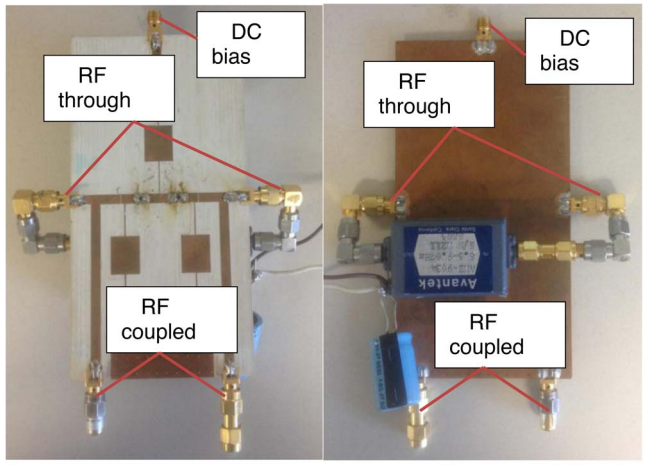

Fig. 15. Picture of the VCO (a) Top view. (b) Bottom View.

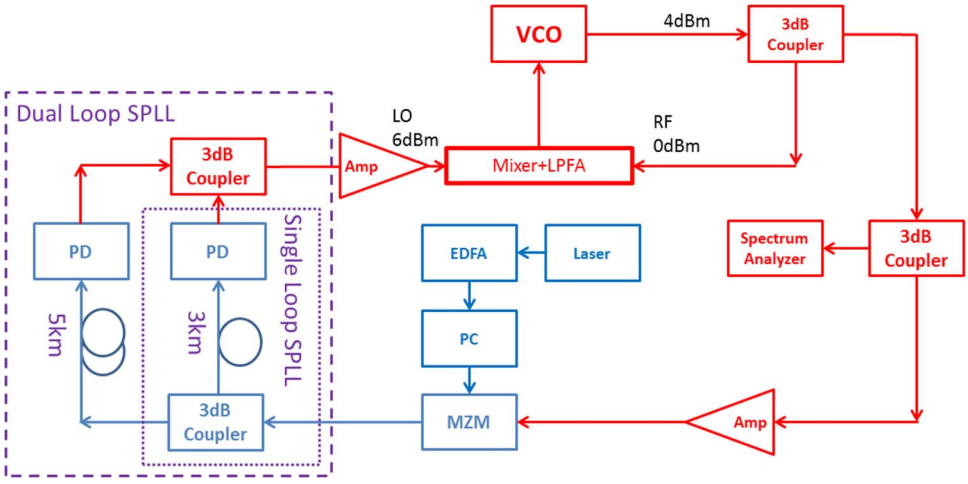

Fig. 16. Experiment Setup of VCO with SPLL (dotted box) and DSPLL (dashed box).

Measured phase noise of VCO with 3 km SPLL is shown in blue curve of Fig. 17. The phase noise of the SPLL VCO is reduced from −26 dBc/Hz of free running case to −71 dBc/Hz at 1 kHz offset corresponding to a reduction of 45 dB; at 10 kHz offset, phase noise is improved by 20 dB reaching −78 dBc/Hz. Simulation result using (17) is also depicted in red curve of Fig. 17. We can see the excellent agreement between analytical and experimental results. SPLL with 5 km delay is attempted to achieve further phase noise reduction, but the long delay introduces strong side-modes that are spaced every 40 kHz away from the carrier, which causes the phase lock loop to be unstable and fails to acquire a locked state. However, the experiments using DSPLL has been effective in stabilizing the PLL operation and eventually a better phase noise is achieved due to side-mode suppression in the loop. Experiment result of DSPLL with 3 km and 5 km delay is shown in green curve of Fig. 17, where the phase noise of the DSPLL VCO is reduced from −26 dBc/Hz of free running case to −91 dBc/Hz at 1 kHz offset corresponding to a reduction of 65 dB; at 10 kHz offset, phase noise is improved by 42 dB reaching −100 dBc/Hz. Simulation result of DSPLL using (18) is also provided in magenta curve of Fig. 17, and it matches up well with the measurement results. We can see from Fig. 17 that DSPLL provides 20 dB more reduction than SPLL in offset frequencies from 1 kHz to 50 kHz.

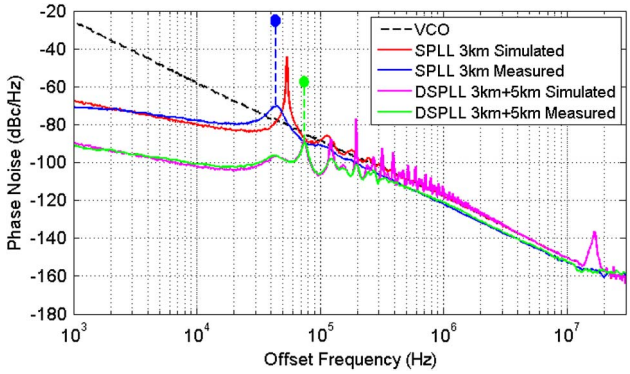

Fig. 17. Phase noise of VCO employing different SPLL topologies using Board 1 for fiber optic link loss of 42 dB and SPLL parameters of $K_d = 0.01$ V/rad, and $K_o = 2\Pi \times 1$ MHz/V. Black dashed curve is VCO free running phase noise. Phase noise of VCO employing single loop SPLL with 3 km delay is shown as a red curve (simulated) and a blue curve (measured). Phase noise of VCO employing dual loop SPLL with 3 km and 5 km delays is shown as a magenta curve (simulated) and green curve (measured). Blue dot: first spurious signals of SPLL at 44 kHz offset with level of -23 dBc; green dot: first spurious signals of DSPLL at 75 kHz offset with level of -55 dBc.

TABLE 2

Comparison of SSB phase noise with different circuit configurations

Control Method	Circuit Topology	Measured (dBc/Hz)	
		1kHz	10kHz
100m OEO using BPF Phase Control	Free Run	-53	-81
	SPLL 3km	-91	-108
100m OEO using MZM Phase Control	Free Run	-69	-96
	SPLL 5km	-89	-119
VCO	VCO w/ 5port BPF	-26	-58
	SPLL 3km	-71	-78
	DSPLL 3km+5km	-91	-100

In Fig. 17, the blue dot and green dot represent the actual level of the first spurious signals of SPLL and DSPLL, respectively. For SPLL, the first spurious signal appears at offset frequency of 44 kHz with a level of -23 dBc (blue dot), which is relatively high, but for DSPLL, the spurious signal at 44 kHz offset in previous case is suppressed by more than 70 dB and becomes a small hump with a level of -96 dBc due to the dual loop operation, and the actual first spurious signal in DSPLL is pushed away to 75 kHz offset with a level of -55 dBc (green dot), corresponding to a suppression of 32 dB compared to that in SPLL configuration.

5. Discussion and Conclusion

This paper is dedicated to the analysis, design, and experimental performance evaluation of self-phase locked loop oscillators using long optical fiber delay lines. Table 2 summarizes the experimentally achieved phase noise reduction at 1 kHz and 10 kHz offset frequencies for various circuit topologies using MZM based fiber optic link.

In the case of OEO using MZM control, phase noise of -119 dBc/Hz is achieved at 10 kHz offset for a 9.6 GHz carrier. The lowest achieved phase noise is similar to that reported by Alemohammad *et al.* in [12]. However, the laser source used in [12] is a solid-state laser with superior spectral linewidth [20], whereas in this paper, a DFB laser with poorer spectral purity is used. Lower phase noise is expected if the noise contribution from the optical source in our system can be reduced. In addition, the fiber optic link has a NF of about 50 dB, contributing

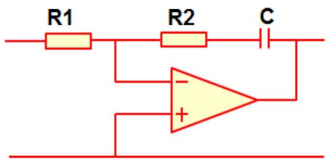

Fig. 18. Active filter circuit topology.

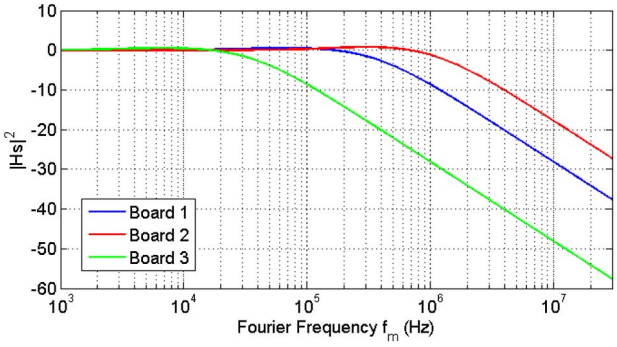

Fig. 19. Simulated loop bandwidth for different 'Mixer+LPFA' boards.

TABLE 3

Loop bandwidths with different filter parameters for $K_d = 0.1$, $K_o = 200$ kHz/V, and R1 $= 51\ \Omega$

Board	Rand Capacitor Values	Loop BW	ω_n	ζ
1	R2=1kΩ, C=4.7nF	≈ 200kHz	2π×115kHz	1.7
2	R2=3.3kΩ, C=0.27nF	≈ 700kHz	2π×481kHz	1.3
3	R2=100Ω, C=470nF	≈ 20kHz	2π×11.5kHz	1.7

substantial noise to the system, and the VCO is noisy and unstable, which also limits the overall phase noise performance. If the NF of the fiber optic link is reduced to 20 dB and a better VCO (Synergy DRO100) is used, phase noise of −150 dBc/Hz is predicted at 10 kHz offset for a 10 GHz carrier.

Both close-in and far-away-from-carrier-phase noise could be reduced by combing IL and PLL function [14]; therefore, one could employ forced self-injection [5], [6] and self-phase locking to build an SILPLL oscillator [21]–[24] to improve short term stability of an oscillator without relying on external reference source. Long term stability of the oscillator can be improved by utilizing passive temperature compensation [25].

Appendix
"Mixer + LPFA" Board Design Parameters

To perform the PLL function, a mixer and a low pass filter amplifier (LPFA) are integrated on a single circuit board, i.e. "Mixer+LPFA" board. The mixer is a double-balanced mixer from Hittite (HMC558LC3B). The LPFA is constructed using an op-amp (LT1028) circuit, shown in Fig. 18. The filter transfer function is given as [26]

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1} \tag{19}$$

where $\tau_1 = R_1 C$; $\tau_2 = R_2 C$. PLL loop Transfer function incorporating this active filter is found as [26]

$$H(s) = \frac{2\zeta\omega_n s + \omega_n}{s^2 + 2\zeta\omega_n s + \omega_n} \tag{20}$$

where $\omega_n = \sqrt{(K_o K_d)/\tau_1}$ is the natural frequency, and $\zeta = (\tau_2 \omega_n)/2$ is the damping factor. The 3 dB bandwidth of PLL transfer function can be adjusted by changing the resistor R2 and capacitor C of the filter while R1 is fixed at 51 Ω. The loop transfer function (20) is plotted in Fig. 19 for various filter parameters to estimate the loop bandwidth behavior. The results of loop bandwidth, natural frequency and damping factor are tabulated in Table 3.

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