IEEE Photonics Journal
An IEEE Photonics Society Publication

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Volume 6, Number 5, October 2014

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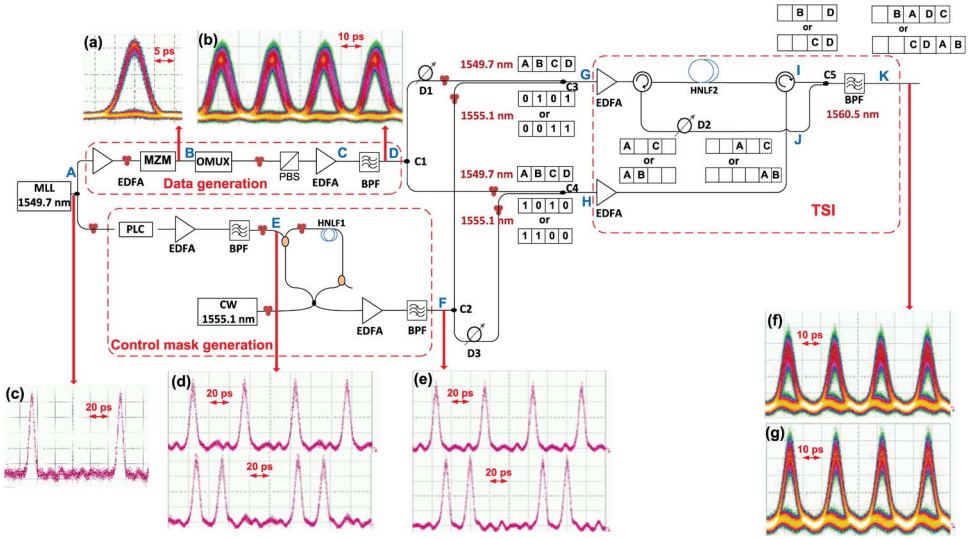

DOI: 10.1109/JPHOT.2014.2356509

Reconfigurable Time Slot Interchange Based on Four-Wave Mixing and a Programmable Planar Lightwave Circuit

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DOI: 10.1109/JPHOT.2014.2356509

Manuscript received August 6, 2014; revised August 30, 2014; accepted September 2, 2014. Date of publication September 10, 2014; date of current version September 17, 2014. Corresponding author: L. R. Chen (e-mail: lawrence.chen@mcgill.ca).

Abstract: We demonstrate the all-optical reconfigurable time slot interchange (TSI) of individual bits at 40 Gb/s based on four-wave mixing (FWM) and a programmable planar lightwave circuit (PLC). The PLC is used to generate different control signals (masks) that determine which bits undergo TSI. By programming the PLC to generate two different masks, two different TSI patterns are obtained. TSI is achieved using FWM between the data signal and the desired mask with bidirectional propagation in a length of highly nonlinear fiber. Error-free operation is obtained for both of the TSI patterns, with a power penalty < 5.2 dB, at a bit error rate of 10^{-9}.

Index Terms: Time slot interchange (TSI), planar lightwave circuits, four wave mixing (FWM), wavelength conversion.

1. Introduction

Optical packet-switched (OPS) networks require functionalities such as optical buffering or tunable optical delays (ODLs) [1]–[4] and time slot interchange (TSI) [5], [6]. Optical buffers are required for contention resolution, which arises when two or more packets arrive at a node and are destined for the same output port at the same time. Optical buffers are also used to align payloads and labels in label-switched networks. TSI is a signal processing function that can be categorized in two types: packet-level TSI and bit-level TSI. In packet-level TSI, the order of packets are swapped at a switching node [5], [6]. On the other hand, in bit-level TSI, the order of data bits is swapped, i.e., bits are shifted from their current into new temporal slots. Both packet-level and bit-level TSI provide increased flexibility in network operation. For example, bit-level TSI can increase switching capabilities for time-division-multiplexed networks. All-optical approaches for buffering, TSI, and other signal processing functions are of interest [10].

The main challenge for performing all-optical packet-level TSI is to provide large optical delays that are tunable over a wide range, e.g., ns and greater, and that do not induce signal distortion. In [5], packet-level TSI was performed along with serial-to-parallel conversion, parallel-to-serial

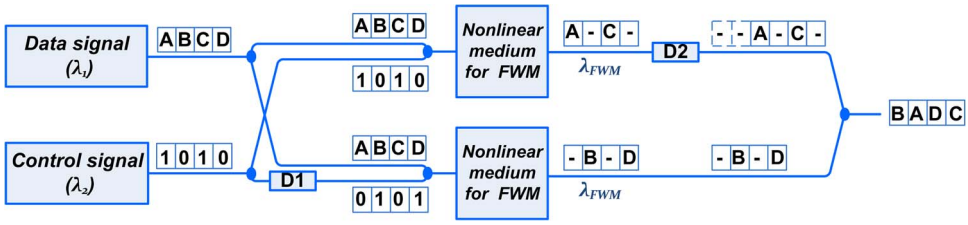

Fig. 1. Conceptual diagram of the proposed TSI technique.

conversion, and packet compression with 10 Gb/s data using an optical buffer with a large variable delay based on a multi-loop configuration and a single switch element. The approach, however, is not scalable due to accumulation of amplified spontaneous emission (ASE) noise from Erbium-doped fiber amplifiers (EDFAs) in the loop configuration. In [6], all-optical TSI of variable length packets with 40 Gb/s data was demonstrated using conversion-dispersion-based tunable ODLs. In a stream of packets, for each block of two packets, one is delayed relative to the other using a highly dispersive medium before being multiplexed back together. Packets are extracted via wavelength conversion through four wave mixing (FWM) in a length of highly nonlinear fiber (HNLF). Then, using a periodically poled lithium niobate (PPLN) waveguide for sum frequency generation followed by difference frequency generation (DFG), the packets are re-converted to their original wavelength. By varying the amount of delay, TSI of packets having two different lengths was achieved.

Bit-level TSI can be performed easily in the electronic domain using shift registers. However, the data rates that can be processed are constrained by the speed of electronics and there is the need for O/E as well as E/O conversion. Several approaches for optical bit-level TSI have been reported [7]–[9]. For example, in [9], bit-level TSI of 2.5 Gb/s data (NRZ-OOK) was achieved whereby bits in adjacent time slots were swapped based on two wavelength conversion processes (using DFG in a PPLN waveguide) and a wavelength dependent delay enabled by cascaded fiber Bragg gratings. A key element of all-optical bit-level (packet-level) TSI is the selection of bits from the original data (packet) stream that will be processed (i.e., undergo TSI); this is usually achieved using wavelength conversion. A control signal (or mask) is required to select which bits will undergo wavelength conversion, and hence TSI. In [9], a fixed mask was used resulting in a fixed TSI pattern.

In this paper, we demonstrate all-optical reconfigurable bit-level TSI of 40 Gb/s RZ-OOK data using FWM for wavelength conversion and a programmable silica-based planar lightwave circuit (PLC). The PLC can generate different masks to reconfigure the TSI pattern while FWM preserves the phase information of the data signals, which makes our technique transparent to modulation format.

2. Principle of Operation

Fig. 1 illustrates the conceptual diagram of our proposed TSI technique. To understand the principal of operation, we consider a TSI pattern in which a block of 4 input data bits, denoted ABCD, are swapped to become BADC. Our TSI approach consists of the following steps. First, a control mask (for illustrative purposes, we show “1010”) which determines the bits that are temporally swapped is generated. Second, the control mask and the data signal are split to generate two copies of each; one copy of the data signal and one copy of the control mask are combined and passed through a nonlinear medium, where the “1” bits of the control mask are aligned with the bits A and C of the data. Due to FWM, bits A and C are selected and converted to a new wavelength, denoted λ_{FWM}. Next, the new signal at λ_{FWM} comprising the selected bits A and C undergoes a delay of 2 bits, denoted D2. The second copy of the control mask undergoes a 1-bit delay (D1) and is combined with the second copy of the data signal; they are then passed through a second nonlinear medium. In this case, the “1” bits of the control signal are aligned with bits B and D of the data signal. Due to FWM, bits B and D are selected

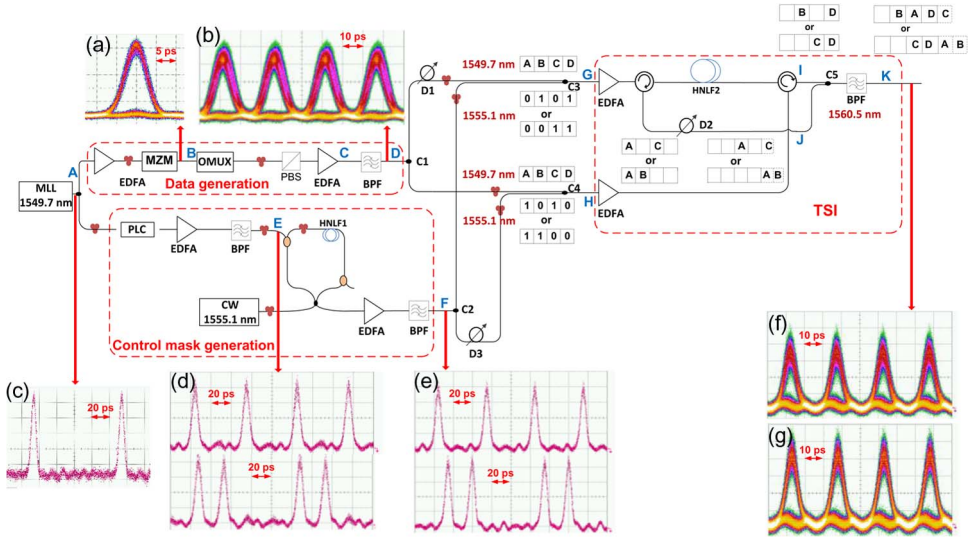

Fig. 2. Schematic of experimental setup for reconfigurable TSI. Insets. (a) Eye diagram of the 10 Gb/s data; (b) eye diagram of the 40 Gb/s data; (c) temporal trace of the MLL output; (d) temporal traces of the control masks before the NOLM; (e) temporal traces of the control masks after the NOLM; (f), (g) eye diagrams of the two TSI patterns corresponding to the control masks 1010 and 1100, respectively.

and converted to λ_{FWM}. Finally, the two streams of selected bits (both at λ_{FWM}) are combined to form the TSI-ed version of the original data signal, i.e., BADC. A similar process is followed for a second TSI pattern, ABCD → CDAB using control mask "1100" and 2-bit and 4-bit delays for D1 and D2, respectively.

3. Experimental Setup, Results, and Discussion

Fig. 2 shows the experimental setup, which comprises 3 main parts: one to generate the data signal, one to generate the mask signal that determines which bits are swapped, and the actual block that performs TSI. The data signal is generated by modulating a 10 GHz pulse train from a mode-locked laser (MLL) at 1549.7 nm with a $2^7 - 1$ PRBS that is then optically multiplexed to 40 Gb/s. The 10 GHz pulse train from the MLL has a timing jitter of about 300 fs (point A). A polarization beam splitter (PBS) is used to ensure uniform polarization for all data bits of the 40 Gb/s signal. The data signal is then amplified using an EDFA followed by a 1.2 nm band pass filter (BPF) to reduce out-of-band ASE; the power level at point D is 6.1 dBm and the corresponding extinction ratio (ER) and timing jitter are 20.2 dB and 900 fs, respectively. The eye diagram of the 40 Gb/s signal is shown in the inset of Fig. 2.

The mask signal is generated by passing a copy of the 10 GHz pulse train from the MLL through the programmable PLC and a nonlinear optical loop mirror (NOLM). The PLC is a 6-loop lattice-form Mach–Zehnder interferometer which implements a programmable finite impulse response filter [11]. One arm of each MZI incorporates a heater strip, fabricated by evaporating a 100 nm thick layer of Cr over a waveguide segment. Gold contacts are patterned and wire-bonded to connector pins on a device carrier. By applying different voltages to the connector pins, different temperatures (T_i) and hence phase shifts (ϕ_i) in the arms of the MZIs can be obtained, resulting in different impulse responses. Fig. 3 shows a schematic of the PLC along with a cross-section of the waveguide; full details regarding the device structure and its characterization can be found in [11]. The PLC takes an input signal at 10 GHz and (1) increases the repetition rate to 40 GHz and (2) allows to program the amplitude of the output pulses, namely to generate 4-bit codes which repeat at 10 GHz. Among the different 4-bit binary codes that can be generated, we use two codes, "1010" and "1100", to define two different TSI patterns as described in Section 2: ABCD → BADC using mask 1010 and ABCD → CDAB with mask 1100.

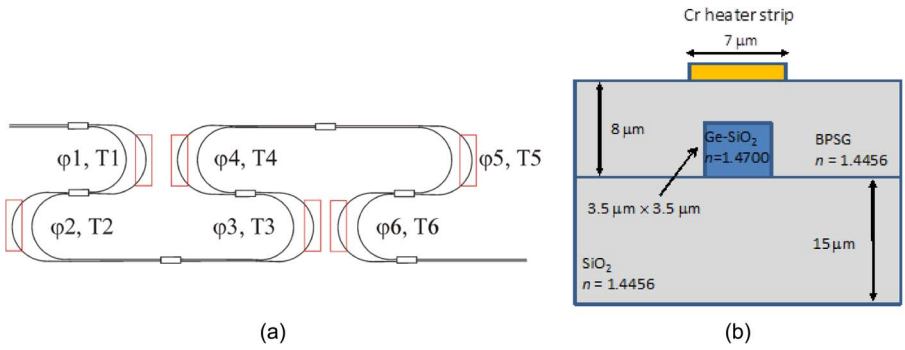

Fig. 3. (a) Schematic of the silica-based PLC and (b) waveguide cross-section.

The output of the PLC is amplified and then filtered using a BPF with a 2.4 nm bandwidth to remove the out of band ASE. It is launched into the NOLM (as the pump signal) along with a continuous wave (CW) signal at 1555.1 nm (as the probe signal). The NOLM comprises a polarization controller (PC) followed by 1000 m of HNLF with a dispersion $= -0.04$ ps$/($nm $\cdot$ km$)$ and dispersion slope $= 0.02$ ps$/($nm$^2 \cdot$ km$)$ (both at 1550 nm). The NOLM is used to remove pulse-to-pulse phase variations at the PLC output, as well as to wavelength convert the mask so that the mask and data signals are at different wavelengths. At point E (NOLM input), the mask has an average power of 15 dBm; the timing jitter for the 1010 and 1100 masks are 400 fs and 380 fs, respectively. At point F (NOLM output), the average power is 5.8 dBm and the corresponding timing jitter for the 1010 and 1100 masks are 360 fs and 340 fs, respectively. Temporal traces of the two control masks are shown as insets in Fig. 2.

For wavelength conversion, we use FWM in a length of HNLF. To understand the operation of the TSI block, we consider the case of using the control mask 1010. Using the two couplers C1 and C2, the mask and data signals are first split to generate two copies of each; both pairs of mask and data signals are subsequently combined using two separate couplers C3 and C4. PCs are located in each of the four branches before the two pair of signals are combined in order to optimize FWM. Each pair is amplified by a high-power EDFA and propagates through 200 m of HNLF (having the same parameters as that used in the NOLM) in opposite directions. Two circulators are located at the both ends of the HNLF to extract the output signals at both ends of the HNLF. In the forward direction (point G), the "1" bits of the mask signal are aligned in time with the even bits (B and D) of the data signal; in the backward direction (point H), they are aligned with the odd bits (A and C); alignment is performed using ODLs D1 and D3, respectively. Due to FWM, the even bits and odd bits of the data signal are separately selected and wavelength converted to the same FWM wavelength ($\lambda_{FWM} = 1560.5$ nm) in the forward and backward directions. The converted odd bits then undergo a 2-bit delay D2 (here 50 ps). The forward and delayed backward signals are then combined using coupler C5, followed by a BPF at 1560.5 nm with bandwidth 1.2 nm to extract the signal at (λ_{FWM}. The output in the time domain comprises a signal in which the order of the odd and even bits is swapped compared to the original data signal (TSI-ed). A similar process is used with the mask signal 1100, except that the converted odd bits undergo a 4-bit delay before combination at C5. The signal after the coupler C5 is the TSI-ed version of the original input data which is then received by a 45 Gb/s photodetector, followed by an error detector to perform bit error rate (BER) measurements. BER measurements are performed for the two TSI scenarios as well as the back-to-back. The eye diagram for the back-to-back case and the two TSI patterns are shown as insets in Fig. 2.

Fig. 4(a) and (e) show 40 bits of the original 40 Gb/s data signal. The results for TSI using the control mask 1010 (ABCD $\rightarrow$ BADC) are shown in Fig. 4(b)–(d): Fig. 4(b) shows the wavelength converted even bits of the data (at 1560.5 nm) while Fig. 4(c) shows the wavelength converted odd bits after the 2-bit delay. Fig. 4(d) shows the combination of the above two and corresponds to the wavelength converted data signal with TSI. The TSI-ed signal has a timing jitter of about

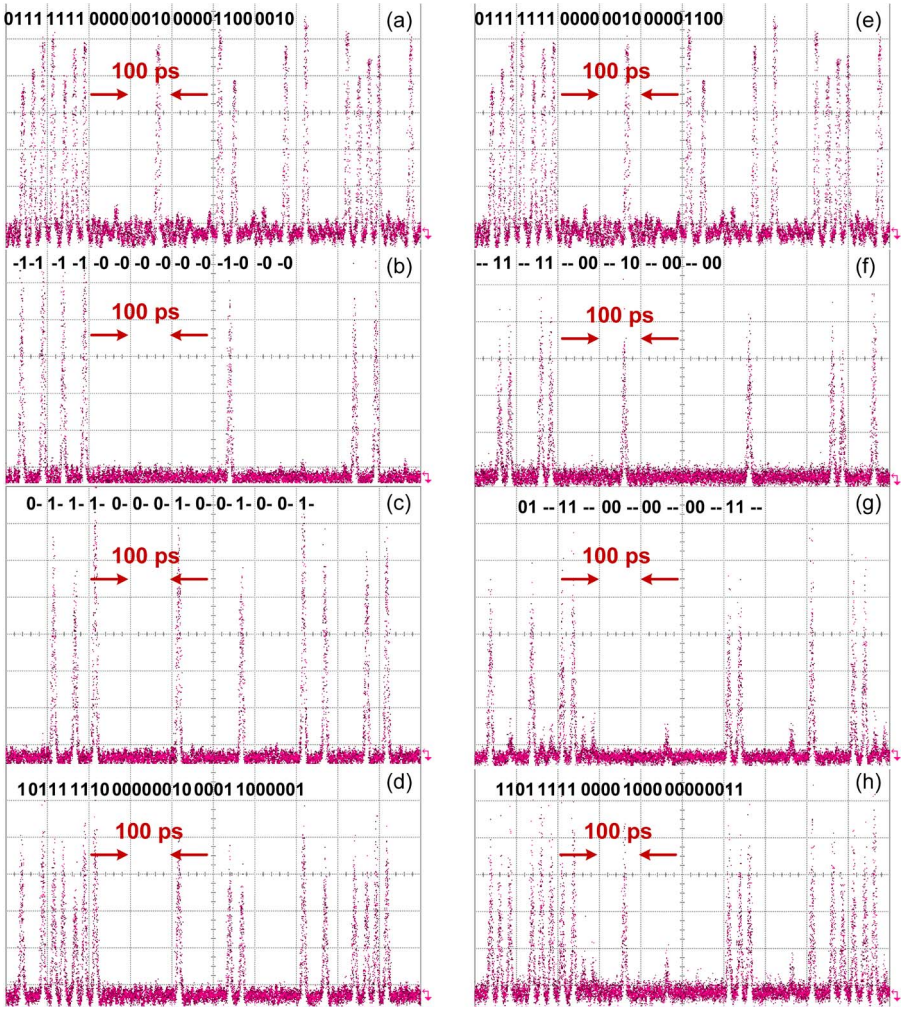

Fig. 4. Temporal traces. (a), (e) 40 bits of the original 40 Gb/s RZ OOK data signal, (b) even bits of the data signal selected by the control mask 1010 delayed by 1 bit, (c) odd bits of the data signal selected by the 1010 control mask and after the 2-bit delay D2 (50 ps), (d) TSI-ed signal corresponding to 1010 control mask (ABCD → BADC), (f) bits 3 and 4 of each block of 4 bits from the data signal selected by the 1100 control mask delayed by 2 bits, (g) bits 1 and 2 of each block of 4 bits from the data signal selected by the 1100 control mask and after the 4-bit delay D2 (100 ps), and (h) TSI-ed signal corresponding to 1100 control mask (ABCD → CDAB). All sub figures show wavelength converted signals located at 1560.5 nm, except sub figures (a) and (e), which are at 1549.7 nm. The 1 and 0 bits refer to those in the original data sequence, along with those that have undergone wavelength conversion (in both directions) and that of the final TSI signal.

620 fs and an ER of 13 dB. Fig. 4(f)–(h) show the corresponding results for the control signal 1100 (ABCD → CDAB). The BER for the original 40 Gb/s signal (back-to-back) and for the signals after TSI are shown in Fig. 5(a). The power penalty at a BER of 10^{-9} are 5.2 dB and 4.5 dB for the TSI signals using masks 1010 and 1100, respectively. Fig. 5(b) shows the spectra at different points of the setup for the swapping pattern (ABCD → BADC).

Factors that contribute to the power penalty include the following. The optically multiplexed 40 Gb/s data signal exhibits slightly different pulse-to-pulse separation between the adjacent bits. Therefore, when aligning the control masks with the data signals, different data bits have slightly different overlap with the 1 bits of the control mask thereby impacting wavelength conversion performance. The setup is also sensitive to polarization and drifts or changes in the PC will affect overall performance. The difference in power penalty for the two TSI patterns is attributed in part to the non-identical signal quality of the corresponding mask signals 1010 and

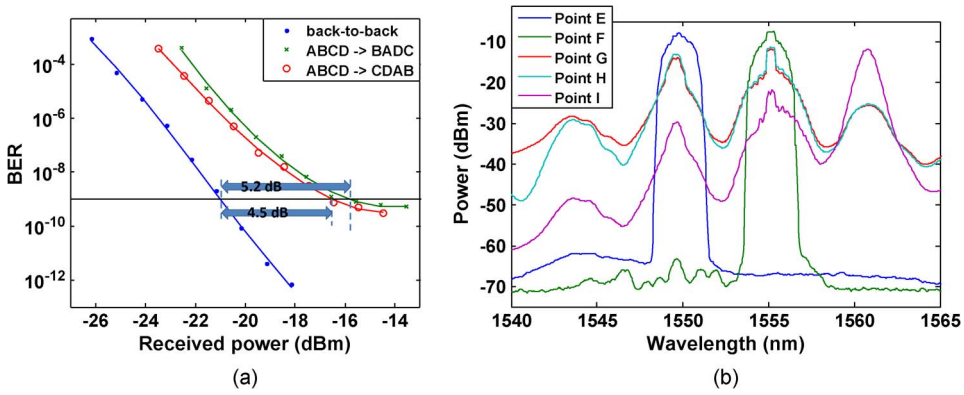

Fig. 5. (a) Measured BER for the 40 Gb/s data signal in back-to-back and after TSI and (b) spectra of signals at different points of the setup for the 1010 control mask.

1100. Moreover, the changes in thestate of polarizations of the signals and the temporal drift over time associated with changing the OLDs results in slight changes in system performance.

The PLC can generate 16 different 4-bit codes (masks) which repeat at 10 GHz. When applying the "masks" to a given data sequence and with a given delay, certain masks "repeat," i.e., a mask and its complement (e.g., 1100 and 0011) can be obtained using a simple delay and we take advantage of this in our TSI implementation. In general, we can separate the 16 4-bit masks in the following groups: 1100, 0110, 0011, and 1001 (Group A); 1010 and 0101 (Group B); 0001, 0010, 0100, and 1000 (Group C); 0111, 1011, 1101, and 1110 (Group D); and 0000 and 1111 (Group E). In this paper, we used Groups A and B to demonstrate reconfigurable TSI. In particular, we use two "parallel" branches in which the data signal and the control mask, as well as a copy of the data signal and the complement of the mask, undergo FWM-based wavelength conversion via bidirectional propagation in the HNLF. We can perform TSI using the other groups of codes. However, a more complex setup is required to generate the mask and its complement, or additional "branches" are required to perform the necessary wavelength conversions before temporal alignment. The number of bits that can be swapped is limited in part by the generation of 4-bit codes that repeat at 10 GHz. It is possible to generate "bursts" of a 4-bit code starting from a lower repetition rate MLL. This will allow a longer string of data bits to be processed, however, only a few of the bits in the original sequence will undergo TSI. For example, if the MLL operates at 5 GHz, with the PLC set to generate "1100" we actually have the controlmask "1100000011000000 ..." and swapping of select bits in an 8-bit pattern "ABCDEFGH" can take place. This also allows for a greater range of TSI patterns although the complexity of the setup will increase.

The current setup incorporates a number of large components and benchtop instruments. The size of the setup, though, can be reduced via integration especially considering the various advances in silicon photonics. For example, the HNLF can be replaced with silicon nanowires and Bragg grating filters (or other filters) can be integrated with nonlinear waveguides. It should also be possible to develop integrated forms of the 2-bit and 4-bit delays, or more generally, an integrated switched delay line using low-loss waveguide spirals. Both of these integrated solutions will allow significant reductions in the size of the setup.

4. Summary and Conclusion

We have demonstrated all-optical reconfigurable, bit-level TSI based on FWM and a programmable PLC. The PLC enables reconfigurability by generating different control masks which lead to different TSI patterns. We have experimentally verified successful TSI in a 40 Gb/s RZ OOK data signal with two different patterns: (ABCD → CDAB), (ABCD → BADC). Error-free operation with a maximum power penalty of 5.2 dB is obtained. An important property of our proposed TSI technique is the potential transparency to different modulation formats, as FWM is used for the wavelength conversion processes.

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