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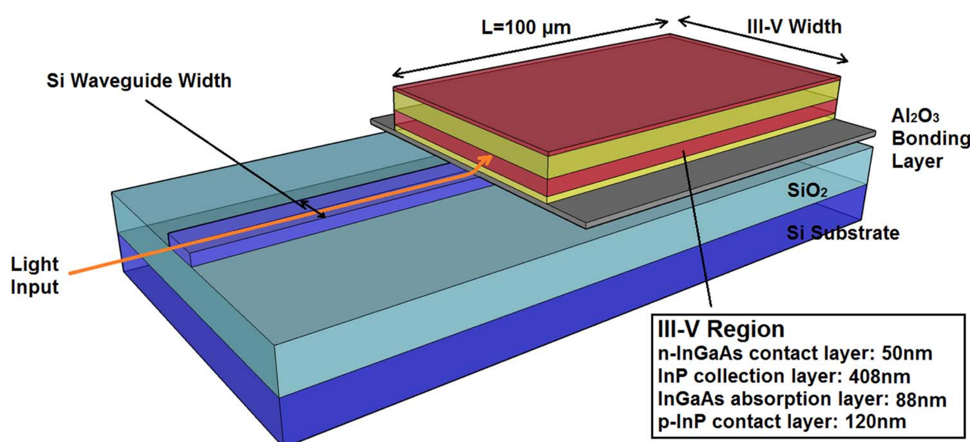

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Design and Analysis of InP-Based Waveguide Uni-Traveling Carrier Photodiode Integrated on Silicon-on-Insulator Through Al_2O_3 Bonding Layer

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Abstract: Thermal resistance and optical evanescent coupling of InP-based waveguide uni-traveling carrier photodiode (UTC-PD) integrated on silicon on insulator (SOI) through novel Al_2O_3 bonding layer have been investigated with a constant heat spreading model and optical beam propagation method (BPM), respectively. Compared to UTC-PD integrated on SOI through conventional SiO_2 bonding layer, there is a significant reduction (up to ∼70.41%) in terms of the total thermal resistance for the same structure through Al_2O_3 bonding layer. On the other hand, based on the evanescent coupling simulation and analysis with BPM, as compared to SiO_2 bonding scheme, no compromise in optical coupling efficiency was found by using Al_2O_3 bonding layer. Our results suggest that Al_2O_3 bonding layer could be a promising candidate for high-power and high-speed III–V photonic devices integrated on SOI, where thermal dissipation is a major concern.

Index Terms: Silicon nanophotonics, photodetectors, uni-traveling carrier photodiodes.

1. Introduction

CMOS compatible silicon photonics technology using silicon-on-insulator (SOI) substrate has advanced rapidly in recent years [1]–[6]. The main drawback of silicon is in light emission and detection. While III–V compound semiconductors are more suitable for light emission and detection application in optical communication system [7], [8]. The heterogeneous integration of III–V materials on SOI through wafer bonding is a promising approach to realize integrated photonic devices with high performances [9], [10]. Generally, SiO_2 is a popular choice as the intermediate bonding layer for high quality wafer bonding [9], [11], [12]. However, the low thermal conductivity of SiO_2 (1.46 W/mK) will affect the heat dissipation [13]. In addition, adhesive bonding with benzocyclobutene (BCB) has also been used to integrate III–V epitaxial structure onto SOI in terms of high bonding strength and bonding quality [5], [14]. Nonetheless, the thermal conductivity of

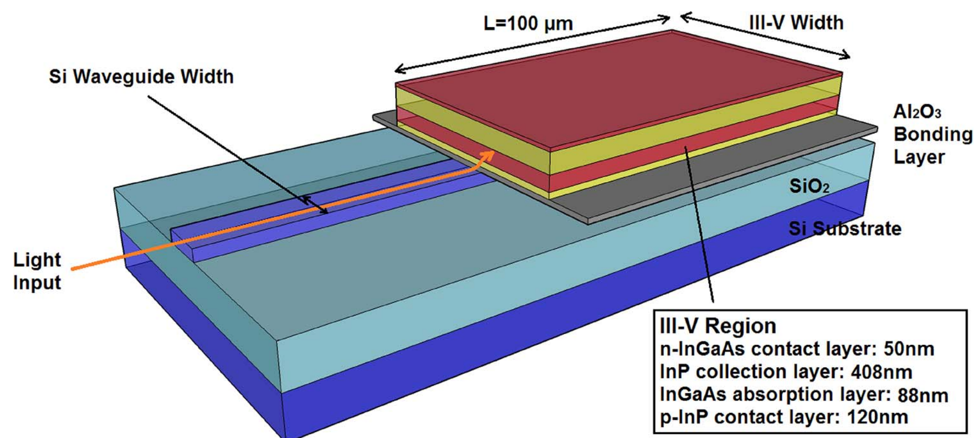

Fig. 1. Schematic of InP-based UTC-PD integrated on SOI through Al_2O_3 bonding layer (not to scale).

BCB (0.29 W/mK) is even poorer [15] and the device heating is a concern for InP/BCB/SOI platform. Recently, we have reported low temperature heterogeneous InP bonding on Si wafer with Al_2O_3 intermediate bonding layer [16], [17]. Al_2O_3 is a promising candidate for intermediate bonding layer with better thermal conductivity (25–50 W/mK) which is at least 17 times higher than that of SiO_2 (1.46 W/mK) [16], [18]. Hence, Al_2O_3 bonding layer has potential applications for improving the performance and reliability of III–V on silicon photonics integrated devices such as semiconductor lasers and photodiodes.

Recently, InP-based waveguide uni-traveling carrier photodiodes (UTC-PDs) integrated on SOI platform has been demonstrated with promising applications [19]. In the UTC-PD, only high-velocity electrons are the active carriers, which increase the device bandwidth and reduce the space charge effect. These factors result in high saturation output power and high speed simultaneously [20]. For high power application, high bias and high optical power are normally applied on the UTC-PD. For example, recently we have demonstrated a high photocurrent of 160 mA under 6.5 V reverse bias voltage from a fabricated top-illuminated InP/InGaAs UTC-PD under optical pumping of 1 W [21]. The device also presented a large 3 dB bandwidth of 62.5 GHz [21]. Significant joule heating are produced which often leads to thermal failure in the realization of compact devices [22]. Therefore, for InP-based UTC-PD integrated on SOI, the thermal property of the device could be the main design concern, which may potentially affect the device performance and reliability. In addition, better thermal conductivity of Al_2O_3 as the bonding layer will also beneficial to other photonic devices integrated on SOI platform, such as laser diodes, whose threshold current and output power are very sensitive to the device heating.

In this work, thermal resistance and optical evanescent coupling of InP-based waveguide UTC-PD integrated on SOI through Al_2O_3 bonding layer have been investigated with a constant heat spreading model and beam propagation method (BPM), respectively. Compared to UTC-PD integrated on SOI with SiO_2 bonding layer, there is a significant reduction up to $\sim$70.41% in terms of the total thermal resistance for the same structure with Al_2O_3 bonding layer. On the other hand, based on the evanescent coupling simulation and analysis with BPM, there is nearly no compromise in optical coupling efficiency by using Al_2O_3 bonding layer. Our results suggest that Al_2O_3 bonding layer could be a promising candidate for high power and high speed III–V photonic devices integrated on SOI in which thermal dissipation is a major concern.

2. Structure Design

The schematic of InP-based UTC-PD integrated on SOI through Al_2O_3 bonding layer is shown in Fig. 1. The proposed structure is designed on a SOI wafer with a 0.22 μm-thick top Si waveguide layer and a 2 μm-thick buried oxide layer. In our UTC-PD structure design, the 80 nm-thick

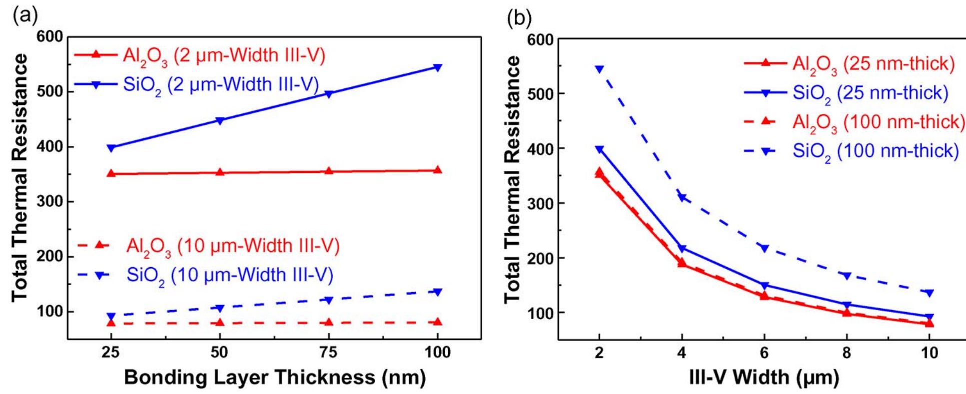

Fig. 2. (a) Calculated total thermal resistance R_{th_total} as a function of bonding layer thickness. (b) Calculated total thermal resistance R_{th_total} as a function of III–V width.

$In_{0.53}Ga_{0.47}As$ layer acts as the absorption region and the 400 nm-thick InP layer functions as the collection region [23]. The specially designed dipole-doped layers, consisting of 8 nm-thick $In_{0.53}Ga_{0.47}As$ layer and 8 nm-thick InP layer, were employed at the $In_{0.53}Ga_{0.47}As$/InP absorption and collection interface to reduce the current blocking [21], [24]. The n-type metal and p-type metal are placed on the 50 nm-thick $In_{0.53}Ga_{0.47}As$ contact layer and 120 nm-thick p-type InP contact layer, respectively. Evanescent coupling is used for the single mode incident light to couple into the III–V region in this structure. The length L of InP-based UTC-PD region is 100 μm. III–V and Si waveguide width are horizontally perpendicular to the light propagation direction. The SOI waveguide is defined by a rib width of 1 μm. The III–V width is varied from 2 μm to 10 μm in accordance with high speed and high photocurrent requirements.

3. Results and Discussion

3.1. Thermal Resistance Analysis

The total thermal resistance of InP-based UTC-PD integrated on SOI using Al_2O_3 or SiO_2 as the bonding layer was calculated by a constant heat spreading model [25]. The total thermal resistance of the device can be represented as the sum of thermal resistance from respective layers. This model has been widely used in hybrid systems and electronic and photonic devices such as metamorphic HBTs and lasers [26], [27]. For the InP-based UTC-PD integrated on SOI structure, light is coupled from beneath SOI waveguide to upper InP-based UTC-PD region, where the heat is produced. Assuming that the SOI wafer is wide enough and the Si has high thermal conductivity (156 W/mK) [28], the total thermal resistance $R_{\mathrm{th_total}}$ for downward transfer of heat flux from the InP-based UTC-PD region to Al_2O_3 or SiO_2 bonding layer can be calculated by

$$R_{\mathrm{th_total}} = R_{\mathrm{th(III-V)}} + R_{\mathrm{th(Al_2O_3/SiO_2)}} \tag{1}$$

where $R_{\mathrm{th(III-V)}}$ is the sum of thermal resistance of the InP-based UTC-PD, including the p-type InP contact layer, the $In_{0.53}Ga_{0.47}As$ absorption layer, and the InP collection layer. $R_{\mathrm{th(Al_2O_3/SiO_2)}}$ is the thermal resistance of the Al_2O_3 or SiO_2 bonding layer. The thermal resistance of each layer can be determined by

$$R_{\mathrm{th}} = \frac{1}{k}\int_0^{H_i} \frac{dx}{(L+2x)(W+2x)} \tag{2}$$

where H_i is the thickness of each layer. k, L, and W are the thermal conductivity, length, and width of a specified slab, respectively. The length of InP-based UTC-PD region L is 100 μm

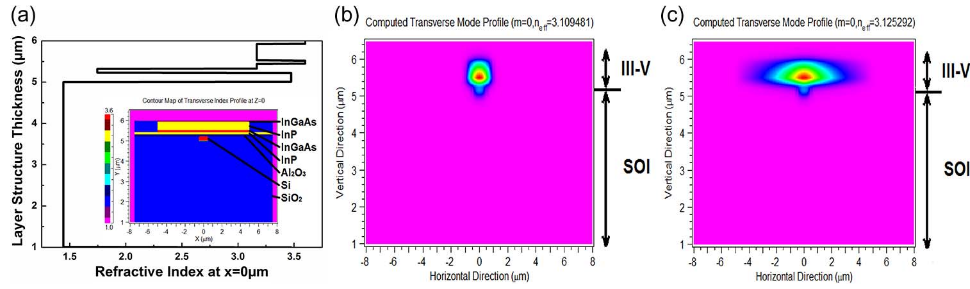

Fig. 3. (a) A refractive index schematic of the InP-based UTC-PD integrated on SOI through Al_2O_3 bonding layer at $x = 0$ μm. (Inset) Cross-section structure of refractive index profile. (b) Mode profile for 2 μm-width III–V width and 100 nm-thick Al_2O_3 bonding layer. (c) Mode profile for 10 μm-width III–V width and 100 nm-thick Al_2O_3 bonding layer.

and width W is varied from 2 μm to 10 μm. The total thermal resistance of the structure along the light propagation was calculated.

Fig. 2(a) and (b) compared the calculated results using (1) and (2) for the total thermal resistance of InP-based UTC-PD integrated on SOI through Al_2O_3 and SiO_2 bonding layers as a function of bonding layer thickness and III–V active region width. Fig. 2(a) shows that, for UTC-PD/SOI with Al_2O_3 bonding layer, the total thermal resistance of the structure is much lower than that with SiO_2 bonding layer. As the bonding layer thickness increases, there is a significant increase in total thermal resistance of the structure using SiO_2 bonding layer. However, the total thermal resistance of the structure with Al_2O_3 bonding layer is less sensitive to the thickness of the bonding layer. Hence, for the design of our InP-based UTC-PD integrated on SOI, it is not a major concern of the device in thermal dissipation if Al_2O_3 bonding thickness is less than 100 nm. In Fig. 2(b), the total thermal resistance of the structure with 10 μm-width III–V UTC-PD is significantly lower than the one with 2 μm-width III–V region. For InP waveguide UTC-PD, wider III–V region is beneficial for high photocurrent application. When the III–V width is 10 μm and bonding thickness is 100 nm, the total thermal resistance of the UTC-PD/SOI with Al_2O_3 bonding layer has a significant reduction $\sim$70.41% than that with SiO_2 bonding layer. This is a significant improvement in thermal dissipation for the integrated device using Al_2O_3 bonding layer.

On the other hand, III–V UTC-PD with narrower waveguide is desirable for high speed application, since the RC limited bandwidth is high as shown in

$$f_{\mathrm{RC}} = \frac{1}{2\pi C_{\mathrm{PD}}(R_s + R_l)} \tag{3}$$

where C_{PD} is the junction capacitance, which is proportional to the device area, R_s is the PD series resistance, and R_l is the load resistance (50 Ohm in our network analyzer). Obviously, narrower III–V UTC-PD will have larger bandwidth.

From Fig. 2(b), it can be seen that, when the width of III–V layer is scaled down to 2 μm, the UTC-PD/SOI with 100 nm Al_2O_3 bonding layer shows a 53% reduction in terms of the total thermal resistance than that using SiO_2 as the bonding layer.

Compared to the UTC-PD/SOI with conventional SiO_2 layer, our design of UTC-PD/SOI via Al_2O_3 bonding layer is beneficial for both high power and high speed device performance in terms of thermal dissipation. In addition, the bonding process using Al_2O_3 layer has no noticeable difficulty, which has been verified by the experimental work carried out in our lab [16]. Furthermore, the process can be easily implemented into fabrication of III–V laser on SOI platform.

3.2. Evanescent Coupling Analysis

Although the use of Al_2O_3 bonding layer can significantly improve the device thermal property, it is yet unclear whether the device performance such as optical coupling efficiency will be compromised or not. BPM is used to analyze the light evanescent coupling from SOI waveguide to

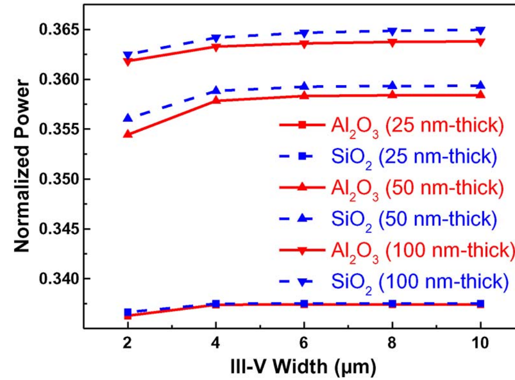

Fig. 4. $In_{0.53}Ga_{0.47}As$ active region power with Al_2O_3 and SiO_2 bonding layer, for various III–V widths and bonding layer thicknesses.

InP-based UTC-PD region at 1.55 μm wavelength with a commercial Rsoft BeamPROP software [29]. A single mode incident light launched from Si waveguide and evanescently coupled to the III–V region, as shown in Fig. 1. In the simulation, the refractive indices of Si and SiO_2 are 3.475 and 1.444, respectively [30]. The refractive index of 1.74618 is used for the Al_2O_3 bonding layer, which is between a high index p-type InP layer ($n_{InP} = 3.1681$) and a Si waveguide [31], [32]. A refractive index schematic of the InP-based UTC-PD integrated on SOI through Al_2O_3 bonding layer structure at $x = 0$ μm is illustrated in Fig. 3(a) and refractive index profile using BPM is presented in the inset. In order to design the structure, we need to ensure that enough optical mode overlap with the active region which can be absorbed effectively. The fundamental mode profiles in the coupled waveguide structure using 2D modesolver are calculated as an example in Fig. 3(b) and (c). It can be seen that almost all the transverse electric (TE) mode fields reside in III–V active region, when the III–V width is 2 μm and 10 μm. Therefore, the proposed design illustrates the optical mode could experience maximal absorption in the III–V region.

To investigate the coupling efficiency between active and passive materials, coupled normalized power Γ_i in a given region in the x–y transverse plane is calculated using

$$\Gamma_i = \frac{\int_{H_i} |E_x|^2 dy}{\int |E_x|^2 dy} \tag{4}$$

where H_i is thickness of the III–V active region, and E_x is the electromagnetic field of the optical mode over the x–y plane.

The optical power in the $In_{0.53}Ga_{0.47}As$ active region (UTC-PD absorption region) was computed. Fig. 4 compares the normalized power coupled into $In_{0.53}Ga_{0.47}As$ region for the InP-based UTC-PD on SOI with Al_2O_3 and SiO_2 bonding layers. As the bonding layer thickness increases, there is only a slight increase in normalized power in the $In_{0.53}Ga_{0.47}As$ active region. Furthermore, for a given III–V width, the difference of normalized power between the devices using SiO_2 and Al_2O_3 bonding layers is negligible ($> 0.1\%$). Therefore, by using a high thermal conductivity Al_2O_3 as the bonding layer for the InP-based UTC-PD on SOI, we would not expect any compromise in device optical performance.

4. Conclusion

In this work, thermal resistance and optical evanescent coupling efficiency of InP-based waveguide UTC-PD integrated on SOI through Al_2O_3 bonding layer have been investigated with a constant heat spreading model and BPM, respectively. Compared to UTC-PD integrated on SOI with SiO_2 bonding layer, there is a significant reduction up to $\sim$70.41% in terms of the total thermal resistance for the same structure with Al_2O_3 bonding layer. On the other hand, based on the evanescent coupling simulation and analysis with BPM, no compromise in optical coupling

efficiency was found by using Al_2O_3 bonding layer. The results suggest that Al_2O_3 bonding layer could be a promising candidate for high power and high speed III–V photonic devices integrated on SOI in which thermal dissipation is a major concern.

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