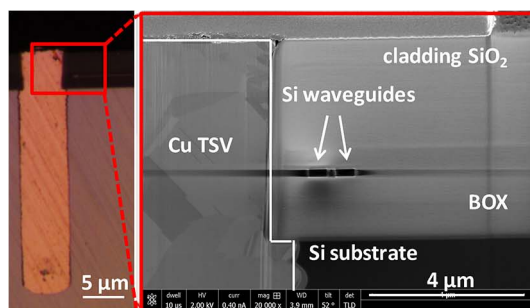


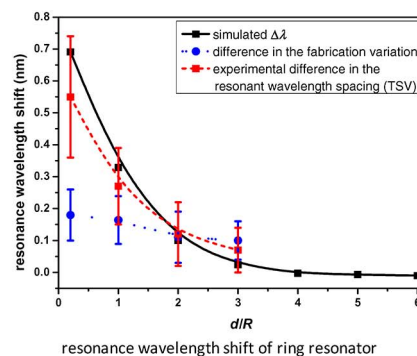
# Through-Si-via (TSV) Keep-Out-Zone (KOZ) in SOI Photonics Interposer: A Study of the Impact of TSV-Induced Stress on Si Ring Resonators

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Microscope image of the cross-section of SOI photonics TSV interposer (inset: TEM image of the coupling region)



# Through-Si-via (TSV) Keep-Out-Zone (KOZ) in SOI Photonics Interposer: A Study of the Impact of TSV-Induced Stress on Si Ring Resonators

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**Abstract:** Si photonic devices are sensitive to the change in refractive index on the Si-on-insulator (SOI) platform. One of the critical limitations in the compact 3D photonic integration circuit is the through-Si-via (TSV)-induced stress, which affects the performances of Si photonic devices integrated in interposer. We build a model to analyze and simulate the wavelength shift of the ring resonator caused by the effective-refractive-index change in the waveguide, arising from TSV-induced stress in the SOI interposer. Double-cascaded ring resonators integrated in the SOI interposer were fabricated and their wavelength shifts were characterized. The results show that the resonance wavelength shift on the order of 0.1 nm can be caused by the TSV-induced stress for  $d/R < 3$ , where  $d$  and  $R$  are the distance between the TSV and the Si waveguide, and the radius of TSV, respectively. This shift results in performance deviation from the target of design. Finally, this paper proposes a TSV keep-out-zone for the Si photonic ring resonator and a compact scaling of the SOI photonics interposer.

**Index Terms:** Silicon nanophotonics, fabrication and characterization.

## 1. Introduction

Si photonics has been intensively researched and developed as it provides a low-cost and power efficient solution for next generation interconnect technology based on on-chip, chip-to-chip, and long-haul optical communication [1]–[9]. A multifunctional platform requires photonics and complementary metal–oxide–semiconductor (CMOS) circuits to be integrated in a same system. To achieve advantages of power efficiency and bandwidth densities of photonics, monolithic integration of CMOS circuits and Si photonics functional blocks has been explored and recently demonstrated [10]–[15]. However, this approach requires an increased number of mask layers to fabricate CMOS-integrated Si photonics chips, and it also needs sophisticated co-integration processing skills to integrate them together on the same Si chip. Consequently, it is difficult to achieve high overall yield [16]–[18]. Moreover, the huge size mismatch between CMOS and photonics functional blocks is another disadvantage of the monolithic integration approach. The large footprint of Si photonics blocks can easily consume most of the die space, leaving little space for other electronics functional

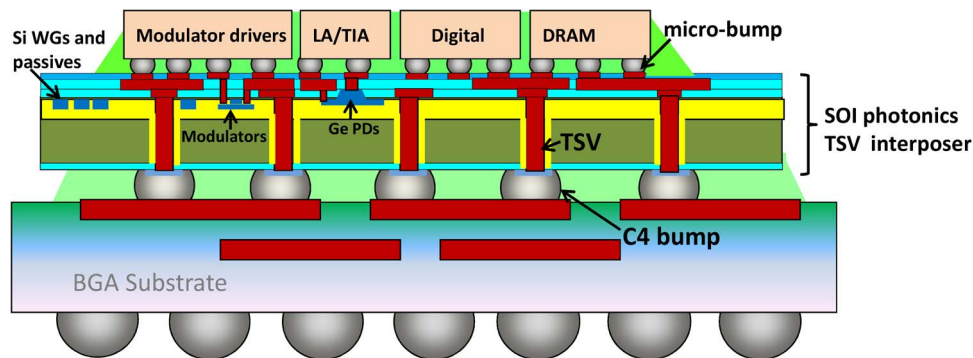


Fig. 1. Schematic of SOI photonics TSV interposer in 3D CMOS-photonics integration system.

blocks, e.g., digital, radio frequency, and high-voltage, to be placed. Some researchers [16], [17], [19] have proposed to separate the fabrication of Si photonics and CMOS electronics, and finally integrate them together using through-Si-via (TSV) and micro-bump interconnect, which is a 3D integration scheme. In this paper, we proposed a Si-on-insulator (SOI) photonics TSV interposer, in which TSVs are fabricated in an SOI photonics wafer. As shown in Fig. 1, in this scheme, high density Cu wirings and micro-bumps provide interconnection among guest dies, and TSVs communicate with I/O ports on the organic package (e.g., fc-BGA) and/or printing circuit board (PCB), whereas Si photonic devices deal with huge amount of data transmitted in from and out to the external world.

TSV is a key technology in the 3D integration, which provides flexible and compact electrical/physical connectivity between different chips [20]. In electronics 3D integration using TSV, the impact of TSV-induced stress on transistors has been intensively investigated [21]. However, how to place TSVs in the presence of Si photonic device is something that is missing in the literatures. To realize compact scaling, which is one of the important benefits of 3D integration, high-density TSVs are situated close to the Si photonic devices. One of the critical limitations in the compact 3D photonics integration is the TSV-induced stress, which affects the performance of Si photonic devices integrated in interposer, particularly for the stress-sensitive devices, such as Si photonic ring resonators. One example is the resonance wavelength shift arising from the effective-refractive-index change in the waveguide, which results from TSV-induced stress due to the different coefficients of thermal expansion (CTEs) between Cu and Si/SiO<sub>2</sub> of interposer. This shift results in a performance deviation from the design target.

Some works have been reported on TSV-induced stress models [20], [22], [23]. These models are based on the 2D plane-strain solution to the classical Lamé problem in elasticity [24], namely, the approximation of an infinitely long fiber (TSV) in an infinite matrix (Si wafer), which are, however, not suitable for the SOI photonics TSV interposer, which consists of buried oxide (BOX) and cladding oxide, Si substrate and TSV with finite depth.

In this paper, the impact of TSV-induced stress on Si photonic devices in SOI photonics interposer is analyzed. The model of TSV-induced stress distribution in the Si waveguide in SOI photonics interposer is built. The model of the effective-refractive-index change caused by the stress-induced changes of refractive index tensors is also presented. We have also fabricated and characterized Si photonic double-cascaded ring resonators integrated with TSV structures on an SOI platform to demonstrate the impact of TSV-induced stress, because the ring resonator is one of the most stress-sensitive Si photonic devices. The characterization results are statistically analyzed with the impact of fabrication nonuniformity eliminated. Finally, this paper proposes a stress aware design framework and a TSV keep-out-zone (KOZ) for the Si photonic ring resonator. A compact scaling of SOI photonics interposer is ultimately achieved.

## 2. Theoretical Model and Simulation

Thermal stress is induced during the TSV fabrication due to the mismatch in the CTEs of the TSV material (Cu) and Si/SiO<sub>2</sub>. The stress in the waveguide induced by TSV with different positions in

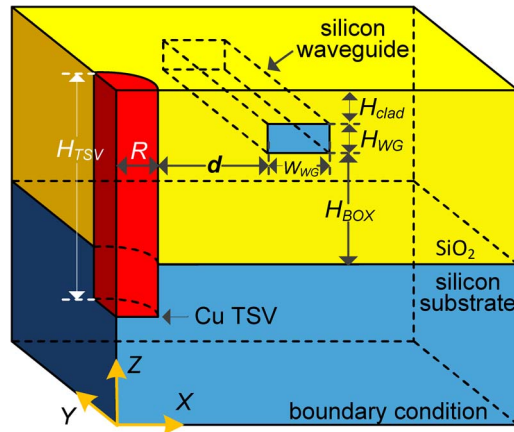


Fig. 2. Schematic of the 3D FEA model of SOI photonics TSV interposer. Due to the symmetry considerations, only a quarter of the structure is simulated. The geometries are not to scale.

the interposer has been numerically analyzed by the 3D finite element analysis (FEA) method. The refractive index changes due to TSV-induced stress tensors are modeled by the stress-optic constants, and, meanwhile, the relationship between effective refractive index in the SOI waveguide and the refractive index tensors are modeled by the mode solver. The resonant wavelength shift of the ring resonator arising from the change in the effective refractive index is simulated by the finite-difference time-domain (FDTD) method.

### 2.1. 3D FEA Model and Simulation of TSV-Induced Stress

The stress distribution in SOI photonics interposer is numerically analyzed by the 3D FEA method using the commercial software Mechanical APDL (ANSYS) 14.0. The schematic of the 3D FEA model of SOI interposer is shown in Fig. 2, which illustrates a quarter of the interposer due to the symmetry consideration. The boundary condition is set at the plane of  $x = 0$ ,  $y = 0$ , and  $z = 0$  to reduce the calculation load that depends on its symmetrical structure. The simulation window is set to be  $50 \mu\text{m} \times 50 \mu\text{m} \times 50 \mu\text{m}$  to avoid the impact of boundary condition on the stress distribution in the waveguide. The thermal load is set to be annealed at  $350^\circ\text{C}$  and cooled to room temperature of  $25^\circ\text{C}$ . The elastic mismatch between Cu and Si/SiO<sub>2</sub> is negligible in this 3D FEA model. A very thin Ti layer between Cu via and SiO<sub>2</sub> is used as a diffusion barrier in the actual experiment. However, the stress caused by the Ti layer is very small and it is thus neglected in the simulation model. The symbol denotations, the material properties, and other parameters used in simulation are listed in Table 1.

The variables in this simulation are  $d/R = 0.2/1/2/3/4/5/6$ . Fig. 3 shows the simulated contour plot of stress distribution in the TSV and the waveguide layer in the SOI interposer (only  $\sigma_{xx}$  with  $d/R = 0.2$  is presented). It shows that the stress can reach the order of 100 MPa. The mesh volume-weighted mean stress in the waveguide in the range of  $y \leq 2.5 \mu\text{m}$  is calculated from the contour plot, which covers the coupling region of the ring resonator in the following simulation. To extract the TSV-induced stress, the residual thermal stress distribution in SOI photonics interposer without TSV, which is caused by the difference in the CTEs of Si and SiO<sub>2</sub>, is also analyzed for comparison by the 3D FEA method. The mesh volume-weighted mean stresses of the waveguide in the SOI interposer without TSV are  $\sigma_{xx} = -4.8 \text{ MPa}$ ,  $\sigma_{yy} = 22.7 \text{ MPa}$ ,  $\sigma_{zz} = 25.9 \text{ MPa}$ , and  $\sigma_{xy} = 0.2 \text{ MPa}$ . Positive stress represents “tension,” whereas negative stress represents “compression.” Based on the superposition principle [23], the TSV-induced weighted mean stress is calculated by deducting the weighted mean stress of the interposer without TSV. The TSV-induced weighted mean stresses in the waveguide are summarized in Fig. 4. As the waveguide is usually very long in the Z direction as shown in Fig. 2, the shear stresses in this direction, namely,

TABLE 1

Symbols denotation, material properties, and other parameters used in the simulation

Symbol	Denotation	Material property and other parameters
$\sigma_{xx}/\sigma_{yy}/\sigma_{zz}$	normal stress along the $X/Y/Z$ direction	
$\sigma_{xy}$	shear stress in the $XY$ plane	
$\Delta T$	thermal load	$\Delta T = 25^\circ\text{C} - 350^\circ\text{C} = -325^\circ\text{C}$ (interposer was annealed at $350^\circ\text{C}$ and cooled to $25^\circ\text{C}$ )
$E_f/E_m/E_o$	Young's modulus of the Cu / Si / $\text{SiO}_2$ respectively	1.17e5 MPa / 1.31e5 MPa / 0.73e5 MPa
$\nu_f/\nu_m/\nu_o$	Poisson's ratio of the Cu / Si / $\text{SiO}_2$ respectively	0.35 / 0.28 / 0.17
$\alpha_f/\alpha_m/\alpha_o$	coefficient of thermal expansion (CTE) of the Cu / Si / $\text{SiO}_2$ respectively	17 ppm/ $^\circ\text{C}$ / 2.8 ppm/ $^\circ\text{C}$ / 0.5 ppm/ $^\circ\text{C}$
$W_{WG}$	width of the waveguide	$0.5 \mu\text{m}$
$H_{WG}$	height of the waveguide	$0.22 \mu\text{m}$
$H_{BOX}$	height of the buried oxide (BOX)	$2 \mu\text{m}$
$H_{clad}$	height of the cladding oxide	$3 \mu\text{m}$
$H_{TSV}$	depth of TSV	$30 \mu\text{m}$
$R$	radius of TSV	$2.5 \mu\text{m}$
$d$	the edge-to-edge distance between the TSV and the Si waveguide	$0.5 \mu\text{m} / 2.5 \mu\text{m} / 5 \mu\text{m} / 7.5 \mu\text{m} / 10 \mu\text{m} / 12.5 \mu\text{m} / 15 \mu\text{m}$
$d/R$		0.2 / 1 / 2 / 3 / 4 / 5 / 6

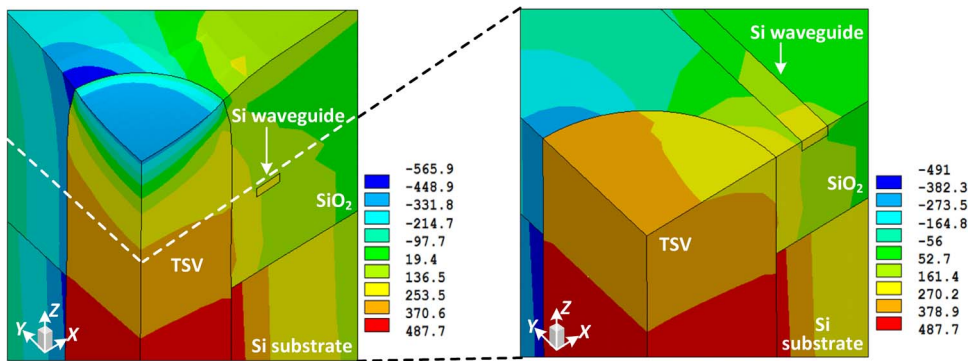


Fig. 3. Contour plot of stress distribution in the TSV and Si waveguide ( $d/R = 0.2, \sigma_{xx}$ ).

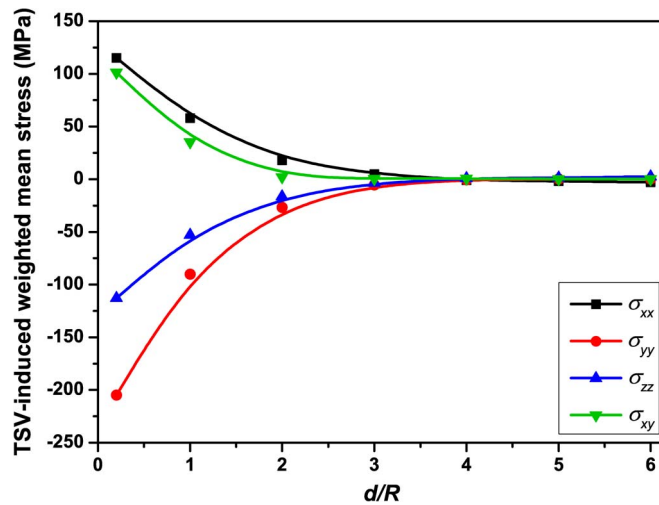


Fig. 4. TSV-induced weighted mean stress in the waveguide in the SOI interposer.

TABLE 2

Photo-elastic constants of Si [26]

material	refractive index <sup>a</sup> $n_0$	strain-optic constants <sup>b</sup>			stress-optic constants		
		$p_{11}$	$p_{12}$	$p_{44}$	$C_1$ ( $10^{-12}$ /Pa)	$C_2$ ( $10^{-12}$ /Pa)	$C_3$ ( $10^{-12}$ /Pa)
Si	3.476	-0.101	0.0094	-0.0552	-11.35	3.65	-23.72

<sup>a</sup> Measured at wavelength  $\lambda = 1.55 \mu\text{m}$ <sup>b</sup> Measured at wavelength  $\lambda = 1.15 \mu\text{m}$ 

$\sigma_{yz}$  and  $\sigma_{xz}$ , are negligible in this paper. Note that the TSV-induced weighted mean stress can reach from several MPa to hundreds MPa for  $d/R < 3$ .

## 2.2. Change in Effective Refractive Index Caused by the Stress-Induced Change in Refractive Index Tensors

The phase of photonic devices is affected by the refractive index of the waveguide, which can be changed by stress due to the photo-elastic effect. The stress-induced change in refractive index tensors is modeled by the stress-optic constants, which are expressed in Eq. (1)–(4) [25].  $\Delta n_{yz}$  and  $\Delta n_{xz}$  are negligible in this paper because the waveguide is very long in the  $Z$  direction, i.e.,

$$\Delta n_{xx} = n_{xx} - n_0 = -C_1 \sigma_{xx} - C_2 (\sigma_{yy} + \sigma_{zz}) \quad (1)$$

$$\Delta n_{yy} = n_{yy} - n_0 = -C_1 \sigma_{yy} - C_2 (\sigma_{xx} + \sigma_{zz}) \quad (2)$$

$$\Delta n_{zz} = n_{zz} - n_0 = -C_1 \sigma_{zz} - C_2 (\sigma_{xx} + \sigma_{yy}) \quad (3)$$

$$\Delta n_{xy} = n_{xy} - 0 = -C_3 \sigma_{xy}. \quad (4)$$

In the preceding equation,  $n_{xx}$ ,  $n_{yy}$ ,  $n_{zz}$ , and  $n_{xy}$  are refractive index tensors, and  $n_0$  is the refractive index without stress.  $C_1 = n_0^3(p_{11} - 2\nu p_{12})/2E$ ,  $C_2 = n_0^3[-\nu p_{11} + (1 + \nu)p_{12}]/2E$  and  $C_3 = n_0^3 p_{44}/2G$  are the stress-optic constants related to the Young's modulus, Poisson's ratio, and the strain-optic constants ( $p_{11}$ ,  $p_{12}$  and  $p_{44}$ ), respectively. For isotropic crystals,  $p_{44} = (p_{11} - p_{12})/2$  and  $G = E/2/(1 + \nu)$  [25]. The photo-elastic constants of Si are listed in Table 2 [26]. The stress-optic constants in Table 2 may not be accurate at  $1.55 \mu\text{m}$ , because they are derived from the strain-optic constants measured at  $1.15 \mu\text{m}$ . However, the dispersion is expected to be weak since the strong electronic transitions occur at the shorter wavelengths for both Si and  $\text{SiO}_2$  [26]. The stress-optic constants of  $\text{SiO}_2$  are ten times less than that of Si; therefore, the stress-induced changes of refractive index tensors of  $\text{SiO}_2$  are not considered in this paper. The changes of refractive index tensors calculated based on the weighted mean stresses in the Si waveguide are shown in Fig. 5. It shows that  $\Delta n_{xx}$ ,  $\Delta n_{yy}$ ,  $\Delta n_{zz}$ , and  $\Delta n_{xy}$  decrease from the order of  $10^{-3}$  at  $d/R = 0.2$  to about zero at  $d/R = 3$ , and they are negligible for  $d/R > 3$ .

Si waveguide is anisotropic under the TSV-induced stress. For anisotropic materials, the electric field ( $E$ ) and the electric displacement field ( $D$ ) are not parallel, and they are related by the permittivity tensor  $\varepsilon$  (a second-order tensor) [27]. As discussed before, the shear stresses ( $\sigma_{yz}$  and  $\sigma_{xz}$ ) in the  $Z$  direction are very small, and hence, the refractive index tensors ( $n_{yz}$  and  $n_{xz}$ ) are negligible.  $E_y$  can be negligible for transverse electric (TE) mode (electric field along  $X$  axis in Fig. 2); thus, the relation between  $E$  and  $D$  can be expressed as Eq. (5), i.e.,

$$\begin{pmatrix} D_x \\ D_y \\ D_z \end{pmatrix} = \begin{pmatrix} n_{xx}^2 & n_{xy}^2 & 0 \\ n_{xy}^2 & n_{yy}^2 & 0 \\ 0 & 0 & n_{zz}^2 \end{pmatrix} \begin{pmatrix} E_x \\ 0 \\ E_z \end{pmatrix}. \quad (5)$$

Therefore, the change in effective-refractive-index ( $\Delta n_{\text{eff}}$ ) for the TE mode is mainly caused by  $\Delta n_{xx}$ ,  $\Delta n_{xy}$ , and  $\Delta n_{zz}$ , which can be expressed as Eq. (6). It is in agreement with the results simulated using mode solver of Rsoft commercial software. The corresponding fitting results

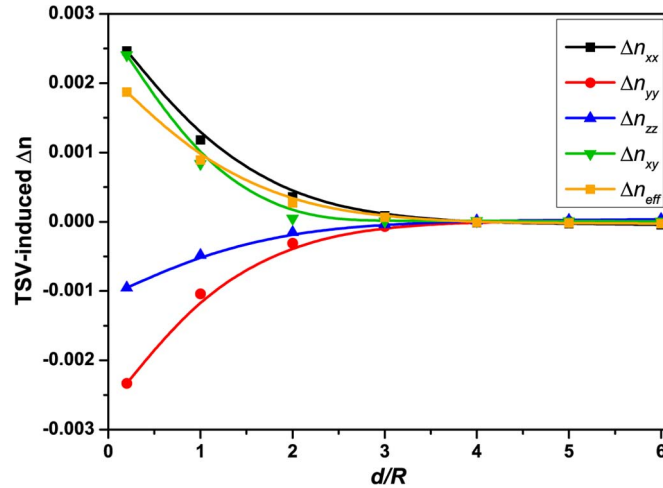


Fig. 5. TSV-induced changes of refractive index tensors and effective refractive index.

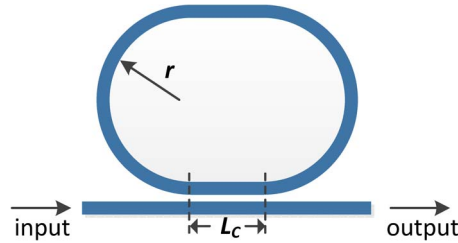


Fig. 6. Schematic of the Si photonic ring resonator.  $L_c$  represents the coupling length, and  $r$  represents the radius of the ring.

simulated using mode solver are expressed as Eq. (7). According to Eqs. (1), (3), and (7), the model for stress-induced  $\Delta n_{eff}$  can be derived as Eq. (8), i.e.,

$$\Delta n_{eff} = \frac{\partial n_{eff}}{\partial n_{xx}} \Delta n_{xx} + \frac{\partial n_{eff}}{\partial n_{xy}} \Delta n_{xy} + \frac{\partial n_{eff}}{\partial n_{zz}} \Delta n_{zz} \quad (6)$$

$$\Delta n_{eff} = a_1 \cdot \Delta n_{xx} + a_2 \cdot \Delta n_{xy} + a_3 \cdot \Delta n_{zz} \quad (7)$$

$$\Delta n_{eff} = - \left[ (a_1 C_1 + a_3 C_2) \sigma_{xx} + (a_1 C_2 + a_3 C_2) \sigma_{yy} + (a_1 C_2 + a_3 C_1) \sigma_{zz} \right] \quad (8)$$

where  $a_1 = 0.843941$ ,  $a_2 = 0$ , and  $a_3 = 0.218913$  for TE mode. The modeling result of  $\Delta n_{eff}$  is also shown in Fig. 5.

### 2.3. Simulation of TSV Impact on Si Photonic Ring Resonator

Effective-refractive-index ( $n_{eff}$ ) is a critical parameter of photonic devices. According to  $\Delta \lambda = \Delta n_{eff} \lambda / n_g$  [28], where  $\lambda$  the wavelength and  $n_g$  the group index,  $\Delta n_{eff}$  can result in a wavelength shift of the device and hence affect the device optical performance. As discussed before,  $\Delta n_{eff}$  can be caused by the TSV-induced stress. A group of TSV designs with different  $d/R$  values (from 0.2 to 6) are considered in our simulation. Based on the modeling result of stress-induced  $\Delta n_{eff}$  in Fig. 5, the wavelength shift of the ring resonator is simulated using the FDTD method. The schematic of the Si photonic ring resonator is presented in Fig. 6, which includes a transmission waveguide, a ring cavity, and a coupling region. The parameters of the simulated ring resonator are  $L_c = 2 \mu\text{m}$  and  $r = 5 \mu\text{m}$ , and the gap between ring and waveguide is  $0.2 \mu\text{m}$ .

The simulated spectra are shown in Fig. 7(a). The wavelength shift of the ring resonator caused by the TSV-induced stress is shown in Fig. 7(b). The results show that the ring resonator

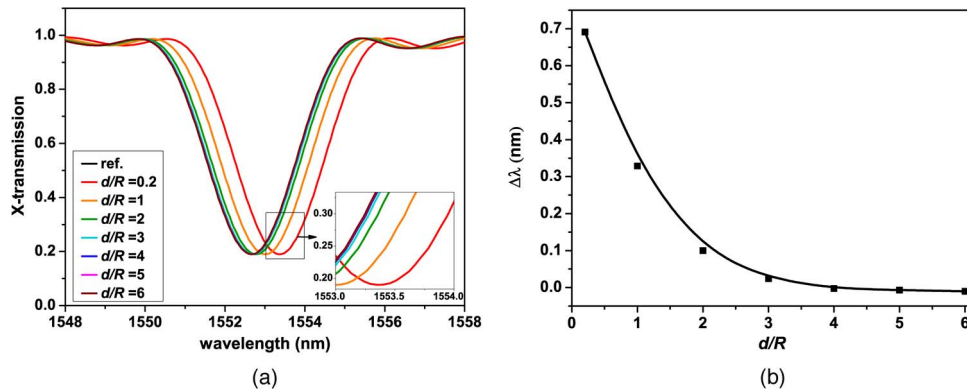


Fig. 7. Simulated wavelength shift of a Si photonic ring resonator. (a) Ring resonator spectra. (b) Ring resonator wavelength shift.

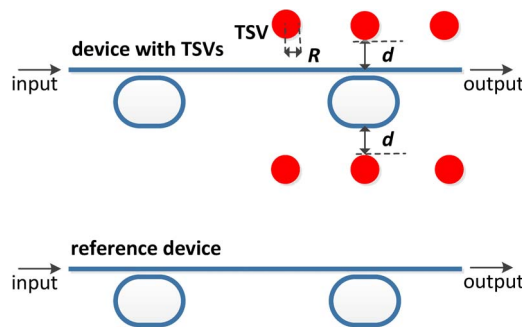


Fig. 8. Schematic of two double-cascaded ring resonators for testing the TSV impact. The geometries are not to scale.

wavelength shift decreases from the order of 0.1 nm to the order of 0.01 nm with increasing  $d/R$ . In optical communications systems, the spacing of dense wavelength division multiplexing defined by ITU is typically 100 GHz (0.8 nm) or 50 GHz (0.4 nm) [29], [30]. Therefore, wavelength shift on the order of 0.1 nm results in the performance deviation from the designed objective, and the wavelength shift is negligible for  $d/R > 3$ . Hence, this paper proposes the TSV KOZ for the Si photonic ring resonator in the SOI interposer of  $d/R < 3$ , in order to keep resonant wavelength shifts one order smaller than 0.1 nm.

### 3. Fabrication and Characterization

We fabricated and characterized Si photonic double-cascaded ring resonators integrated with TSV structures on an SOI platform to demonstrate the impact of TSV-induced stress, because ring resonator is one of the most stress-sensitive Si photonic devices. The characterization results are statistically analyzed with the impact of fabrication nonuniformity eliminated.

#### 3.1. Design of Experiment and Fabrication

We design an SOI photonics interposer integrated with Si photonic ring resonators and TSVs to verify the impact of TSV-induced stress on the optical performance of the Si photonic device. However, the optical performance of the ring resonator is sensitive to the fabrication variation. In order to minimize the ring performance variation caused by the fabrication nonuniformity, a double-cascaded ring resonator is used, as shown in Fig. 8. Fig. 8 includes two double-cascaded ring resonators, where one device is integrated with TSVs and the other is without TSVs that serves as a reference. The TSV-induced stress changes the resonated wavelength spacing of the two ring



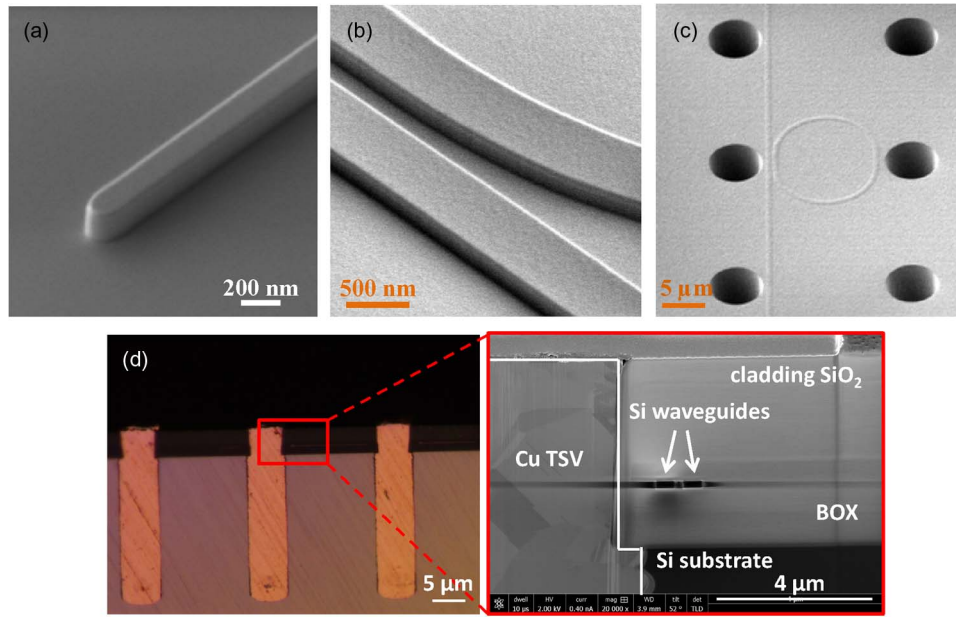


Fig. 9. (a) SEM image of waveguide tip. (b) SEM image of coupling region of the ring resonator. (c) SEM image of the ring resonator integrated with etched TSV in the SOI interposer. (d) Microscope image of the cross-section of SOI photonics TSV interposer (inset: TEM image of the coupling region).

resonators. The difference of the resonated wavelength spacing between the two devices can be extracted to study the impact of TSV-induced stress. All rings in the two devices are put as closely as possible to further minimize any fabrication variation. The distance between the cascaded rings is  $150\ \mu\text{m}$ . The parameters of the single ring resonator are the same as the parameters of the ring resonator simulated, namely,  $L_c = 2\ \mu\text{m}$ ,  $r = 5\ \mu\text{m}$  and the gap between ring and waveguide is  $0.2\ \mu\text{m}$ . A center-to-center pitch of TSVs of  $6R$  ( $R = 2.5\ \mu\text{m}$ ) is designed; and different splits of  $d/R$  are designed, including  $d/R = 0.2$ ,  $d/R = 1$ ,  $d/R = 2$ , and  $d/R = 3$ .

The devices were fabricated on an 8-in SOI wafer with a 220-nm top Si layer and a  $2\ \mu\text{m}$  BOX. First, the Si waveguide ring resonators were formed by a dry etching process. Tilted scanning electron microscope (SEM) images of the waveguides are shown in Fig. 9. The tip width is about 200 nm for coupling with lensed fibers, as shown in Fig. 9(a). Fig. 9(b) shows the SEM image of the coupling region of the ring resonator. With a  $4\text{-}\mu\text{m}$ -thick photo resistance pattern,  $30\text{-}\mu\text{m}$ -deep TSVs were etched through after the waveguide formation. The vertical and smooth sidewall of TSV in the SOI interposer is shown in Fig. 9(c). A  $1\text{-}\mu\text{m}$ -thick  $\text{SiO}_2$  was deposited by the plasma-enhanced chemical vapor deposition method on the sidewall of TSV for isolation. A 200-nm-thick Ti layer was then deposited by the physical vapor deposition (PVD) method as a diffusion barrier. Another  $3\text{-}\mu\text{m}$ -thick PVD Cu seed layer was deposited on the Ti barrier layer. Cu electrochemical-plating was carried out to fully fill the TSV. Finally, the wafer was annealed at  $350\ ^\circ\text{C}$  followed by chemical mechanical polishing. The microscope image of the cross-section of SOI photonics interposer integrated with copper TSVs and the transmission electron microscope (TEM) image are shown in Fig. 9(d). Fig. 9(d) shows the TSV is fully filled with copper. The inset shows the cross-section of the device with TSV.

### 3.2. Characterization

Agilent optical measurement system (photonic dispersion and loss analyzer) was used to characterize the optical performances of two devices with/without TSV structures at room temperature. The optical measurements were performed after selecting the TE polarization. The typical spectra of four groups of devices fabricated for testing the TSV impact are shown in Fig. 10. Each group includes two spectra, with one belonging to the device with TSVs, and the other belonging to the

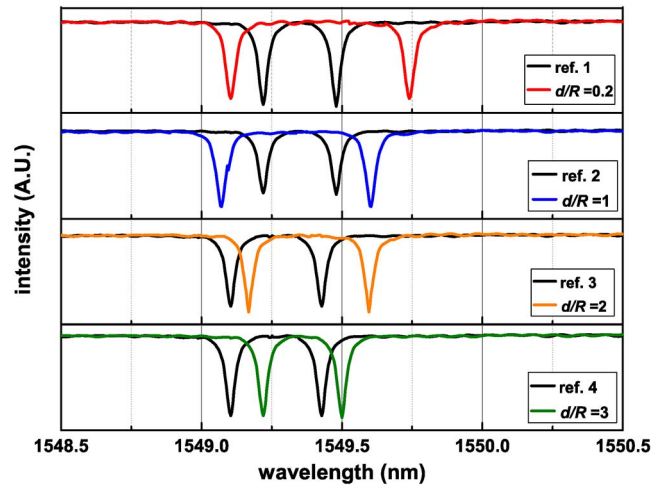


Fig. 10. Optical spectra of double-cascaded ring resonators with/without TSV structures.

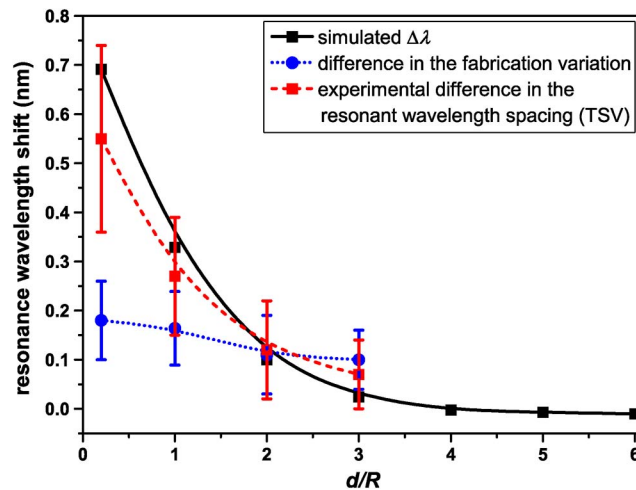


Fig. 11. Simulated and experimental resonance wavelength shift of the ring resonator.

reference device without TSV. Compared with the reference devices, there are changes to the wavelength spacing of each device with TSVs. The results show that the TSV-induced stress causes a wavelength shift of the ring resonators. The differences in the resonant wavelength spacing are statistically analyzed from 15 samples for each group. In order to consider fabrication variation in the different die locations, another four groups of two double-cascaded ring resonators without any TSVs were fabricated, and the differences in the resonant wavelength spacing are also statistically analyzed from 15 samples of each group. The measurement results are shown in Fig. 11, including the simulated results.

For the four groups of devices without any TSVs, the average differences in the resonant wavelength spacing between the device and the reference is  $\sim 0.15$  nm and the deviation is  $\sim 0.07$  nm. The results show that in the absence of TSV-induced stress, the difference in the wavelength spacing of the double-cascaded ring resonators between the device and the reference is relatively constant. For the four groups of devices with TSVs, the average differences in the resonant wavelength spacing between the devices with TSVs and the reference devices are obviously different. With increasing  $d/R$ , the average difference reduces from 0.55 to 0.07 nm, with a deviation reducing from 0.19 to 0.07 nm. The result of wavelength spacing change shows that the TSV-induced

stress impact on the optical device becomes stronger when the TSV structure is closer to the optical device. When the distance between the TSV and the waveguide is more than  $7.5 \mu\text{m}$  ( $d/R = 3$ ), the stress impact on the optical device is negligible. The experimental results are basically in agreement with the analysis in the above model. In conclusion, the TSV KOZ for the Si photonic ring resonator in SOI photonics interposer has been experimentally demonstrated.

#### 4. Conclusion

An SOI photonics TSV interposer has been proposed. The impact of TSV-induced stress on the optical performance of the photonic devices has been theoretically investigated as well as experimentally demonstrated for the first time in this paper. The TSV-induced stress in the waveguide has been numerically analyzed by the 3D FEA method. The refractive index changes due to TSV-induced stress tensors are modeled by the stress-optic constants, and meanwhile the relationship between the effective refractive index in SOI waveguide and the refractive index tensors are modeled by the mode solver. The resonant wavelength shift of the ring resonator arising from the change in the effective refractive index is simulated by the FDTD method. Experimentally, an SOI photonics interposer demo has been fabricated using a CMOS-compatible integration process. The TSV-induced resonance wavelength shift has been characterized and the experimental results are basically in agreement with the analysis in the proposed model. Finally, this paper proposes the TSV KOZ for the Si photonic ring resonator in the SOI interposer of  $d/R < 3$ , in order to keep resonant wavelength shifts one order smaller than 0.1 nm.

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#### References

- [1] I. A. Young, E. Mohammed, J. T. S. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, and P. L. D. Chang, "Optical I/O technology for tera-scale computing," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 235–248, Jan. 2010.
- [2] R. Soref, "The past, present, and future of silicon photonics," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1678–1687, Nov./Dec. 2006.
- [3] B. Jalali and S. Fathpour, "Silicon photonics," *J. Lightw. Technol.*, vol. 24, no. 12, pp. 4600–4615, Dec. 2006.
- [4] G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. Bowers, "III-V/silicon photonics for on-chip and intra-chip optical interconnects," *Laser Photon. Rev.*, vol. 4, no. 6, pp. 751–779, Jan. 2010.
- [5] A. V. Krishnamoorthy, R. Ho, X. Zheng, H. Schwetman, J. Lexau, P. Koka, G. Li, I. Shubin, and J. E. Cunningham, "Computer systems based on silicon photonic interconnects," *Proc. IEEE*, vol. 97, no. 7, pp. 1337–1361, Jul. 2009.
- [6] A. Shacham, B. G. Lee, A. Biberman, K. Bergman, and L. P. Carloni, "Photonic NoC for DMA communications in chip multiprocessors," in *Proc. HotI, 2007*, pp. 29–38.
- [7] A. Biberman, S. Manipatruni, N. Ophir, L. Chen, M. Lipson, and K. Bergman, "First demonstration of long-haul transmission using silicon microring modulators," *Opt. Exp.*, vol. 18, no. 15, pp. 15544–15552, Jul. 2010.
- [8] A. Joshi, C. Batten, Y. Kwon, S. Beamer, I. Shamim, K. Asanovic, and V. Stojanovic, "Silicon-photonic cros networks for global on-chip communication," in *Proc. NoCS, 2009*, pp. 124–133.
- [9] Y. Urino, Y. Noguchi, M. Noguchi, M. Imai, M. Yamagishi, S. Saitou, N. Hirayama, M. Takahashi, H. Takahashi, E. Saito, M. Okano, T. Shimizu, N. Hatori, M. Ishizaka, T. Yamamoto, T. Baba, T. Akagawa, S. Akiyama, T. Usuki, D. Okamoto, M. Miura, J. Fujikata, D. Shimura, H. Okayama, H. Yaegashi, T. Tsuchizawa, K. Yamada, M. Mori, T. Horikawa, T. Nakamura, and Y. Arakawa, "Demonstration of 12.5-Gbps optical interconnects integrated with lasers, optical splitters, optical modulators and photodetectors on a single silicon substrate," *Opt. Exp.*, vol. 20, no. 26, pp. B256–B263, Dec. 2012.
- [10] C. Gunn, "CMOS photonics for high-speed interconnects," *IEEE Micro*, vol. 26, no. 2, pp. 58–66, Mar./Apr. 2006.
- [11] L. C. Kimerling, D. Ahn, A. B. Apsel, M. Beals, D. Carothers, Y. K. Chen, T. Conway, D. M. Gill, M. Grove, C.-Y. Hong, M. Lipson, J. Liu, J. Michel, D. Pan, S. S. Patel, A. T. Pomerene, M. Rasras, D. K. Sparacin, K.-Y. Tu, A. E. White, and C. W. Wong, "Electronic-photonic integrated circuits on the CMOS platform," in *Proc. SPIE, Silicon Photon.*, 2006, pp. 6–15.
- [12] T. Pinguet, B. Analui, E. Balmater, D. Guckenberger, M. Harrison, R. Koumans, D. Kucharski, Y. Liang, G. Masini, A. Mekis, S. Mirsaidi, A. Narasimha, M. Peterson, D. Rines, V. Sadagopan, S. Sahni, T. J. Sleboda, D. Song, Y. Wang, B. Welch, J. Witzens, J. Yao, S. Abdalla, S. Gloeckner, P. Dobbelaere, and G. Capellini, "Monolithically integrated high-speed CMOS photonic transceivers," in *Proc. 5th IEEE Int. Conf. Group IV Photon.*, 2008, pp. 362–364.
- [13] A. Mekis, S. Gloeckner, G. Masini, A. Narasimha, T. Pinguet, S. Sahni, and P. De Dobbelaere, "A grating-coupler-enabled CMOS photonics platform," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 3, pp. 597–608, May/Jun. 2011.

- [14] C. Batten, A. Joshi, J. Orcutt, A. Khilo, B. Moss, C. W. Holzwarth, M. A. Popović, H. Li, H. I. Smith, J. L. Hoyt, F. X. Kärtner, R. J. Ram, V. Stojanović, and K. Asanović, "Building many-core processor-to-dram networks with monolithic CMOS silicon photonics," *IEEE Micro*, vol. 29, no. 4, pp. 8–21, Jul./Aug. 2009.
- [15] J. F. Buckwalter, X. Zheng, G. Li, K. Raj, and A. V. Krishnamoorthy, "A monolithic 25-Gb/s transceiver with photonic ring modulators and Ge detectors in a 130-nm CMOS SOI process," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1309–1322, Jun. 2012.
- [16] A. Masood, W. Bogaerts, J. Van Olmen, J. Van Aelst, D. Van Thourhout, and D. Sabuncuoglu Tezcan, "Photonics-CMOS 3D integration: copper through-silicon-via approach," in *Proc. IEEE Annu. Symp. Photon. Benelux Chapter*, 2009, pp. 165–168.
- [17] J. Van Campenhout, M. Pantouvaki, P. Verheyen, H. Yu, P. De Heyn, G. Lepage, W. Bogaerts, and P. Absil, "Silicon-photonics devices for low-power, high-bandwidth optical I/O," in *Adv. Photon. Congr., OSA Tech. Dig.*, 2012, pp. 1–3.
- [18] M. Paniccia, A. Liu, N. Izhaky, and A. Barkai, "Integration challenge of silicon photonics with microelectronics," in *Proc. 2nd IEEE Int. Conf. Group IV Photon.*, 2005, pp. 20–22.
- [19] Y. Arakawa, T. Nakamura, Y. Urino, and T. Fujita, "Silicon photonics for next generation system integration platform," *IEEE Commun. Mag.*, vol. 51, no. 3, pp. 72–77, Mar. 2013.
- [20] C. Zhang and L. Li, "Characterization and design of through-silicon via arrays in three-dimensional ICs based on thermomechanical modeling," *IEEE Trans. Electron. Devices*, vol. 58, no. 2, pp. 279–287, Feb. 2011.
- [21] A. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos, N. Minas, S. Domae, D. Perry, M. Choi, A. Redolfi, C. Okoro, Y. Yang, J. Van Olmen, S. Thangaraju, D. S. Tezcan, P. Soussan, J. H. Cho, A. Yakovlev, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k/metal gate CMOS performance," in *Proc. IEDM*, 2010, pp. 2.2.1–2.2.4.
- [22] K. Lu, X. Zhang, S. Ryu, J. Im, R. Huang, and P. S. Ho, "Thermo-mechanical reliability of 3-D ICs containing through silicon vias," in *Proc. ETEC*, 2009, pp. 630–634.
- [23] S. Ryu, K. Lu, X. Zhang, J. Im, P. S. Ho, and R. Huang, "Impact of near-surface thermal stresses on interfacial reliability of through-silicon vias for 3-D interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 35–43, Mar. 2011.
- [24] T. C. Lu, J. Yang, Z. Suo, A. G. Evans, R. Hecht, and R. Mehrabian, "Matrix cracking in intermetallic composites caused by thermal expansion mismatch," *Acta Metall. Mater.*, vol. 39, no. 8, pp. 1883–1890, Aug. 1991.
- [25] M. Huang, "Stress effects on the performance of optical waveguides," *Int. J. Solids Struct.*, vol. 40, no. 7, pp. 1615–1632, Apr. 2003.
- [26] W. N. Ye, D. X. Xu, S. Janz, P. Cheben, M. J. Picard, B. Lamontagne, and N. G. Tarr, "Birefringence control using stress engineering in silicon-on-insulator (SOI) waveguides," *J. Lightw. Technol.*, vol. 23, no. 3, pp. 1308–1318, Mar. 2005.
- [27] D. J. Griffiths, *Introduction to Electrodynamics*, 4th ed. Reading, MA, USA: Addison-Wesley, 1999.
- [28] A. Delage, D. Xu, R. W. McKinnon, E. Post, P. Waldron, J. Lapointe, C. Storey, A. Densmore, S. Janz, B. Lamontagne, P. Cheben, and J. H. Schmid, "Wavelength-dependent model of a ring resonator sensor excited by a directional coupler," *J. Lightw. Technol.*, vol. 27, no. 9, pp. 1172–1180, May 2009.
- [29] X. Zheng, I. Shubin, G. Li, T. Pinguet, A. Mekis, J. Yao, H. Thacker, Y. Luo, J. Costa, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "A tunable  $1 \times 4$  silicon CMOS photonic wavelength multiplexer/demultiplexer for dense optical interconnects," *Opt. Exp.*, vol. 18, no. 5, pp. 5151–5160, Mar. 2010.
- [30] T. Hu, P. Yu, C. Qiu, H. Qiu, F. Wang, M. Yang, X. Jiang, H. Yu, and J. Yang, "Tunable Fano resonances based on two-beam interference in microring resonator," *Appl. Phys. Lett.*, vol. 102, no. 1, pp. 011112-1–011112-4, Jan. 2013.