IEEE Photonics Journal
An IEEE Photonics Society Publication

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Volume 5, Number 3, June 2013

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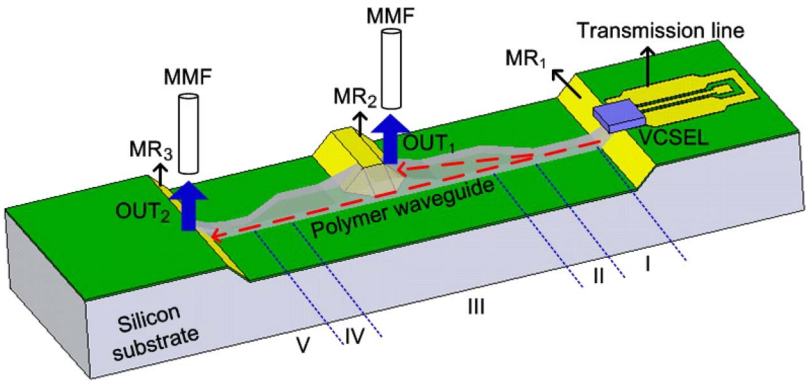

DOI: 10.1109/JPHOT.2013.2264662
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Polymer-Waveguide-Based Optical Circuit With Two Vertical-Transition Output Ports Realized on Silicon Substrate for Optical Interconnects

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DOI: 10.1109/JPHOT.2013.2264662

Manuscript received April 25, 2013; revised May 14, 2013; accepted May 16, 2013. Date of current version June 4, 2013. This work was supported by Hsinchu Science Park Administration of the Republic of China under Grant 101MG23-1. Corresponding author: M.-L. Wu (e-mail: mlwu@dop.ncu.edu.tw).

Abstract: A polymer-waveguide-based optical circuit with two vertical-transition output ports for the optical interconnects is demonstrated on a silicon substrate. Such a 1 × 2 vertical splitter is realized using a polymer waveguide monolithically integrated with three silicon 45° microreflectors. The vertical-cavity surface-emitting laser chip assembled at the input port and two multimode fibers located at two output ports are arranged to demonstrate a two-port optical proximity coupling of the off-chip optical interconnects based on the proposed splitter. The optical insertion loss of −6.6 dB is experimentally obtained for the proposed 1 × 2 vertical splitter with a splitting ratio of 1.3 : 1. The clearly 10-Gb/s optical eye patterns at both output ports verify that the 1 × 2 vertical splitter is suitable for the optical interconnects with multiple output ports.

Index Terms: Optical waveguides, micromirrors, silicon substrate, optical interconnection.

1. Introduction

Short-reach optical interconnects have an increasing demand due to the emerging applications in cloud computing, including the board-to-board interconnects [1], [2], the on-board interconnects [3]–[9], the chip-to-chip interconnects [10], [16], and the on-chip interconnects [11]–[15], [17], [18]. The optical waveguides combined with a vertical-transition structure developed on a silicon substrate [15]–[17] or a silicon-on-insulator (SOI) substrate [10]–[14], [18] to form a vertical-coupling configuration have received great attention in the recent years [10]–[18]. Several approaches were proposed to realize the vertical-transition structures, such as the grating coupler [10], the three-dimensional (3-D) taper [11], [12], the vertically integrated multimode interferometer (MMI) coupler [13], [14], the through-silicon photonic via (TSPV) combined the grating coupler [15], and the reflective mirrors [16]–[25]. Among those approaches, the grating coupler, the vertically integrated MMI coupler, and the TSPV combined with a grating coupler can couple optical power in the vertical direction within a very compact region. The 3-D taper as a prism coupler developed on the planar waveguide can also couple optical power in the vertical direction. However, the aforementioned couplers suffer a low tolerance of the spectral bandwidth and the structural size. Therefore, a

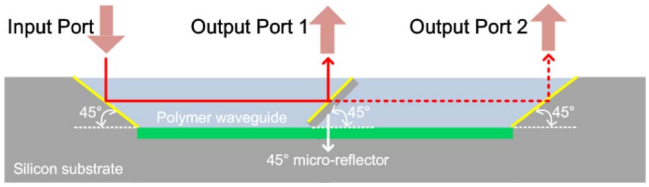


Fig. 1. Cross-sectional illustration of polymer-waveguide-based optical circuit with two vertical-transition output ports. The 1 × 2 vertical splitter is realized using a polymer waveguide combined with three 45° reflectors on a silicon substrate.

vertical-transition structure relatively insensitive to the optical wavelength would facilitate the development of the optical interconnects. The reflective mirrors as a vertical-transition structure developed on a silicon or SOI substrate would be a good choice for the optical interconnects, considering the reflective-mirror reflectivity with respect to the spectral bandwidth.

Considering that the silicon-based 54.7° reflective mirrors apply for the out-of-plane optical coupling, a high coupling loss between waveguide-to-waveguide in the vertical direction (using two 54.7° reflective mirrors) [16] or between vertical-cavity surface-emitting laser (VCSEL)-to-fiber (using one 54.7° reflective mirror) [19] was suffered due to laser beam walk-off at the receiving waveguide [16] or the flat-facet fiber [19]. The 45° reflective mirrors could provide an out-of-plane optical coupling with a reflective angle of minimum deviation [17], [18], [20]–[25]. Several approaches were proposed to realize the 45° reflectors, including a 45° slant end face of waveguide using a liquid-immersion tilt exposure [20], a reactive-ion-etching (RIE) process [21], and a silicon-based rear 45° mirror using an etchant tetramethylammonium hydroxide (TMAH) mixed surfactant NCW-1002 in an anisotropic wet-etching process [22]. However, an excess loss larger than 2 dB was suffered for the aforementioned mirrors due to an inaccuracy slant angle of 45° or a rough surface of a mirror. The high-quality silicon-based 45° reflector with a slant angle within 45 ± 1° and a root-mean-square (RMS) surface roughness value less than 30 nm was obtained using the anisotropic wet-etching process in a solution of potassium hydroxide (KOH) and isopropyl alcohol (IPA) [23], [24]. Such a silicon-based 45° reflector monolithically integrated with the silicon waveguide was experimentally demonstrated [25] and was further applied for an optical interconnect transmitter with a data rate of 5 Gb/s [18]. In order to well confine the laser beam in the silicon waveguide, the operating wavelength of 1310 nm was chosen in the demonstrations [18] to avoid material absorption. To extend the wavelength range of the laser sources for the optical interconnects based on the guided-wave optical paths, the silicon-based 45° reflector terminated polymer waveguides developed on silicon substrates were realized for on-chip out-of-plane optical interconnects using the wavelength of 850 nm [17]. In this paper, as shown in Fig. 1, an essential optical path with a 1 × 2 vertical splitter based on the polymer waveguide is developed on the silicon substrate. To verify the performance of the proposed 1 × 2 vertical splitter, a two-port optical proximity coupling of the off-chip optical interconnects based on the proposed splitter is experimentally demonstrated, as shown in Fig. 2.

2. Design of Two-Port Optical Proximity Coupling of Off-Chip Optical Interconnects Based on 1 × 2 Vertical Splitter

As shown in Fig. 1, the polymer waveguide combined with three silicon-based 45° reflectors is proposed to develop the proposed 1 × 2 vertical splitter on a silicon substrate. In this configuration, three silicon-based 45° reflectors are applied as the vertical-transition structures. In order to demonstrate a two-port optical proximity coupling of the off-chip optical interconnects based on the proposed splitter, as shown in Fig. 2(a), a VCSEL chip assembled at the input port and two multimode fibers (MMFs) located at two output ports are arranged. The proposed splitter can be separated into five regions, including two straight waveguides (regions I and V) with a width (W_1) of 40 μm, two taper regions with a taper angle of around 3° (regions II and IV), and a straight

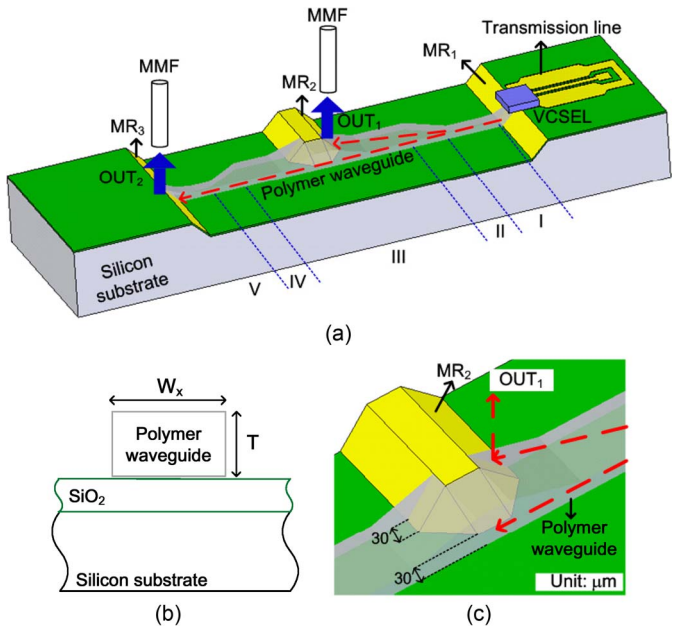


Fig. 2. Schematic illustrations of the polymer waveguide combined with 45° reflectors developed on a silicon substrate as vertical-transition structures is proposed to realize the 1 × 2 vertical splitter. (a) A VCSEL chip assembled at the input port and two MMFs located at two output ports are arranged to demonstrate a two-port optical proximity coupling of the off-chip optical interconnects. (b) The cross-sectional schema of polymer waveguide. (c) The MR_2 inserted into the region III of polymer waveguide to form a vertical-transition structure.

waveguide (region III) with a width (W_2) of 110 μm. The laser beam emitting from a VCSEL chip at the input port impinges upon the 45° microreflector 1 (MR_1), couples into the polymer waveguide (region I), and then propagates into the taper region (region II). The 45° microreflector 2 (MR_2) is designed in region III to vertically deflect partial optical power to output port 1 (OUT_1). Partial power propagates along the polymer waveguide (region III), penetrates into another taper region (region IV), and finally emits from output port 2 (OUT_2) via the 45° microreflector 3 (MR_3) in region V. As shown in Fig. 2(a), the total waveguide length is 6 mm and waveguide thickness (T) is 20 μm. The depth of the silicon 45° microreflector is 50 μm. The cross section of the polymer waveguide is schematically shown in Fig. 2(b). The EpoCore photoresist with a refractive index of 1.58 is adopted to develop the core layer of the polymer waveguide. A silicon dioxide (SiO_2) with a thickness of 1 μm is applied as a lower cladding layer. Its refractive index is 1.45. The air region surrounding the core layer served as the upper cladding layer of the polymer waveguide. As shown in Fig. 2(c), a vertical-transition structure based on the silicon 45° microreflector 2 (MR_2) is developed in region III to split optical power in the waveguide. The splitting ratio of the proposed vertical splitter is controlled using the insertion depth (ID) of the transition structure. In order to realize a splitting ratio of 1 : 1, the transition structure inserts into the polymer waveguide with an ID of 80 μm. In such a design, partial power propagating in the waveguide would impinge upon MR_2 with a width of 30 μm for output port 1 and a 50-μm-width etching structure is included within an ID of 80 μm. In addition, partial power would propagate along a free channel without a vertical-transition structure. The width of the free channel is also set as 30 μm for output port 2.

In order to evaluate the optical characteristics of the proposed 1 × 2 vertical splitter, the ray-tracing simulator of Advanced Systems Analysis Program (ASAP) is applied to analyze the transmission efficiencies at output ports and its splitting ratio. Its structural parameters are described below. The operating wavelength of 850 nm, the full diverging angle of 25°, and the emitting-area diameter of 15 μm for a VCSEL chip are fitted at the input port. The numerical aperture (NA) of 0.25 and the core diameter of 62.5 μm for the MMFs are fitted at the output ports, respectively. The

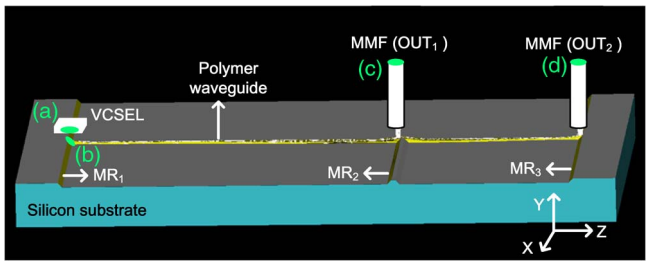


Fig. 3. Optical simulation of the proposed 1 × 2 vertical splitter is carried out based on the ray-tracing model. Simulated lightwave distribution within the proposed splitter is demonstrated. The interfaces (a)–(d) are denoted in the proposed splitter.

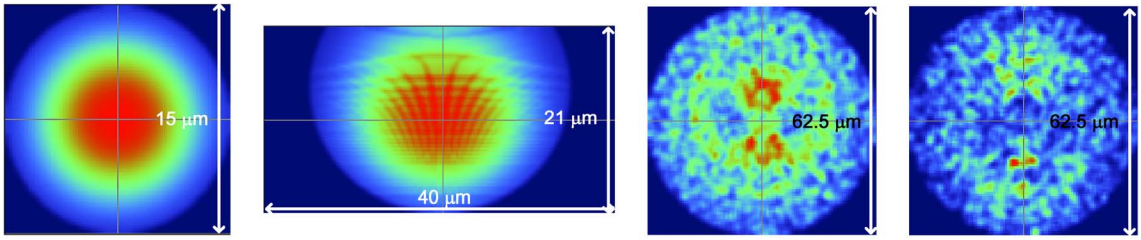


Fig. 4. Simulated intensity profiles distributed at different interfaces of (a) the VCSEL facet, (b) the MR_1 surface, (c) the MMF facet at OUT_1, and (d) the MMF facet at OUT_2.

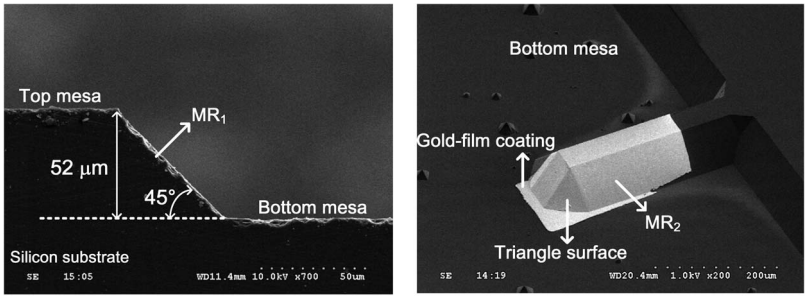
VCSEL-to-waveguide separation of 3 μm and the MMF-to-waveguide separation of 10 μm are set in the input and output ports, respectively.

As shown in Fig. 3, the simulated lightwave emitting from a VCSEL chip at the input port is coupled into the 1 × 2 vertical splitter. As shown in the figure, the lightwave is well confined within the polymer waveguide. At output ports OUT_1 and OUT_2, the lightwaves emitting from both output ports are received by two 62.5-μm-core MMFs, respectively. Fig. 4(a)–(d) shows the simulated intensity profiles of lightwave distributed on surfaces (a)–(d) of the proposed splitter. As shown in Fig. 4(a), the intensity field of VCSEL light source is assumed to be a Gaussian distribution with a diameter of 15 μm. Fig. 4(b) shows the intensity profile distributed on the surface of MR_1 within region I. The intensity-profile shift is observed owing to the refraction occurring at the air-to-polymer interface. The spot size of the laser beam on MR_1 is controlled within 21 μm due to a small divergent angle of the laser beam and a short separation between the VCSEL chip and MR_1. Hence, most of optical power could be coupled into the waveguide with a low excess power loss. Fig. 4(c) and (d) shows the intensity profiles distributed on the interfaces of MMFs located at output port 1 (OUT_1) and output port 2 (OUT_2), respectively. The non-Gaussian intensity profiles distributed on interfaces (c) and (d) of MMFs are observed. The simulated transmission efficiencies of -8.86 and -9.06 dB are obtained at output ports OUT_1 and OUT_2, respectively. Its corresponding splitting ratio is 1.05.

3. Realization and Characterization of Two-Port Optical Proximity Coupling of Off-Chip Optical Interconnects Based on 1 × 2 Vertical Splitter

3.1. Realization of Two-Port Optical Proximity Coupling of Off-Chip Optical Interconnects Based on 1 × 2 Vertical Splitter

In order to realize the vertical-transition structures in the proposed 1 × 2 vertical splitter, the silicon 45° reflectors are fabricated on the {110} planes of an oriented–defined (100) silicon



(a) (b)

Fig. 5. SEM pictures of (a) the side view of silicon 45° reflector and (b) the fabricated 45° reflector MR_2 with a gold-film coating.

substrate using the anisotropic wet-etching process in a solution of KOH and IPA. The RMS surface roughness of the 45° reflector can be controlled as low as 15 and 30 nm before and after the gold metal plating. The surface quality is better than the (1/10) λ requirement of an optical mirror. The detailed description of fabricating a silicon 45° reflector was revealed in the previous papers [23], [24]. The scanning-electron-microscopy (SEM) photos of fabricated silicon 45° reflectors MR_1 and MR_2 are illustrated in Fig. 5(a) and (b), respectively. According to the side view of MR_1 shown in Fig. 5(a), its etching depth of 52 μm is close to the designed value of 50 μm. The slant angle of 45° is well controlled, as shown in the figure. After fabricating the silicon optical bench (SiOB), SiO_2 as a lower cladding layer for the polymer waveguide and as an isolation layer for the transmission line is deposited on the SiOB by using plasma-enhanced chemical vapor deposition (PECVD). Finally, as shown in Fig. 5(b), the gold-film coating as a high-reflectivity layer is deposited on the 45° reflectors using electron-gun (E-gun) evaporation. The thickness of the gold-film coating is 300 nm.

The polymer waveguide with a thickness of 20 μm is fabricated on the bottom mesa of the silicon substrate by using the photolithography process. The fabricated polymer waveguides near MR_1 and MR_2 are demonstrated in Fig. 6(a) and (b), respectively. The end facet of the waveguide located within region I is shown in the inset in Fig. 6(a). The coplanar-waveguide transmission line with In/Ag solder bumps deposited on the top mesa of silicon substrate by an E-gun evaporator is shown in Fig. 6(c). The thickness of the coplanar-waveguide transmission line is 1 μm. The high-frequency performance of the proposed transmission line was discussed in the previous papers [18]. The thickness and the composition of In/Ag solder bumps are 3 μm and 97/3 wt.%, respectively. A commercial 10-Gb/s VCSEL chip is assembled on the proposed silicon substrate using the flip-chip bonding, as shown in Fig. 6(d).

3.2. Optical Characterization of Two-Port Optical Proximity Coupling of Off-Chip Optical Interconnects Based on 1 × 2 Vertical Splitter

The optical characteristics of the two-port optical proximity coupling of the off-chip optical interconnects based on the 1 × 2 vertical splitter are measured after the VCSEL chip being assembled onto the silicon substrate, including the transmission efficiencies at output ports and its splitting ratio. The propagation loss of −0.35 dB/cm for the straight waveguide with a core size of 40 × 20 μm^2 was revealed in the previous lecture [17]. At output ports, two MMFs with a core diameter of 62.5 μm are adopted to receive the laser beams. As shown in Fig. 7, the VCSEL chip is biased at 6 mA using direct-current (dc) probes. In this figure, two light spots at output ports are denoted using red-dot circulars. The corresponding transmission efficiencies are obtained at output port 1 (OUT_1) and output port 2 (OUT_2) as −9.06 and −10.22 dB, respectively. The splitting ratio of the proposed splitter is about 1.3. The total insertion loss of the proposed splitter is −6.6 dB. As compared with the simulated transmission efficiency at output port 2 (OUT_2), the efficiency variation of −1.16 dB for the fabricated structure is attributed to the light scattering on a non-45° triangle

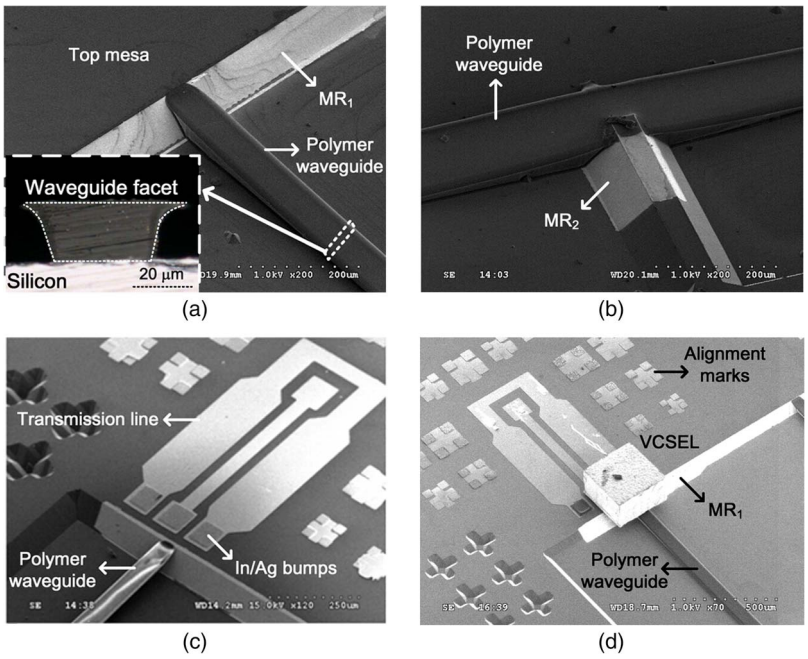


Fig. 6. SEM pictures of (a) the fabricated polymer waveguide combined with the MR_1 within the region I (Inset shows the polymer-waveguide facet.), (b) the fabricated polymer waveguide combined with the MR_2 within the region III, (c) the fabricated transmission line and In/Ag bumps deposited on the top mesa of silicon substrate, and (d) a VCSEL chip flip-chip assembled on the proposed 1 × 2 vertical splitter.

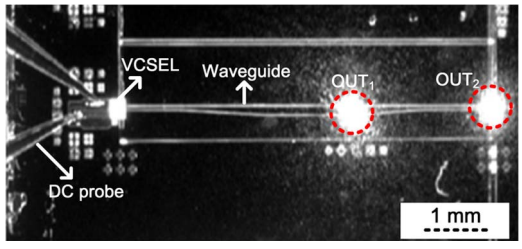


Fig. 7. Photo of laser beams emitting from the output ports OUT_1 and OUT_2 of two-port optical proximity coupling of the off-chip optical interconnects.

surface shown in Fig. 5(b). Such a non-45° triangle surface is produced during the wet-etching process of MR_2. Since the material absorption of polymer waveguide has not been considered in the simulation, a slight difference of −0.2 dB for the simulated and measured transmission efficiencies at output port 1 (OUT_1) is observed.

3.3. High-Speed Characterization of Two-Port Optical Proximity Coupling of Off-Chip Optical Interconnects Based on 1 × 2 Vertical Splitter

To evaluate the high-speed performance of two-port optical proximity coupling of the off-chip optical interconnects based on the 1 × 2 vertical splitter, the optical-eye-pattern measurement with a data rate of 10.3125 Gb/s is carried out for both output ports under a pseudorandom-binary-sequence (PRBS) pattern with a length of $2^{15} - 1$. Its experimental setup is schematically illustrated in Fig. 8. The high-speed non-return-to-zero (NRZ) signals with an output voltage of 0.8 V (peak to peak) generated by a pulse pattern generator (PPG) are fed into the VCSEL chip of the proposed splitter using a GSG coplanar probe. The photodetector with a bandwidth of 9 GHz is employed to

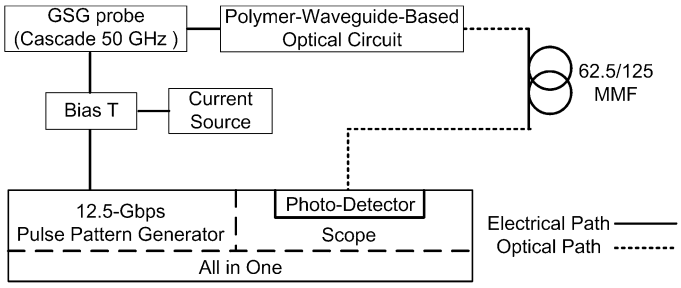


Fig. 8. Experimental setup for measuring the optical eye diagrams of two-port optical proximity coupling of the off-chip optical interconnects.

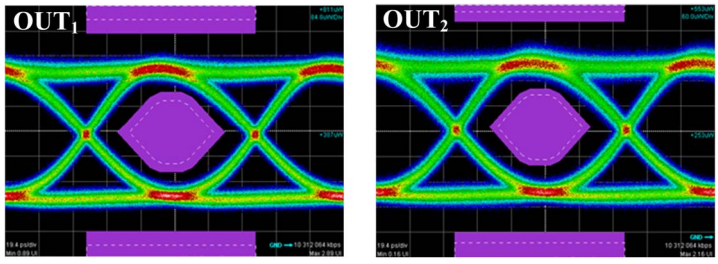


Fig. 9. Optical eye patterns of two-port optical proximity coupling of the off-chip optical interconnects operated at the data rate of 10.312 Gb/s for (a) the output port 1 (OUT_1) and (b) the output port 2 (OUT_2).

characterize the high-speed performance of two-port optical proximity coupling of the off-chip optical interconnects. The optical power of 3 mW emits from the VCSEL chip under a bias current of 10 mA. As shown in Fig. 9(a) and (b), the clearly optical eye patterns with a superposition of 300 waveforms are obtained for both output ports. A 10-Gb/s Ethernet eye mask is adopted to check the eye-pattern performance. There is no mask-hit detected for the optical eye patterns with a margin of over 15% at the room temperature.

4. Conclusion

In this paper, a polymer waveguide combined with three silicon 45° microreflectors has been realized on a silicon substrate to demonstrate a 1 × 2 vertically optical splitter. The high-frequency transmission line combined with the In/Ag solder bumps has been developed to assemble a VCSEL chip onto the silicon substrate. The optical insertion loss of −6.6 dB has been experimentally obtained for the two-port optical proximity coupling of the off-chip optical interconnects based on the 1 × 2 vertical splitter with a splitting ratio of 1.3 : 1. The clearly 10-Gb/s eye patterns at both output ports of the proposed splitter have been demonstrated and verify that the 1 × 2 vertical splitter is suitable for the optical interconnects with multiple output ports.

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