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Microring-Based *N* × *N* Scalable Polymeric Electrooptic Routing Switch Array: Theory, Architecture, and Design Scheme

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Abstract: Device architecture and design scheme of an $N \times N$ scalable electrooptic (EO) routing switch array (RSA) are proposed using electric-field-induced EO polymeric microrings. The basic 2×2 /cross/bar EO switching element is optimized under 1550-nm wavelength, and the ring radius is only 13.76 μ m with < 10⁻⁴ dB/cm bending loss. The basic element reveals a free spectral range (FSR) of 17 nm, a switching voltage of 5 V, and response times of 70/140 ps, and the crosstalk under cross and bar states are about -28.8 and -39.9 dB, respectively. Using 2 \times 2 switching elements, 4 \times 4, 8 \times 8, 16 \times 16, and 32 \times 32 RSAs are presented, under all routing paths, their maximum insertion losses are 2.57, 5.19, 5.99 and 7.59 dB, respectively, and their maximum crosstalk are -28.7, -28.7, -26.27 and -25.07 dB, respectively. Universal structure, routing scheme, electrical/optical responses, and dynamic power consumption (PC) of $N \times N$ RSA are then demonstrated, and dependence relations between routing performances and the RSA size N are achieved through data fitting. Comparisons with other reported passive/active routers/switches confirm that, due to superiority on fewer rings, picosecond faster response speed, zero static PC, and lower insertion loss and crosstalk, this polymer-based routing scheme can be a good candidate in on-chip optical systems.

Index Terms: Routing switch array (RSA), electrooptic (EO) polymer, insertion loss, crosstalk, switching voltage.

1. Introduction

Because of recent advances in nanoscale photonics and photonic devices, such as waveguides [1], [2], modulators [3]–[5], lasers [6]–[8], and photodetectors [9], [10], photonic network-on-chip (NoC), instead of electronic NoC, becomes a promising solution to meet the ever increasing chip-level interconnect challenges. The core part of a photonic NoC is an on-chip photonic interconnection network, which is composed of passive waveguides and optical routers [11], and it should reveal better performances to meet the needs of on-chip photonic interconnection designs in terms of bandwidth, power consumption (PC), footprint, and scalability. Compared with other materials such as silica, lithium niobate, and III–V compound semiconductors, polymers offer many unique properties,

e.g., ease of fabrication, low production cost, and compatibility with Si and GaAs fabrication technologies, and they can also be deposited directly on any kind of flat or curve substrates. Besides, accurate control of refractive indices and properties can be obtained for the tailored polymer materials by different combinations of monomers, and the low-temperature fabrication process of polymer waveguides gives the designer a large degree of freedom. All these are an important factor in the practical implementation of complex high-density interconnect and circuits. Therefore, as silicon and other III–V compound semiconductors, polymers also become candidates in the design and fabrication of both passive and active routing devices [12]–[16].

Generally, an optical routing switch is built upon waveguides and optical switches, and it can optically route data packets between a set of input and output ports toward any directions. There are two considerations during the design of an optical routing element. On one hand, basic 2×2 switching element and reasonable architecture are the first step for constructing large optical routing switch array (RSA). Previously, by using directional coupler (DC), Y-fed coupler, Mach-Zehnder interferometer (MZI), multimode interference (MMI), etc., different 1×1 and 2×2 polymer electrooptic (EO) switches have been reported by our group [12]–[16]. However, they are found to be unsuitable to form large-scale switching arrays, because of long waveguide and electrode. Within the available optical switches, microring resonator (MRR)-based optical switches are typically preferred due to their ultracompact size, simple-mode resonances, and ease of phase-matching between an MRR and its coupling waveguides. Besides, the MRR structure is more convenient for building large switching arrays by cascading fundamental element. Until now, the reported MRR EO switches either in experiment or in theory are generally the carrier-injection-based silicon or GaAs ones, e.g., the singlering-based silicon MRR switch [17], the double-ring-based silicon MRR switches [18]-[21] and GaAs MRR switch [22], the ten-ring coupled silicon MRR switch [23], and the interferometric silicon MRR switch [24]. However, because of effective carrier lifetime, the response time of carrier-dispersionbased switches is roughly at the level of 1 ns, and also, in the above reports [17]-[24], the scalability of the basic element to large array is not discussed. In view of these two issues, in this paper, we adopt poled polymer and fast EO effect instead of silicon and carrier-injection dispersion effect for designing MRR EO switch, leading to an even fast response time at the level of picosecond. One novel point in this paper is that the bending radius of the polymer microring is as small as 13.76 μ m, which is similar to that of a silicon MRR, owning to the low-index left/right air claddings besides polymer core. What's more, this paper intensively discusses the scalability of the proposed 2×2 MRR switch element for constructing high radix routing array used in photonic NoC, which is also a difference from other reports.

On the other hand, existing photonic NoC designs include switching networks using TO or EO effect tuning switches and passive networks using switches with a fixed-wavelength assignment. Since passive networks can route data with fixed wavelength and do not require extra control circuits, they tend to have better power performance. However, most of the existing passive networks suffer from poor scalability and high design complexity, such as the reported four- and five-port optical routers based on MRRs [25]-[29]. Still, only four- and five-port optical routing switches are far from enough to construct all photonic NoCs. Though Min et al. proposed a universal method for constructing N-port nonblocking passive routing element [30], active switching networks remain the preferred choice of design for large-scale optical NoC systems [31], [32], due to their reconfigurable data links other than definite-path routing operation. Instead of passive and TO-tuned switching networks, in this paper, a scalable EO RSA with N input ports and N output ports (N = 4, 8...) is proposed for switching 1550-nm (free spectral range (FSR) = 17 nm) data stream between any two different nodes by applying different manners of voltage, and it can offer more compact structure in size, shorter response time, and zero static PC, due to the adoption of polymer materials, linear EO effect, and efficient routing architecture, as when compared with the ever reported passive routing element [30] or slow-speed TO-tuned routing element [25]-[29]. In addition, to the best of our knowledge, this is the first time to demonstrate a scalable EO polymer RSA with the proposed basic switching element in such a careful and thorough manner.

The structure of this paper is organized as follows. First in Section 2, basic 2×2 routing element is presented using two active MRRs and two passive waveguides, and detailed optimization and



Fig. 1. (a) Structure of the 2×2 cross/bar EO routing switch. (b) Cross-section view AA' over the coupling region between MRR waveguide and channel waveguide. (c) The equivalent driving model of the MRR EO switch.

analysis are conducted. In Section 3, by using four 2×2 routing switches, a 4×4 RSA is proposed, and formulation and characterization are derived. Furthermore, in Section 4, an 8×8 RSA is described, and its performances of routing operation from two typical input ports to other output ports are numerically simulated. In Section 5, the generic structure and routing scheme of the $N \times N$ RSA are raised. The relations between the performances of an RSA and its size are evaluated, and some comparisons are made between this design scheme and some state-of-art reported ones. Finally, some conclusions are reached in Section 6.

2. Basic 2 \times 2 Cross/Bar Routing Switch

2.1. Material System

For enabling device development and good performances, the material system should meet the following requirements: First, all the used materials should satisfy refractive index condition to form a waveguide. Second, the core material should have large EO coefficient so that a small operation voltage can be achieved for enhancing wavelength-tuning efficiency of microring, and also, high thermal stability with small polar-order relaxation is desired. Third, the refractive index difference between the EO core and the left/right cladding layer should be large for well confining the optical field in bending waveguide and obtaining small ring radius as well as small device size. Fourth, the core, upper/under confined layers, and left/right cladding layers should be transparent for reducing optical power loss. In order to satisfy the above characteristics, during design, the guest-host polymer AJL8/ APC, exhibiting good thermal stability, improved poling behaviors, and high optical transparency around 1550 nm, is selected as EO core material, whose refractive index, amplitude loss coefficient, and EO coefficient (at 1550 nm) are $n_{10} = 1.59$, $\alpha_{10} = 0.25$ dB/cm, and $\gamma_{33} = 68$ pm/V, respectively [33], [34]. Low-loss photosensitive fluorinated copolymer P(PFS-GMA) is adopted as upper/under confined layer material, whose refractive index and amplitude loss coefficient (at 1550 nm) are $n_{20} = 1.461$ and $\alpha_{20} = 0.25$ dB/cm, respectively [35]. The electrode material is gold, and its refractive index and bulk extinction coefficient (at 1550 nm) are $n_{30} = 0.19$ and $\kappa_{30} = 6.1$, respectively [36]. Air is chosen as left/right cladding material with a refractive index and amplitude loss coefficient of $n_{40} = 1$ and $\alpha_{40} = 0$, respectively, which allows small bending radius and small device size due to its large index contrast with the EO core. Note that the adopted optical constants in the following may be different from those obtained from different processing conditions or technologies.

2.2. Structure and Principle

Fig. 1 depicts (a) the structure of the 2 \times 2 cross/bar polymer EO routing switch, and (b) crosssectional view AA' over the coupling region between the MRR waveguide and the channel waveguide. The device consists of a horizon rectangular waveguide, a vertical rectangular waveguide, and two microrings (R₁ and R₂) with the same radius. The distance between the two input ports and the coupling planes S_1 and S_4 , and that between the two output ports and the coupling planes S_2 and S_3 are both L_1 (1000 μ m); the distance between S_1 and S_3 and that between S_2 and S_4 are both L_3 . As shown in Fig. 1(b), the electrode is only deposited upon the MRR waveguide, and the channel waveguide is passive without electrode. Due to bending effect, the mode propagation constant is different from that of the straight waveguide with the same size [37]. Therefore, under the case of without applying voltage, for obtaining the same mode propagation constants, the two core widths of the MRR waveguide and channel waveguide are slightly different, defined as w_r and w_c , respectively. Also, the under-cladding thickness of the channel waveguide is slightly larger than that of the MRR waveguide, and their relation is $t_{2c} = t_2 + t_3$, where t_2 and t_3 are the under-cladding thickness and electrode thickness of the MRR waveguide. When t_2 is sufficiently large, a small increase of the under-cladding thickness will cause no influence to mode constants.

Let the light with resonance wavelength input into the horizon waveguide only. (1) When the applied voltage U_e on R₁ and R₂ is zero, the output power from the vertical channel becomes the maximum through the coupling between channel waveguide and MRR waveguide. This state is named cross state. (2) As U_e increases, the core refractive index of the MRR waveguide is changed, and the mode propagation constant reveals mismatch with that of the channel waveguide; therefore, the output powers from the horizon and vertical channel are changed. With a suitable voltage (named switching voltage), the output power from the vertical channel becomes the minimum, whereas that from the horizon channel becomes the maximum. This state is named bar state. The case of light inputting into the vertical waveguide can be similarly treated.

2.3. Modeling and Formulation

The refractive index change of the MRR EO core material resulting from the applied voltage $U_{\rm e}$ is

$$\Delta n_{10} = \frac{1}{2} n_{10}^3 r_{33} E_1 = \frac{n_{10}^3 n_{20}^2 r_{33} U_e}{2(2n_{10}^2 t_2 + n_{20}^2 t_1)}.$$
 (1)

Then, the refractive index of the EO core material will be changed from n_{10} to $n_{10} + \Delta n_{10}$, leading to a propagation constant variation from β_0 to $\beta_U = \beta_0 + \Delta\beta$, and the indices of other materials will not be changed, since they are non-EO materials. β_0 and β_U can be achieved from the theoretical approach proposed by Marcatili [38].

Take the case of light inputting into the horizon channel for analysis. As shown in Fig. 1(a), over the coupling plane S_1 , define a_{11} and b_{11} as the input and output light amplitudes of the horizon waveguide, and a_{21} and b_{21} as the input and output light amplitudes of the MRR waveguide. Over other three coupling planes S_2 , S_3 and S_4 , a_{21} , b_{21} , a_{31} , b_{31} , a_{41} , b_{41} , a_{12} , b_{12} , a_{22} , b_{22} , a_{32} , b_{32} , a_{42} , and b_{42} are also defined and labeled in the figure. The relation among the four amplitudes over each plane can be described by the following transfer matrixes [39], [40]:

$$\begin{bmatrix} a_{2i} \\ b_{2i} \end{bmatrix} = \frac{1}{j\kappa_{CR}} \begin{bmatrix} t_{CR} & -1 \\ 1 & -t_{CR} \end{bmatrix} \begin{bmatrix} a_{1i} \\ b_{1i} \end{bmatrix}, \begin{bmatrix} a_{4i} \\ b_{4i} \end{bmatrix} = \frac{1}{j\kappa_{CR}} \begin{bmatrix} t_{CR} & -1 \\ 1 & -t_{CR} \end{bmatrix} \begin{bmatrix} a_{3i} \\ b_{3i} \end{bmatrix}, i = 1, 2$$
(2)

and t_{CR} and κ_{CR} are transmittance coefficient and coupling coefficient between the bending MRR waveguide and straight channel waveguide, respectively, which can be calculated by using the coupled-mode theory (CMT) on DC with weighted coupling [41]. Besides, outside the coupling planes, optical propagation in resonators can be expressed as

$$\begin{bmatrix} a_{21} \\ b_{21} \end{bmatrix} = \begin{bmatrix} 0 & \exp(-j\phi_1) \\ \exp(j\phi_2) & 0 \end{bmatrix} \begin{bmatrix} a_{31} \\ b_{31} \end{bmatrix}, \begin{bmatrix} a_{22} \\ b_{22} \end{bmatrix} = \begin{bmatrix} 0 & \exp(-j\phi_2) \\ \exp(j\phi_1) & 0 \end{bmatrix} \begin{bmatrix} a_{32} \\ b_{32} \end{bmatrix}$$
(3)

$$a_{41} = b_{42} \exp(-j\psi_2), a_{12} = b_{11} \exp(-j\psi_2), a_{42} = 0$$
(4)

where $\phi_1 = 1.5\pi R(\beta_R - j\alpha_R)$, $\phi_2 = 0.5\pi R(\beta_R - j\alpha_R)$ and $\psi_2 = L_3(\beta_C - j\alpha_C)$ are not purely real or imaginary; $\beta_C = \beta_0$ is the mode propagation constant of the channel waveguide, $\beta_R = \beta_0$ is that of the MRR waveguide under $U_e = 0$, and $\beta_R = \beta_U = \beta_0 + \Delta\beta$ is that of the MRR waveguide under



Fig. 2. (a) Curves of mode effective indices of MRR waveguide (MRR) and channel waveguide (Channel) versus waveguide core width. (b) Curves of fundamental mode effective index n_{CR} and bending radius *R* versus resonance order *m*. (c) Effects of bending radius *R* on mode effective index n_{CR} and power loss coefficient α_{b} .

 $U \neq 0$; and $\alpha_{\rm C}$ and $\alpha_{\rm R}$ are mode amplitude loss coefficients of the channel waveguide and MRR waveguide, respectively. Combining (2)–(4), we can derive the transfer functions as

$$U = b_{12}/a_{11} = (t_{CR}^2/f_2) \{ f_1 - k_{CR}^2 \exp[-j(\phi_1 + \phi_2)] \}$$

$$\times \exp(-j\psi_2) \{ 1 - \exp[-j(\phi_1 + \phi_2)] \}$$

$$V = b_{41}/a_{11} = -(1/f_1f_2)$$

$$\times \left(k_{CR}^2 f_2 \exp(-j\phi_2) + t_{CR}^2 k_{CR}^2 \exp[-j(\phi_1 + 2\psi_2)] \{ f_1 - k_{CR}^2 \exp[-j(\phi_1 + \phi_2)] \}^2 \right)$$
(6)

where $f_1 = 1 - t_{CR}^2 \exp[-j(\phi_1 + \phi_2)]$, and $f_2 = f_1^2 - k_{CR}^4 \exp[-j(2\phi_1 + 2\psi_2)] \{f_1 + t_{CR}^2 \exp[-j(\phi_1 + \phi_2)]\}$.

Define the input light amplitude into the horizon channel as a'_{11} , the output light amplitudes from the horizon channel and vertical channel as b'_{12} and b'_{41} , respectively, and they can be written as

$$a'_{11} = a_{11} \exp(j\psi_1), b'_{12} = b_{12} \exp(-j\psi_1), b'_{41} = b_{41} \exp(-j\psi_1)$$
(7)

where $\psi_1 = L_1(\beta_C - j\alpha_C)$ is also a complex number. Finally, the power transfer functions can be expressed as

$$|B|^{2} = |b_{12}'/a_{11}'|^{2} = |(b_{12}/a_{11})\exp[-j(2\psi_{1})]|^{2} = |U\exp[-j(2\psi_{1})]|^{2}$$
(8)

$$|D|^{2} = |b_{41}'/a_{11}'|^{2} = |(b_{41}/a_{11})[-j(2\psi_{1})]|^{2} = |V\exp[-j(2\psi_{1})]|^{2}$$
(9)

and the output powers in decibel form are

$$P_{o1} = 10 lg(|B|^2), P_{o2} = 10 lg(|D|^2).$$
 (10)

2.4. Waveguide Core Size Optimization

For increasing EO overlap integral, the selected mode is E_{00}^{ν} , whose main field components are E_{γ} and H_x . For MRR waveguide, assuming that the upper/ under-cladding thickness is half-infinite, without considering the influence of bending on mode constants, Fig. 2(a) shows the relation of effective refractive index of E_{00}^{ν} , E_{01}^{ν} , and E_{10}^{ν} modes versus MRR waveguide core width w_r , where the core thickness and width are equal, that is, $w_r = t_1$. It can be found that the single mode condition is $1.2 < w_r = t_1 < 2.1 \ \mu$ m, and during design, we select $w_r = t_1 = 1.7 \ \mu$ m. The influence of bending on E_{00}^{ν} mode refractive index is further considered [37], as shown in Fig. 2(a), where the bending radius is $R = 13.76 \ \mu$ m. As can be seen, because of bending, the mode index is increased, and under $w_r = t_1 = 1.7 \ \mu$ m, the mode effective index is $n_{CR} = 1.5243$.

For the channel waveguide, the core thickness is equal to that of the MRR waveguide, which is 1.7 μ m. When the applied voltage is zero, the mode effective indices of the two waveguides should be identical. Fig. 2(a) also presents the curve of effective index of E_{00}^{ν} mode versus the channel waveguide core width w_c . For enabling the two effective indices to be identical, we choose $w_c = 2.03 \ \mu$ m.



Fig. 3. Effects of (a) the upper/under confined layer thickness t_2 and (b) electrode thickness t_3 on the mode effective refractive index n_{CR} and mode loss coefficient α_{R} . (c) Effect of coupling gap *d* between the channel waveguide and MRR waveguide on coupling coefficient κ_{CR} .

2.5. Bending Radius Optimization

The bending radius should satisfy the resonance equation

$$2\pi Rn_{\rm CR} = m\lambda \tag{11}$$

where *m* is resonance order, and n_{CR} is mode effective index that is also dependent on bending radius. Fig. 2(b) shows the curves of fundamental mode effective index n_{CR} and bending radius *R* versus resonance order *m*, where $w_r = t_1 = 1.7 \mu m$, and the upper/under confined layers are assumed to be half-infinite. As *m* increases, n_{CR} decreases and *R* increases. Properly, we select m = 85, and the bending radius is determined to be $R = 13.76 \mu m$.

On another aspect, the bending will cause extra bending loss. Fig. 2(c) exhibits the effects of bending radius *R* on mode effective index n_{CR} and bending power loss coefficient α_b . It can be observed that α_b decreases exponentially as the increase of *R*. When $R = 13.76 \ \mu m$, α_b is dropped below 10^{-4} dB/cm, which can be neglected compared with propagation loss α_R .

2.6. Cladding and Electrode Thickness Optimization

Concerning the discussion on Fig. 2, the upper/under confined layers are assumed to be infinitely thick. However, in practical design, both the cladding and the electrode cannot be taken so thick, and its minimum thickness should be decided. Fig. 3(a) and (b) show the effects of the upper/under confined layer thickness t_2 and electrode thickness t_3 on the mode effective refractive index n_{CR} and mode loss coefficient α_R . We can find from Fig. 3(a) that, when t_3 is taken as sufficiently large, e.g., $t_3 = 100 \ \mu m$, n_{CR} becomes constant when $t_2 \ge 2.5 \ \mu m$, and the mode propagation will form a steady state. On the other hand, in order to increase the electric field in the MRR core, the upper/under/under-cladding should be as thin as possible, and consequently, $t_2 = 2.5 \ \mu m$.

Since the electrode thickness cannot be made as large as 100 μ m, its minimum value should also be determined. We can see from Fig. 3(b) that, when t_3 increases sufficiently large, n_{CR} becomes constant too, the mode propagation will also form a steady state. When $t_3 \ge 0.2 \mu$ m, the electrodes can be regarded as half-infinite, which is in accordance with the assumption of $t_3 = 100 \mu$ m in Fig. 3(a). Considering all the influences of t_2 and t_3 on n_{CR} and α_R , we have $t_2 = 2.5 \mu$ m and $t_3 = 0.2 \mu$ m. In this case, the mode amplitude loss coefficient of the channel waveguide is about $\alpha_C = 0.256 \text{ dB/cm}$, and that of the MRR waveguide is about $\alpha_R = 0.298 \text{ dB/cm}$.

2.7. Coupling Gap Optimization

The coupling coefficient between the MRR waveguide and channel waveguide is a key parameter of the device, which should be carefully selected during the design stage of the device. Fig. 3(c) shows the effect of coupling gap *d* between the channel waveguide and MRR waveguide on the coupling coefficient κ_{CR} , where $w_r = t_1 = 1.7 \ \mu$ m, and $w_c = 2.03 \ \mu$ m. This gap cannot be taken too small; otherwise, the fabrication accuracy may be a problem; whereas it cannot be taken too large, otherwise, the coupling effect becomes too weak. Therefore, we choose $d = 0.14 \ \mu$ m, and the corresponding coupling coefficient is $\kappa_{CR} = 0.08664$ and transmittance coefficient is $t_{CR} = \sqrt{1 - \kappa_{CR}^2} = 0.99624$.



Fig. 4. (a) Curves of output powers versus the applied voltage on the two microrings. (b) Curves of output powers versus light wavelength. (c) FSR of the MRR EO switch.

2.8. Switching Characteristics

Let the light input into the horizon waveguide only, that is, $P_{11} \neq 0$ and $P_{12} \neq 0$. Using (8)–(10), under the resonance wavelength of 1550 nm, Fig. 4(a) shows the curves of output powers P_{o1} and P_{o2} versus the applied voltage on the two microrings R_1 and R_2 . It can be found that, when $U_e = 0$ V, the device is operated at cross state. The insertion loss under this state is about 2.42 dB, and the crosstalk between the two ports is -28.8 dB. As the increase of U_e , the mode mismatch between the channel waveguide and MRR waveguide is enhanced, the output power from the cross port drops, and the output powers from the through port increases. When the applied voltage is $V_s = 5.0$ V, the crosstalk between the two ports is below -39.9 dB, and the insertion loss of the through port is about 0.13 dB.

2.9. Spectral Characteristics

Under the applied voltages of 0, 5 and 10 V, Fig. 4(b) presents the curves of output powers of the cross port and through port versus light wavelength. It can be found that, under $U_e = 0$ V and $\lambda = 1550$ nm, the input power into the horizon waveguide will fully output from the cross port through the coupling with microrings, the device reveals cross state, and the crosstalk is less than -28.8 dB. Under $U_e = 5$ V, the output power of the cross port drops from point a to d, and that of the through port increases from point b to c. This state is named bar state, and the crosstalk is less than -39.9 dB. As $U_e = 10$ V, the crosstalk is lower than that under $U_e = 5$ V, which is below -50 dB. An EO tuning efficiency on wavelength is found to be 16 pm/V, showing an efficient value as when compared with the LiNbO₃ MRR switch (10 pm/V) [42]. As exhibited in Fig. 4(c), the free spectral range (FSR) is about 17 nm (~2100 GHz). Therefore, the switch can also function at some other wavelengths, such as 1534 nm and 1567 nm. For simplicity, in this paper, we only discuss the switching property at 1550 nm.

2.10. Response Time and the Maximum Switching Frequency

Define $\varepsilon_{\rm m} = C/(C')$ as the microwave equivalent relative dielectric constant, where $C = \oint \varepsilon_0 \varepsilon E \cdot dS$ is the capacitance of the electrode shown in Fig. 1(b), E and ε are the electric field and dielectric constant over the integral surface, ε_0 is the dielectric constant in vacuum, and C' is the capacitance of the same electrode when it is embedded in vacuum. With the optimized parameters, the calculated capacitance of each microring is only $C_{\rm R1} = C_{\rm R2} = C_{\rm R} = 4.32 \times 10^{-4} \, \text{pF}$ due to the small electrode area, and the microwave dielectric constant is about $\varepsilon_{\rm m} = 2.2223$. The cross/bar switch is driven in lumped manner, and its equivalent circuit is shown in Fig. 1(c). Assume that the applied voltage is $V_{\rm g}(t)$, whose Fourier transformation is $V_{\rm g}(\omega)$ with ω identifying angular microwave frequency, and then, the time variation signal applied on electrode is

$$u_{\rm e}(t) = F^{-1} \left[V_{\rm g}(\omega) H(\omega) \right] \tag{12}$$

where F^{-1} is the inverse Fourier transformation, $H(\omega)$ is the transfer function of the lumped circuit, expressed as

$$H(\omega) = (1 + j\omega R_g C_{eq})^{-1}$$
(13)



Fig. 5. Dynamic responses under the switching operation of (a) 1 MHz, (b) 10 GHz, and (c) 1 GHz. (d) Curve of crosstalk versus switching frequency. (e) Curves of energy needed per bit and the average PC versus switching frequency.

 C_{eq} is an equivalent capacitance including C_{R1} , C_{R2} and the parasitic capacitance (denoted by C_{pad}), and R_g is the internal resistance of the driving source. Under the dynamic operation of $u_e(t)$, the phases ϕ_1 and ϕ_2 should be modified to

$$\phi_{1}(t) = \int_{t-1.5\pi R/v_{0}}^{t} [\beta_{\mathsf{R}}(\tau) - \mathbf{j}\alpha_{\mathsf{R}}(\tau)] \mathbf{v}_{0} \mathsf{d}\tau, \\ \phi_{2}(t) = \int_{t-0.5\pi R/v_{0}}^{t} [\beta_{\mathsf{R}}(\tau) - \mathbf{j}\alpha_{\mathsf{R}}(\tau)] \mathbf{v}_{0} \mathsf{d}\tau$$
(14)

where $\beta_{\rm R}(t)$ and $\alpha_{\rm R}(t)$ are both time-dependent variables, and v_0 is the mode phase velocity in microring. Then the dynamic output powers $P_{\rm o1}$ and $P_{\rm o2}$ can both be treated as the functions of t, that is

$$P_{oi}(t) = P_{o1}[\phi_1(t), \phi_2(t), \kappa_{CR}(t), t_{CR}(t)], i = 1, 2.$$
(15)

The dynamic responses of the switch under the operation of two square-wave signals (5-V_{pp}, 2.5-V_{bias}, 1 MHz, and 10 GHz) are shown in Fig. 5(a) and (b), respectively. One can find that, due to the low-pass filtering function of the lumped circuit, the applied signal on the electrode under 10 GHz is distorted to a nonstep style compared with that under 1 MHz, leading to nonstep power exchange between the two ports. As the switching frequency increases to 100 GHz (not shown), the output power's amplitudes and switching signal's amplitude are decreased, and the normal switching function cannot be realized. In other words, the crosstalk under both two states increases as the switching frequency (defined as f_m) increases, which is proven by Fig. 5(d). For obtaining a maximum crosstalk of -10 dB, the allowed maximum switching frequency is about $f_{max} = 25$ GHz. From Fig. 5(c), the 10%–90% rise time and fall time under $f_m = 1$ GHz are roughly $t_r = 80$ ps and $t_f = 140$ ps, respectively. These two values are obviously smaller than those of the carrier-injection-based silicon switches with up to 1- to 10-ns response time [17]–[21], [23], [24].

2.11. Power Consumption

Under static bar state or cross state, the driving current across the device is nearly zero, and the device almost consumes no power, e.g., $PC_{sta} \approx 0$; however, under the exchange of operation state, the charge current results in power loss on R_g . The energy needed per bit and the PC are defined by, respectively

$$E_{\rm dyn}^{\rm b}(f_{\rm m}) = (1/R_{\rm g}) \int_{0}^{T_{\rm m}} \left[V_g(t) - u(t) \right]^2 {\rm d}t \tag{16}$$

$$\mathbf{P}\mathbf{C}_{\mathsf{dyn}}(f_{\mathsf{m}}) = \mathbf{E}_{\mathsf{dyn}}^{\mathsf{b}} \times f_{\mathsf{m}}.$$
(17)

Curves of E_{dyn}^{b} and PC_{dyn} versus f_{m} are shown in Fig. 5(e). It can be seen that, as f_{m} increases, the needed PC also increases, and under the maximum switching frequency of 25 GHz, the energy needed for one bit is about 1.05 pJ, and the average power is about 25.7 mW. The consumed power is 0.15 mW when f_{m} decreases to 1 GHz, and that is 10^{-5} mW when f_{m} drops to 10 MHz.



Fig. 6. (a) Diagram of the 4 × 4 RSA. (b) When $U_3 = U_4 = 0$ V, output powers from ports N, E, and S versus the applied voltages $U = U_1 = U_2$. (c) When $U_2 = U_4 = 0$ V, output powers from ports N, E, and S versus the applied voltages $U = U_1 = U_3$. (d) Responses under the exchange between W → N state and W → S state operated with 1 GHz switching signal. (e) PC and energy needed per bit under different switching frequencies.

TABLE 1
Routing conditions of 4 \times 4 RSA under the typical operation of light inputting into port W

Input	Output	U_1	U_2	U_3	U_4
	N	0	0	0	0
W	Е	V_{s}	$V_{\rm s}$	0	0
_	S	$V_{\rm s}$	0	V_{s}	0

3. Design Scheme of 4 \times 4 RSA

3.1. Structure and Formulation

By using two basic 2 \times 2 cross/bar EO switches, a 4 \times 4 RSA is proposed, and it can route a 1550-nm data stream from one direction to any one of other three directions under the operations of the four applied voltages U_1 , U_2 , U_3 , and U_4 , as shown in Fig. 6(a). Typically, letting the light input into the west port, when the light outputs from the north port, east port, and south port, the related transfer functions can be obtained by

$$M_{W \to N}(U_1, U_2, U_3) = |V(U_1) \times \exp[-j(2\psi_1)]|^2$$
(18)

$$M_{W \to E}(U_1, U_2, U_3) = |U(U_1) \times U(U_2) \times \exp[-j(2\psi_1 + \psi_3)]|^2$$
(19)

$$M_{W \to S}(U_1, U_2, U_3) = |U(U_1) \times V(U_2) \times U(U_3) \times \exp[-j(2\psi_1 + 2\psi_3)]|^2$$
(20)

where $\psi_3 = L_2(\beta_c - j\alpha_c)$, and $L_2 = 1000 \ \mu m$. The output powers in decibel form are given by

$$P_{W \to N} = 10 \log[M_{W \to N}(U_1, U_2, U_3)]$$
(21)

$$P_{W \to E} = 10 \log[M_{W \to E}(U_1, U_2, U_3)]$$
(22)

$$P_{W\to S} = 10 \log[M_{W\to S}(U_1, U_2, U_3)].$$
(23)

According to (21)-(23), the routing conditions are concluded and listed in Table 1.

Taking the routing operation $W \rightarrow N$ as an example, the insertion loss is defined as

$$IL_{W \to N} = 10 \log[M_{W \to N}(U_1, U_2, U_3)]$$
(24)

and the crosstalk between port N and port E and that between port N and port S are defined as, respectively

$$CT_{W\to N}^{NE} = 10 lg \left[\frac{M_{W\to E}(U_1, U_2, U_3)}{M_{W\to N}(U_1, U_2, U_3)} \right]$$
(25)

$$CT_{W \to N}^{NS} = 10 lg \left[\frac{M_{W \to S}(U_1, U_2, U_3)}{M_{W \to N}(U_1, U_2, U_3)} \right].$$
 (26)

The insertion loss and crosstalk under other two routing operations can be similarly characterized.

Routing characteristics of 4×4 RSA

State	$IL_{W \rightarrow N}$	$CT_{W \rightarrow N}^{NE}$	$CT_{W \rightarrow N}^{NS}$	$IL_{W \to E}$	$CT_{W \rightarrow E}^{EN}$	$CT_{W \rightarrow E}^{ES}$	$IL_{W \rightarrow S}$	$CT_{W \rightarrow S}^{SN}$	$CT_{W \rightarrow S}^{SE}$
W-N	2.42	-59.9	-62.3	·	_	_	_	_	_
W-E		_		0.20	-39.8	-71.1	-	··	
W-S			_	—			2.57	-37.5	-28.7
	N N Z	N	N ₁ N _{p2}	N ₂	1.0 65 ps	f _m = 1 C	3Hz 10 10'		6

TABLE 2

Fig. 7. Diagram and routing paths of 8 \times 8 RSA, and light is lunching into port (a) W_{i1}, and (b) W_{i2}. (c) Response under the exchange between W_{i1} \rightarrow N_{o1} state and W_{i1} \rightarrow S_{o2} state operated with 1 GHz switching signal. (d) PC and energy needed per bit under different switching frequencies.

3.2. Routing Performance

In terms of (18)–(23), when $U_3 = U_4 = 0$ V, Fig. 6(b) exhibits the output powers from ports N, E, and S versus the applied voltage $U_1 = U_2$. It is shown that, when $U_1 = U_2 = 0$ V, the output power from port N becomes the maximum, which is named W \rightarrow N state. When $U_1 = U_2 = 5$ V, the output power from port E becomes the maximum, which is named W \rightarrow E state. When $U_2 = U_4 = 0$ V, Fig. 5(c) exhibits the output powers from ports N, E, and S versus $U = U_1 = U_3$. It can be seen that, when $U_1 = U_3 = 0$ V, the device is set to be W \rightarrow N state. When $U_1 = U_3 = 5$ V, the output power from port S is the maximum, which is named W \rightarrow S state. The characteristics including insertion loss and crosstalk under each state are concluded and listed in Table 2.

In the following sections, to estimate the characteristics of 8×8 and $N \times N$ RSAs based on this 4×4 switching element, we define nine losses under the three routing operations as follows: (1) under $W \rightarrow N$ state, N-ON-loss $l_{11} = 2.42$ dB, E-OFF-loss $l_{12} = 62.3$ dB, and S-OFF-loss $l_{13} = 64.7$ dB; (2) under $W \rightarrow E$ state, N-OFF-loss $l_{21} = 40.04$ dB, E-ON-loss $l_{22} = 0.20$ dB, and S-OFF-loss $l_{23} = 71.25$ dB; (3) under $W \rightarrow S$ state, N-OFF-loss $l_{31} = 40.04$ dB, E-OFF-loss $l_{32} = 31.26$ dB, and S-ON-loss $l_{33} = 2.57$ dB. The first number in the subscript denotes different operation states (1, 2, and 3 correspond to $W \rightarrow N$, $W \rightarrow E$, and $W \rightarrow S$), and the second number in the subscript denotes different output ports (1, 2, and 3 correspond to ports N, E, and S). Moreover, because of similar operations, we also name $N \rightarrow E$, $E \rightarrow S$ and $S \rightarrow W$ states as $W \rightarrow N$ state, $N \rightarrow S$, $E \rightarrow W$ and $S \rightarrow N$ states as $W \rightarrow E$ state, and $N \rightarrow W$, $E \rightarrow N$ and $S \rightarrow E$ states as $W \rightarrow S$ state. The same nine loss parameters can also be defined under a similar operation. Still, under $W \rightarrow N$ state, we name the port under ON-state as *N*-ON-port, and other two ports as *E*-OFF-port and *S*-OFF-port, respectively. Other cases can be similarly treated.

By taking the capacitances of four rings' electrode into consideration, the dynamic responses and PC are similarly obtained and shown in Fig. 6(d) and (e), respectively. The 4×4 RSA reveals nearly similar response times (85 ps and 165 ps) with those of the 2×2 basic element at 1 GHz. The dynamic PC and energy needed per bit under 1-GHz switching operation are calculated to be 0.21 mW and 0.21 pJ/bit, respectively.

4. Design Scheme of 8 \times 8 RSA

4.1. Structure and Typical Routing Scheme

By using four 4 × 4 RSAs (sixteen 2 × 2 cross/bar routing switches), an 8 × 8 RSA is built, and there are two input ports and two output ports in each direction, as shown in Fig. 7. The four applied voltages on the microrings of the (i, j)th basic RSA element are denoted by U_{ii}^1 , U_{ii}^2 , U_{ii}^3 , and U_{ii}^4 ,



Fig. 8. When light is lunching into port W_{i1} , curves of output powers from all ports versus the needed voltage change, under the cases of the 8 × 8 RSA exchanging from $W_{i1} \rightarrow N_{o1}$ state to (a) $W_{i1} \rightarrow N_{o2}$, (b) $W_{i1} \rightarrow E_{o1}$, (c) $W_{i1} \rightarrow E_{o2}$, (d) $W_{i1} \rightarrow S_{o1}$, (e) $W_{i1} \rightarrow S_{o2}$, and (f) $W_{i1} \rightarrow W_{o2}$. (g) Insertion loss of each ON-port and (h) the maximum crosstalk between each ON-port and other OFF-ports.

respectively. Taking the light inputting into the west port for example, there are two typical routing operations, including the light lunching into port W_{i1} [Fig. 7(a)] and that into W_{i2} [Fig. 7(b)]. The routing paths under each case are also labeled in these two figures.

4.2. Routing Performance Under the Case of Light Lunching Into Wi1

When the light inputs into port W_{i1} [see Fig. 7(a)], the amplitude transfer functions along each path are expressed as

$$M_{W_{i1} \to N_{o1}} = \left| V(U_{11}^{1}) \times \exp[-j(2\psi_{1})] \right|^{2}$$
(27)

$$M_{W_{11} \to N_{02}} = \left| U(U_{11}^1) \times U(U_{11}^2) \times V(U_{12}^1) \times \exp[-j(4\psi_1 + \psi_3)] \right|^2$$
(28)

$$M_{W_{11} \to E_{01}} = \left| U(U_{11}^{1}) \times U(U_{11}^{2}) \times U(U_{12}^{1}) \times U(U_{12}^{2}) \times \exp[-j(4\psi_{1} + 2\psi_{3})] \right|^{2}$$

$$M_{W_{11} \to E_{02}} = \left| U(U_{11}^{1}) \times U(U_{12}^{2}) \times U(U_{12}^{1}) \times V(U_{12}^{2}) \times V(U_{12}^{2}) \right|^{2}$$
(29)

$$N_{i_{1}} \rightarrow E_{o2} = \left| U(U_{11}^{1}) \times U(U_{11}^{2}) \times U(U_{12}^{1}) \times V(U_{12}^{2}) \right|^{2} \times U(U_{12}^{3}) \times V(U_{22}^{2}) \times \exp[-j(6\psi_{1} + 3\psi_{3})] \right|^{2}$$
(30)

$$M_{W_{11} \to S_{01}} = \left| U(U_{11}^1) \times V(U_{11}^2) \times U(U_{11}^3) \times U(U_{21}^2) \times U(U_{21}^3) \times \exp[-j(4\psi_1 + 3\psi_3)] \right|^2$$
(31)

$$M_{W_{11} \to S_{02}} = \left| U(U_{11}^{1}) \times U(U_{11}^{2}) \times U(U_{12}^{1}) \times V(U_{12}^{2}) \right|$$

$$\times U(U_{12}^3) \times U(U_{22}^2) \times U(U_{22}^3) \times \exp[-j(6\psi_1 + 4\psi_3)]|^2$$
(32)

$$M_{W_{11} \to W_{02}} = \left| U(U_{11}^{1}) \times V(U_{11}^{2}) \times U(U_{11}^{3}) \times U(U_{21}^{2}) \times V(U_{21}^{3}) \right. \\ \left. \times (U_{21}^{4}) \times \exp[-j(4\psi_{1} + 4\psi_{3})] \right|^{2}.$$
(33)

Noticing that, for any *i*, *j*, and *p*, when $U_{ij}^p = 0$ V, the device is set to be $W_{i1} \rightarrow N_{o1}$ state, which can be treated as a normal state. To enable the device to exchange from $W_{i1} \rightarrow N_{o1}$ state to $W_{i1} \rightarrow N_{o2}$

state, voltages U_{11}^1 and U_{11}^2 should be both changed from 0 to 5 V. Using (27)–(33), Fig. 8(a) shows the curves of the output powers from all ports versus the change of U_{11}^1 and U_{11}^2 . It can be seen that, when $U_{11}^1 = U_{11}^2 = 5$ V, the output power from port N_{02} becomes the maximum, and the maximum crosstalk relative to other ports is about -37.4 dB. Similarly, in order to enable the device to exchange from $W_{i1} \rightarrow N_{01}$ state to $W_{i1} \rightarrow E_{01}$ state, voltages U_{11}^1 , U_{12}^1 , U_{12}^1 , and U_{12}^2 should all be changed from 0 to 5 V. Fig. 8(b) shows the curves of the output powers from all ports versus the change of U_{11}^1 , U_{12}^1 and U_{12}^2 . It can be seen that, when $U_{11}^1 = U_{11}^2 = U_{12}^1 = U_{12}^1 = 5$ V, the output power from port E_{01} becomes the maximum, and the maximum crosstalk is about -39.7 dB. The situations of the device exchanging from $W_{i1} \rightarrow N_{01}$ to $W_{i1} \rightarrow E_{02}$, $W_{i1} \rightarrow S_{01}$, $W_{i1} \rightarrow S_{02}$, and $W_{i1} \rightarrow W_{02}$ are similarly analyzed and shown in Fig. 8(c)–(f), respectively, and the maximum crosstalk are observed to be about -26.3, -30.9, -28.5, and -28.7 dB, respectively. The insertion loss of each ON-port and the maximum crosstalk between each ON-port and other OFF-ports are summarized and shown in Fig. 8(g) and (h), respectively. Therefore, under this situation, among all routing operations, the maximum insertion loss is about 5.19 dB, and the maximum crosstalk is about -26.3 dB.

4.3. Routing Performance Under the Case of Light Lunching Into W_{i2}

When the light inputs into port W_{i2} [see Fig. 7(b)], the amplitude transfer functions along each path are expressed as

$$M_{W_{i2} \to W_{o1}} = \left| V(U_{21}^{1}) \times V(U_{11}^{4}) \times \exp[-j(4\psi_{1})] \right|^{2}$$
(34)

$$M_{W_{12} \to N_{01}} = \left| V(U_{21}^1) \times U(U_{11}^4) \times U(U_{11}^1) \times \exp[-j(4\psi_1 + \psi_3)] \right|^2$$
(35)

$$M_{W_{12} \to N_{02}} = \left| U(U_{21}^{1}) \times U(U_{21}^{2}) \times V(U_{22}^{1}) \times U(U_{12}^{4}) \times U(U_{12}^{1}) \times \exp[-j(6\psi_{1} + 2\psi_{3})] \right|^{2}$$
(36)
$$M_{W_{12} \to E_{01}} = \left| U(U_{21}^{1}) \times U(U_{21}^{2}) \times V(U_{22}^{1}) \times U(U_{12}^{4}) \right|^{2}$$

$$\times V(U_{12}^{1}) \times U(U_{12}^{2}) \times \exp[-j(6\psi_{1} + 3\psi_{3})]|^{2}$$
(37)

$$M_{W_{12} \to E_{02}} = \left| U(U_{21}^1) \times U(U_{21}^2) \times U(U_{22}^1) \times U(U_{22}^2) \times \exp[-j(4\psi_1 + 2\psi_3)] \right|^2$$
(38)

$$M_{W_{12} \to S_{01}} = \left| U(U_{21}^1) \times V(U_{21}^2) \times U(U_{21}^3) \times \exp[-j(2\psi_1 + 2\psi_3)] \right|^2$$
(39)

$$M_{\mathsf{W}_{12}\to\mathsf{S}_{02}} = \left| U(U_{21}^1) \times U(U_{21}^2) \times U(U_{22}^1) \times V(U_{22}^2) \times U(U_{22}^3) \times \exp[-j(4\psi_1 + 3\psi_3)] \right|^2.$$
(40)

Similarly, when $U_{ij}^p = 0$ V (for any *i*, *j* and *p*), the device is set to be $W_{i2} \rightarrow W_{o1}$ state, which can be treated as a normal state. The situations of the device exchanging from $W_{i2} \rightarrow W_{o1}$ to $W_{i2} \rightarrow N_{o1}$, $W_{i2} \rightarrow N_{o2}$, $W_{i2} \rightarrow E_{o1}$, $W_{i2} \rightarrow E_{o2}$, $W_{i2} \rightarrow S_{o1}$, and $W_{i2} \rightarrow S_{o2}$ are shown in Fig. 9(a)–(f), respectively, and the maximum crosstalk is observed to be about -39.9, -39.7, -28.7, -42.1, -39.9, and -28.7 dB, respectively. The insertion loss of each ON-port and the maximum crosstalk between each ON-port and other OFF-ports are shown in Fig. 9(g) and (h), respectively. Under this situation, the maximum insertion loss is about 5.19 dB, and the maximum crosstalk is about -28.7 dB.

4.4. Switching Time and Power Consumption

Since the routing path from port W_{i1} to S_{o2} is the longest one within all paths, and up to 16 rings should be applied with the switching voltage of 5 V for realizing $W_{i1} \rightarrow S_{o2}$ state. The increased number of rings enhances the equivalent capacitance C_{eq} , and the dynamic responses including both electrical and optical [given by (12) and (15)], as well as the PC will be modified, as shown in Fig. 7(c) and (d). The rise time and fall time of the 8 × 8 RSA are determined to be 40 ps and 71 ps, respectively. The dynamic PC and energy needed per bit under 1-GHz switching operation are calculated to be 0.52 mW and 0.52 pJ/bit, respectively.



Fig. 9. When light is lunching into port W_{i2} , curves of output powers from all ports versus the needed voltage change, under the cases of the 8 × 8 RSA exchanging from $W_{i2} \rightarrow W_{o1}$ state to (a) $W_{i2} \rightarrow N_{o1}$, (b) $W_{i2} \rightarrow N_{o2}$, (c) $W_{i2} \rightarrow E_{o1}$, (d) $W_{i2} \rightarrow E_{o2}$, (e) $W_{i2} \rightarrow S_{o1}$, and (f) $W_{i2} \rightarrow S_{o2}$. (g) Insertion loss of each ON-port and (h) the maximum crosstalk between each ON-port and other OFF-ports.

4.5. Rule of the Maximum Crosstalk Determination

For a definite routing operation, the most important thing we concerned is the maximum crosstalk of an ON-port relative to other OFF-ports. So, in this paper, given the input port, output port, and definite routing path, a rule is found to decide the OFF-port, which has the maximum crosstalk relative to an ON-port. Since $l_{32} < l_{31} = l_{21} < l_{12} < l_{13} < l_{23}$, the analytical steps are concluded below.

- 1) Along each routing path, find out whether there is any E-OFF-port or N-OFF-port reveals $W \rightarrow S$ state with the input light. If so, this port is the desired port. Exit the searching process.
- Along each routing path, find out whether there is any N-OFF-port reveals W → E state with the input light. If so, this port is the desired port. Exit the searching process.
- 3) Along each routing path, find out whether there is any E-OFF-port and S-OFF-port reveals $W \rightarrow N$ state with the input light. If so, this port is the desired port. Exit the searching process.
- Along each routing path, find out whether there is any S-OFF-port reveals W → E state with the input light. If so, this port is the desired port. Exit the searching process.
- 5) If there is no port satisfying (1) \sim (4), find out the subport of each element satisfying (1) \sim (4), and then, the port which possesses the minimum loss is the desired port.

For example, in Fig. 7(a), when the routing operation is $W_{i1} \rightarrow N_{o1}$, there is no direct output port satisfying (1) \sim (4); However, the east port (named subport) of the (1, 1) element is its E-OFF-port, and N_{o2} is directly linked to this subport. So, port N_{o2} reveals the maximum crosstalk with port N_{o1} . When the routing operation is $W_{i1} \rightarrow N_{o2}$, N_{o1} is the N-OFF-port reveals $W \rightarrow E$ state with the input light. So, N_{o1} reveals the maximum crosstalk with port N_{o2} . Other cases can be similarly analyzed. The OFF-port with the maximum crosstalk relative to every ON-port is concluded and shown in Table 3, where the results are perfectly in accordance with those shown in Figs. 8 and 9.

Input	Output	Insertion loss	The maximum crosstalk and Port	Input	Output	Insertion loss	The maximum crosstalk and port
	N _{ol}	<i>I</i> ₁₁	$-l_{12}$, N _{o2}		N ol	$l_{22} + l_{11}$	$-(l_{21}-l_{22})$, W ₀₁
	N_{o2}	$l_{22} + l_{11}$	$-(l_{21}-l_{22}-l_{11}), N_{o1}$		N_{o2}	$2l_{22} + l_{11}$	$-(l_{21}-2l_{22}), W_{o1}$
	E _{o1}	2 <i>l</i> ₂₂	$-(l_{21}-l_{22})$, N ₀₂		E _{ol}	$l_{22} + l_{33} + l_{11}$	$-(l_{32}-l_{33})$, N ₀₂
W	E _{o2}	$l_{22} + l_{33} + l_{11}$	$-(l_{32}-l_{33}-l_{11})$, E ₀₁	W _{i2}	E _{o2}	2 <i>l</i> ₂₂	$-(l_{11}+l_{21}-2l_{22}), W_{o1}$
vv _{i1}	\mathbf{S}_{o1}	$l_{33} + l_{22}$	$-(l_{32}+l_{11}-l_{33}-l_{22})$, N		\mathbf{S}_{o1}	l ₃₃	$-(l_{11}+l_{31}-l_{33})$, W _{o1}
	S_{o2}	$l_{33} + 2l_{22}$	$-(l_{32}-l_{33}-l_{22})$, E ₀₁		S 02	$l_{22} + l_{33}$	$-(l_{32}-l_{33})$, E ₀₂
	W_{o1}	_	_		W_{o1}	2 <i>l</i> ₁₁	$-(l_{13}-2l_{11})$, S ₀₁
	W _{o2}	21,33	$-(l_{32}-l_{33})$, S ₀₁		W _{o2}	_	_

TABLE 3

For the 8 \times 8 RSA, the Insertion loss of each ON-port, the maximum crosstalk and the corresponding port under different routing states



Fig. 10. Diagram and routing paths of $N \times N$ RSA. The light is input into (a) port W_{i1}, (b) port W_{ik}, and (c) port W_{in}.

5. Scalability and Performances of $N \times N$ RSA

5.1. Structure and Routing Scheme of $N \times N$ RSA

As shown in Fig. 10, by using $n^2 4 \times 4$ RSAs, a generic structure of an $N \times N$ RSA is proposed, where N = 4n is the number of input port and output port. When the light input into one input port in the west direction, the routing paths to other output ports are typically shown in Fig. 10, where the light is input into (a) port W_{i1}, (b) port W_{ik} (1 < k < n), and (c) port W_{in}.

Generally, when the light inputs into port W_{ik} ($1 \le k \le n$) only, for enabling the light to output from other ports, the routing scheme, including routing conditions, the insertion loss of each ON-port, and the maximum crosstalk relative to other OFF-ports, are depicted in Table 4, where the maximum crosstalk is determined using the similar technique given in Section 4.4. Typically, we analyze one routing situation $W_{i2} \rightarrow N_{o3}$ (n = 4, m = 3, k = 2) as an example. (1) First, for establishing this data link, the following requirements should be satisfied, including i) the (2, 1) element at $W \rightarrow E$ state, ii) (2, 2) element at $W \rightarrow E$ state, iii) (2, 3) element at $W \rightarrow N$ state, and iv) (1, 3) element at $W \rightarrow E$ state. So, the routing conditions including $U_{k,j}^1 = U_{k,j}^2 = V_s$, j = 1, .2 and $U_{1,m}^1 = U_{1,m}^4 = V_s$ should be required. (2) Along this path, only port W_{o1} is directly linked to the *N*-OFF-port of (2, 1) element at $W \rightarrow E$ state. Therefore, according to the rule given in Section 4.4, W_{o1} possesses the maximum crosstalk relative to port N_{o3} . (3) Form port W_{i2} to N_{o3} , there are three E-ON-losses under $W \rightarrow E$ state and one N-ON-loss under $W \rightarrow N$ state, so the insertion loss of this ON-port is $(k + m - 2)I_{22} + I_{11} = 3I_{22} + I_{11}$; from port W_{i2} to W_{o1} , there are one N-OFF-loss under $W \rightarrow E$ state and one N-ON-loss under $W \rightarrow N$ state, so the insertion loss of this OFF-port is $I_{21} + I_{11}$. Hence, the maximum crosstalk under this state is $3I_{22} - I_{21}$. Other cases in the table can be similarly analyzed, and with this table, the maximum insertion loss and the maximum crosstalk can be predicted.

TABLE 4

When the light is lunching into port W_{ik} ($1 \le k \le n$), routing conditions, insertion loss and the maximum crosstalk under different routing state

Input	Output	Routing condition	Insertion loss	The maximum crosstalk port and its insertion loss	
<u>.</u>	N _{o1}	$U_{j,1}^{1} = U_{j,1}^{4} = V_{s}, j = 1,k-1^{Note1}$			
W _{ik}	$N_{om}, m \ge 1$	$U_{k,j}^{1} = U_{k,j}^{2} = V_{s}, j = 1,m - 1$ $U_{k,m}^{1} = U_{k,m}^{4} = V_{s}, j = 1,k - 1$	$(k+m-2)l_{22}+l_{11},$ $m \ge 1$	$w_{ol}, (k-2)t_{22} + t_{21} + t_{11} m = 1$ $W_{ok-1}, t_{21} + t_{11}, m > 1$	
	$E_{om}, \\ 1 \le m \le k$	$U_{k,j}^{1} = U_{k,j}^{2} = V_{ss,j} = 1,n-1$ $U_{j,n}^{1} = U_{j,n}^{4} = V_{ss,j} = m+1,k-1$ $U_{m,n}^{2} = U_{m,n}^{4} = V_{s}$	$(n+k-m-2)I_{22}+I_{33}+I_{11}$	Non. (n+k-3) l22 + l33 + l32 ,m=1	
	E _{ok}	$U_{k,j}^1 = U_{k,j}^2 = V_{s}, j = 1,n$	<i>nl</i> ₂₂	W_{ok-1} , $l_{21} + l_{11}$, $1 \le m \le k$	
	$E_{om}, m > k$	$\begin{split} U_{k,j}^1 = U_{k,j}^2 = V_{s,j} = 1,n{-}1 \\ U_{k,n}^1 = U_{k,n}^3 = V_s \\ U_{i,n}^2 = U_{i,n}^3 = V_s, i = k{+}1,m{-}1 \end{split}$	$(n+m-k-2)l_{22}+l_{33}+l_{11}$	$E_{\text{ok}}, (n-1)l_{22}+l_{32} m > k$	
	S _{o1}	$U_{k,1}^{1} = U_{k,1}^{3} = V_{s}$ $U_{i,1}^{2} = U_{i,1}^{3} = V_{s}, i = k+1,n$		W_{ok-1} , $I_{31} + I_{11}$, $m = 1$	
	$S_{om}, m > 1$	$U_{k,j}^{1} = U_{k,j}^{2} = V_{s,j} = 1,m-1$ $U_{k,m}^{1} = U_{k,m}^{3} = V_{s}$ $U_{i,m}^{2} = U_{i,m}^{3} = V_{s}, i = k+1,n$	$(n+m-k-1)I_{22}+I_{33}$	$W_{ok-1}, l_{21} + l_{11}, 1 \le m \le n$ E _{ok} , $(n-1)l_{22} + l_{32}, m = n$	
	$W_{om}, m \le k$	$U_{i,1}^1 = U_{i,1}^4 = V_{s}, i = m+1,k-1$	$(k-m-1)l_{22}+2l_{11}$	W _{om+1} , $(k-m-3)l_{22}+l_{21}+l_{11}, 1 \le m \le k-1$	
	$W_{om}, m > k$	$\begin{split} U_{k,1}^{1} = U_{k,1}^{3} = V_{s} \\ U_{i,1}^{2} = U_{i,1}^{3} = V_{s}, \ i = k+1, \m-1 \\ U_{m,1}^{2} = U_{m,1}^{4} = V_{s} \end{split}$	$(m-k-1)l_{22}+2l_{33}$	$\begin{split} & W_{\text{om+2,}} 2l_{13}, m = k - 1 \\ & W_{\text{ok-1,}} l_{31} + l_{11}, k < m \le n - 1 \\ & S_{\text{o1}}, (n - k - 1)l_{22} + l_{33} + l_{32}, m = n \end{split}$	

Note1: if k - 1 < 0, the corresponding condition is not required. Others in this table can be similarly treated.

5.2. Characteristics Formulation on $N \times N$ RSA

1) The maximum and minimum insertion losses and the maximum crosstalk. For an $N \times N$ RSA, let the light input into W_{ik} , within all routing operations, define the minimum and the maximum insertion losses IL_{min} and IL_{max} as

$$IL_{\min} = \min_{k=1}^{n} \min_{i=1}^{N} IL_{\text{Port}_{i}}^{W_{ik}}, i \neq 3n+k, IL_{\max} = \max_{k=1}^{n} \max_{i=1}^{N} IL_{\text{Port}_{i}}^{W_{ik}}, i \neq 3n+k$$
(41)

where $IL_{\text{Port }i}^{W_{ik}}$ denotes the propagation loss from the input port W_{ik} to the ON-port i, port number $i = 1 \sim n$ denotes port $N_{o1} \sim N_{on}$, $i = n + 1 \sim 2n$ denotes $E_{o1} \sim E_{on}$, $i = 2n + 1 \sim 3n$ denotes $S_{o1} \sim S_{on}$, and $i = 3n + 1 \sim 4n$ denotes port $W_{o1} \sim W_{on}$. Similarly, define the maximum crosstalk CT_{max} as

$$CT_{\min} = \max_{k=1}^{n} \max_{i=1}^{N} CT_{\text{Port}i}^{W_{\text{ik}},\max}, i \neq 3n+k$$
(42)

where $CT_{Port i}^{max}$ is the maximum crosstalk of port *i* under ON-state relative to other OFF-ports when light inputs into W_{ik}.

2) Electrical and optical responses. Let the light input into W_{i1} . For an $N \times N$ RSA, along the longest routing path from W_{i1} to S_{on} , there are totally 2N - 4 active rings, so during solving the dynamic electrical response u(t) from (12) and (13), the equivalent capacitance should be modified to

$$C_{\rm eq} = (2N-4)C_{\rm R} + C_{\rm pad}. \tag{43}$$



Fig. 11. Electrical responses (at 1 GHz), optical responses (at 1 GHz) and PCs (at 1 GHz) of the 16 \times 16, 32 \times 32, 64 \times 64, and 80 \times 80 RSAs.

Under certain switching frequency f_m , the dynamic optical responses from the nearest port N_{o1} and the farthest port S_{on} can be determined as

$$M_{W_{11} \to N_{01}}^{f_{m}}(t) = |V[u(t)] \times \exp[-j(2\psi_{1})]|^{2}$$

$$M_{W_{11} \to N_{01}}^{f_{m}}(t) = \left| \{U[u(t)]\}^{N/2 - 1} \times V(0) \times \{U[u(t)]\}^{N/2 - 1} \times U(0) \} \right|^{N/2 - 1} \times U(0)$$
(44)

$$\mathcal{M}_{W_{11} \to S_{on}}^{m}(t) = \left| \{ U[u(t)] \}^{N/2-1} \times V(0) \times \{ U[u(t)] \}^{N/2-1} \times \exp[-j[(N-2)\psi_1 + (N\psi_3/2)]] \right|^2$$
(45)

3) Response time. When port No1 is at ON-state, the crosstalk between port No1 and port Son is

$$CT_{N_{o1} \to S_{on}}(f_{m}) = 20 \lg \frac{\min \left[M_{W_{i1} \to S_{on}}^{f_{m}}(t) \right]}{\max \left[M_{W_{i1} \to N_{o1}}^{f_{m}}(t) \right]}.$$
(46)

When port S_{on} is at ON-state, the crosstalk between port S_{on} and port N_{o1} is

$$CT_{N_{o1} \rightarrow S_{on}}(f) = 20 \lg \frac{\min \left[M_{W_{i1} \rightarrow N_{o1}}^{f_{m}}(t) \right]}{\max \left[M_{W_{i1} \rightarrow S_{on}}^{f_{m}}(t) \right]}.$$
(47)

The 10%–90% rise time and fall time are characterized by those under the switching frequency of 1 GHz, e.g.,

$$t_{\rm r}, t_{\rm f} = t_{\rm r}, t_{\rm f}|_{t_{\rm m}=1\,{\rm GHz}}.$$
 (48)

4) Dynamic PC needed for the switching between ports N_{o1} and S_{on}. With the dynamic electrical response, *PC*_{dyn}(*f*_m) and *E*^b_{dyn}(*f*_m) under the switching frequency of *f*_m can be calculated from (16) and (17), and here, the values at the frequency of 1 GHz are used for representing such characteristic of an *N* × *N* RSA, e.g.,

$$PC_{dyn}, E_{dyn}^{b} = PC_{dyn}, E_{dyn}^{b}|_{f_{m}=1GHz}.$$
(49)

5) Device width and square. The length (or width) and device square of the $N \times N$ RSA are, respectively

$$L_{\text{total}} = (2L_1 + L_2 + 2L_3)N/4, S_{\text{total}} = L_{\text{total}} \times L_{\text{total}}.$$
(50)

With (43)–(49), the RSA with relatively large sizes (N = 16, 32, 64, 80) are analyzed, and their electrical responses (at 1 GHz), optical responses (at 1 GHz), and PCs (at 1 GHz) are shown in Fig. 11(a)–(c), respectively. One can observe that, as the increase of N, these three aspects are changed, that is, the performances are dependent on N, and the dependence relations should be



Fig. 12. Dependences of the performances of $N \times N$ RSA on RSA size (characterized by *N*). (a) The minimum insertion loss, the maximum insertion loss and the maximum crosstalk. (b) Device width, length and square. (c) Response time. (d) PC. (e) Performance fitting equations on RSA size *N*.

derived for predicting the scalability of such kind of routing devices. This will be discussed in Section 5.3.

5.3. Performances Dependence on RSA Size

The performance dependences of the routing device on RSA size (characterized by N) are predicted and shown in Fig. 12. It is shown in Fig. 12(a) that the maximum insertion loss and crosstalk both increase linearly with the increase of N. When N is small, the minimum insertion loss mainly depends on the through loss to the ON-port, and when N is large enough, this loss is larger than the OFF-loss to the neighboring drop port, so the value keeps constant to be the OFF-loss to the neighboring drop port. It is shown in Fig. 11(b) that the device size gets large as N rises. When the RSA size is 80, e.g., the number of input port and that of output port are both 80, the maximum insertion loss within all routing operations is about 12 dB, the maximum crosstalk is less than -22 dB, and the device square is about 6 cm \times 6 cm. The device square can be decreased by shortening L_1 and L_2 , and when they are equal to 200 μ m, the device square of the 80 \times 80 RSA can be decreased to 1.7 cm imes 1.7 cm and those of the 4 imes 4 RSA can be decreased to 0.8 mm imes 0.8 mm. One can find from Fig. 11(c) that, as the increase of N, the rise time drops from \sim 80 ps to \sim 10 ps, while the fall time increases from \sim 165 ps to \sim 490 ps, which can also be verified by the optical responses in Fig. 11(b). As N increases from 4 to 80, the dynamic PC for switching the device at 1 GHz is changed from 0.21 mW to 16.9 mW, due to the variation of electrical response both in amplitude and waveform, as shown in Fig. 12(d). The performance dependences on RSA size are concluded in Fig. 12(e) through data fitting or existing relations.

5.4. Speculations on Device Fabrication Technology

The polymer material can be deposited directly on silicon substrate, and the fabrication technologies are compatible with Si and GaAs processing technologies. Besides, compared with reactive ion beam etching (RIE), photobleaching, and ion-implantation processes, laser [43] and electron beam [44] direct writings are more advantageous because fewer steps are involved. The direct writing technique has the advantage of being maskless, allowing rapid and inexpensive prototyping, in contrast to conventional mask-based photolithographic approach in which a mask must be made before the waveguide devices can be fabricated. Nanometer patterns with flexibility in writing complex structures by electron-beam direct writing are also possible. Therefore, the proposed device can be made through direct writing technique for obtaining nanometer scales, which is desired on the precise control of coupling gap between ring and channel waveguide, as well as ring radius. The electrode can be patterned through deposition technology.

5.5. Comparison and Discussion

 Comparison on basic MRR switching element. Table 5 lists the comparison results among the proposed polymer MRR EO switch (2 × 2 basic element) and the reported MRR EO switches based on silicon, LiNbO₃, InGaAsP, and GaAs. i) Because of large refractive indices (> 3.0) of silicon, GaAs, and InGaAsP, the ring radius based on these materials is usually less than 10 μm.

TABLE 5

Comparison among the reported MRR EO switches [17]–[19], [20], [22], [23], [42] and the proposed 2×2 polymer MRR EO switch. RT: response time; ER: extinction ratio; IL: insertion loss; thr: through port; drop: drop port

Structure/principle/Ref	Material	Ring radius (μm)/ FSR (nm)/ Static PC (mW)	RT (ns)	ER (dB)	Driving (V) Voltage	IL (dB)
1×2 single-ring add-drop switch/ carrier-injection dispersion/ [17]	silicon	5/8.45/NA	NA	32.9 (drop)	0/28.2	7.83 (thr) 2.59 (drop)
1×1 single-ring on-off switch/ Electric-field induced/[42]	LiNbO ₃	80.0/2/NA	NA	11	-10/10	NA
1×2 two-rings serial-coupled switch/ carrier-injection dispersion / [18]	InGaAsP	68.2/1.6/NA	~1	>30 (drop)	NA	NA
1×2 two-rings serial-coupled switch/ carrier-injection dispersion /[19]	silicon	~10/9/NA	1.7/0.8 ns (drop) 1.5/1.3 ns (thr)	13 (thr) 14 (drop)	0.2/0.8	NA
1×2 ten-rings serial-coupled switch/ carrier-injection dispersion /[23]	silicon	10/6/37	0.9/1.1 ns	10 (thr) 45 (drop)	0/1.2	~4.1 (thr) ~5.2 (drop)
1×2 two-rings serial-coupled switch/ carrier-injection dispersion /[22]	GaAs	5/NA/NA	NA	25 (thr) >40 (drop)	0/2	NA
1×2 two-rings serial-coupled switch/ carrier-injection dispersion /[20]	silicon	NA/9.1/NA	0.7/3.4	~8 (thr) ~9 (drop)	0/0.95	~2.5(thr) ~5 (drop)
2×2 two-rings cross-bar switch/ Electric-field induced/ [this]	polymer	13.8/17/0	0.07/0.14	31.1 (thr) 37.6 (drop)	0/5	0.11(thr) 2.42(drop)

TABLE 6

Comparison among the reported 4 \times 4 silicon channel wavelength routers [25]–[27] and the proposed 4 \times 4 RSA. CT: crosstalk; ER: extinction ratio

Device/Ref	Material	Wavelength Tuning Mechanism/Efficiency	Ring number	FSR (nm)	Driving Power or Voltage	The maximum CT or the minimum ER (dB)
4×4 channel wavelength router / [26]	silicon	TO / 0.25 nm/mW	8	8.8	6.5 mW for single ring	> 20 (ER)
4×4 channel wavelength router / [25]	silicon	TO / 0.18 nm/mW	8	NA	0~20.1 mW for device	<-13 (CT)
4×4 channel wavelength router / [27]	silicon	TO/ NA	8	8	NA	> 8 (ER)
4×4 channel wavelength RSA / [this]	polymer	EO/ 10 pm/V	8	17	5 V for device	<-26.3 (CT)

Though the polymer core has small index (~1.6), the polymer ring radius in this paper is also as small as 13.8 μ m with < 10⁻⁴ dB/cm bending loss, because air with an index of 1.0 is adopted as the left/right cladding material. ii) The index change of silicon or GaAs materials is based on carrier-injection dispersion effect, and at some operation states, the device consumes static power (as in [23]). This is different from this switch, whose static PCs at both states are nearly zero. iii) Because of effective carrier lift time, the response time of silicon and GaAs switches is usually at the level of ~ns, and this speed is slower than those of this switch and that reported in [42] based on electric-field-induced refractive index change.

- 2) Comparison between the proposed 4 × 4 routing switch and the ever reported 4 × 4 channel wavelength routers. It can be found from Table 6 that the obvious differences between this device and those in [25]–[27] are the used material and the wavelength tuning mechanism. This electric-field-based device consumes no power or less power than the TO-based silicon router. Moreover, this router has faster response speed due to fast electric-field-induced EO effect than those based on the slow-speed heat induced TO effect.
- 3) Comparison on the reported passive $N \times N$ routing topologies and this active routing scheme. One can find from Table 7 that the main function of the reported routers in [30], [45] is to select a channel wavelength from the input port and output it from another definite port. Therefore, the radii of the used rings are different, which are decided at the design stage of the router. So, the passive wavelength selective routers cannot be adopted in reconfigurable ONoCs. Besides, without the ability of wavelength tuning by TO or EO effect, more rings and waveguide crossings are desired for realizing nonblocking definite-path routing operation. For example, in this paper, $N^2/2$ rings are used compared with N(N - 2) rings in [30] and [45], and since

TABLE 7

Comparison among the reported passive $N \times N$ routing topologies [30], [45] and this active design scheme

Device/Ref	Network type/Function	Wavelength tuning	Ring radius	Ring number
N×N wavelength selective router / [45]	passive/definite-path routing operation	no	different	N(N-2) for even N $(N-1)^2$ for odd N
$N \times N$ wavelength selective router / [30]	passive/definite-path routing operation	no	different	N(N-2)
N×N RSA / [this]	active/reconfigurable-path routing operation	yes	identical	N ² /2

 $N/2 \le N-2$ (e.g., $N \ge 4$), the ring number in this paper is obviously less than those in [30] and [45].

6. Conclusion

Basic 2×2 element is firstly proposed, and by using four 2×2 elements, a 4×4 RSA is presented. The 8×8 RSA is also constructed with four 4×4 RSAs, and a rule to decide the OFF-port with the maximum crosstalk relative to every ON-port is derived. For an $N \times N$ RSA, routing scheme and formulation are achieved, and performance dependences on RSA size are also obtained. Comparisons confirm that this polymer-based routing scheme can be a good candidate in on-chip optical systems.

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