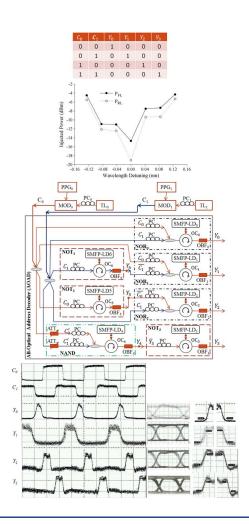




All-Optical Address Decoder Using Injection-Locking Property of External-Cavity-Based Single-Mode FP-LD

Volume 5, Number 2, April 2013

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DOI: 10.1109/JPHOT.2013.2259585 1943-0655/\$31.00 ©2013 IEEE





All-Optical Address Decoder Using Injection-Locking Property of External-Cavity-Based Single-Mode FP-LD

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DOI: 10.1109/JPHOT.2013.2259585 1943-0655/\$31.00 © 2013 IEEE

Manuscript received March 28, 2013; revised April 16, 2013; accepted April 18, 2013. Date of publication April 23, 2013; date of current version April 30, 2013. This work was supported by a grant from the R&D Program (Industrial Strategic Technology Development) funded by the Ministry of Knowledge Economy (MKE), Republic of Korea. Corresponding author: H. Tran Quoc (e-mail: hoaitq@ kaist.ac.kr).

Abstract: A novel all-optical address decoder (AOAD) using an external-cavity-based single-mode Fabry–Pérot laser diode (SMFP-LD) is proposed and demonstrated. The proposed AOAD is the combination of logic gates that are cascaded together to give specific functions of the decoder. The working principles of all logic gates are based on the single-and multi-input injection-locking properties of SMFP-LD. The outputs of the proposed AOAD have contrast ratios of above 27 dB in the spectrum domain, clear waveforms, and clear eyes diagrams with good BER at the data rate of 10 Gb/s. The proposed AOAD has several advantages such as a simple and cascadable structure, low cost, and low bias current (below 19 mA) compared with other optical technologies.

Index Terms: All-optical address decoder (AOAD), injection locking, single-mode Fabry–Pérot laser diode (SMFP-LD), optical processing.

1. Introduction

An address decoder is a circuit that has two or more bits of address bus as inputs and has one or more device selection lines as outputs. In electronics field, the address decoder is represented in all integrated-circuit families, processors, standard FPGA, and ASIC libraries [1]. Likewise, all-optical address decoder (AOAD) is the essential building block for all-optical systems that use optical buses. For example, AOAD should be presented in all-optical switching, control, memory, and future all-optical arithmetic logic units (ALUs) where outputs are based on the combination of inputs. In general, all-optical computing and controlling, using light instead of electrons as a fast and low energy replacement, have several advantages compared with those of electronics, such as higher bandwidth, data transparency, less power consumption [2], higher parallelism, more flexibility in layout, and less loss in communication [3]. To our knowledge, there has been only one proposal on AOAD so far using a semiconductor optical amplifier (SOA) [4]; however, the decoder scheme in [4] not only requires many components such as SOA, erbium-doped fiber amplifier (EDFA), and optical demultiplexer (DEMUX) but is also expensive and requires high bias current (~250 mA). To overcome the requirement of high current and expensive components, a Fabry-Pérot laser diode (FP-LD) may be one of the candidates for the same. Various optical units have been demonstrated using multimode FP-LD (MMFP-LD) [5], [6] and single-mode FP-LD (SMFP-LD) [7]-[9]; however, the cascading of many individual FP-LDs and the relationship between the required input power to

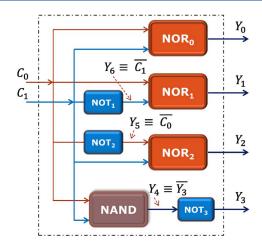


Fig. 1. Block diagram of an AOAD, where C_0 and C_1 are inputs; Y_0 , Y_1 , Y_2 and Y_3 are outputs; Y_4 , Y_5 and Y_6 are the outputs of NOT_3 , NOR_2 and NOT_1 which are the inputs of NOT_3 , NOR_2 and NOR_1 , respectively.

get fully lock state and to release locking state of the SMFP-LD at given wavelength detuning have not been considered in detail.

In this paper, we analyzed input power and detuning wavelength requirements to injection-lock SMFP-LD and released SMFP-LD's locking state, and we applied those principles to demonstrate a 2×4 AOAD using single- and multi-input injection-locking properties in SMFP-LD. Since SMFP-LD has self-locking mode, it does not need additional probe beam, which is required in other optical technologies [5], [6]. Hence, the proposed AOAD using SMFP-LD has several advantages such as simple in configuration, power and cost efficient, and cascadable structure.

2. Operation Principle

The proposed decoder operation is based on the single-input and multi-input injection-locking properties of SMFP-LDs, in which the self-locked mode (dominant mode) is suppressed when the single-input beam or multi-input beams is/are injected with proper input power and wavelength detuning [7]. In addition, the cascading property of SMFP-LDs also plays a crucial role for the implementation of AOAD. From the block diagram in Fig. 1, we can observe that AOAD is composed of several logic gates (NOT, NOR, and NAND), which are connected together to get the desired logic functions. The NOT and NOR gates work on single-input injection-locking principle in which power of single input at logic "1" is enough to suppress the dominant mode, whereas the NAND gate works on multi-input injection-locking principle, which states that the dominant mode will be suppressed only when all the inputs are logic "1" [8]. In multi-input injection-locking, the total input power of N injected beams is set in such a way that the dominant mode of SMFP-LD is suppressed only when all N inputs are logic "1", otherwise (one or more beam is/are logic "0") it is not suppressed. Since logic gates NOT, NOR, and NAND inside the AOAD are connected in cascading order, it is also possible to connect the AOAD in cascading order to make the desired complex functions. The cascadable feature can be obtained due to the fact that SMFP-LDs can be connected serially if input power and wavelength are controlled and matched properly for injection locking. In general, the locking strength of the input beam and hence the suppression of dominant mode is dependent on two parameters, i.e., wavelength detuning range and input power, which are related to each other. Lower detuning requires lower injected power for injection locking, and higher wavelength detuning needs higher input power. However, too small wavelength detuning may cause unstable locking. The relationship between wavelength detuning and injection locking is experimentally measured, as shown in Fig. 2. The change in temperature will shift the dominant mode of the SMFP-LD, which can be considered as advantage as it provides wavelength tunability of SMFP-LD. To maintain the fixed dominant mode, the SMFP-LD was kept firmly by using

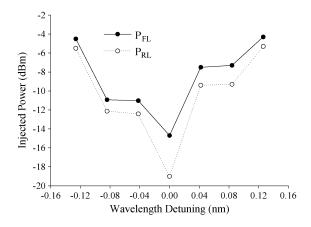


Fig. 2. Required power to get fully lock state (PFL) and to release locking state (PRL) of the SMFP-LD at given wavelength detuning.

TABLE 1

Truth table of an AOAD

C_0	c_1	<i>Y</i> ₀	<i>Y</i> ₁	<i>Y</i> ₂	<i>Y</i> ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

commercially available 4-pin coaxial pigtailed package, and its temperature was precisely controlled by using commercially available thermal electric cooler (TEC), which has the stability guarantee of less than 0.01 °C. Table 1 shows the truth table of AOAD, in which the outputs Y_0 , Y_1 , Y_2 , and Y_3 are logic "1" only when the input logic combination C_0 and C_1 is set at (0,0), (0,1), (1,0), and (1,1), respectively. All other combinations of inputs should provide the logic "0" at respective outputs. The Boolean expressions for output ports Y_0 , Y_1 , Y_2 , and Y_3 with inputs C_0 and C_1 can be written as $Y_0 = \overline{C_0 + C_1}$, $Y_1 = \overline{C_0 + Y_6} = \overline{C_0 + \overline{C_1}}$, $Y_2 = \overline{Y_5 + C_1} = \overline{C_0} + \overline{C_1}$, and $Y_3 = \overline{Y_4} = \overline{C_0}\overline{C_1} = C_0C_1$, and the corresponding expressions using logic gates are $Y_0 = NOR(C_0, C_1)$, $Y_1 = NOR(C_0, NOT(C_1))$, $Y_2 = NOR(NOT(C_0), C_1)$, and $Y_3 = NOT(NAND(C_0, C_1)) = AND(C_0, C_1)$. Hence, the experimental setup of the AOAD can be constructed, as shown in Fig. 3.

In Fig. 3, C_0 , C_1 , $\overline{C_0}$, $\overline{C_1}$, Y_0 , Y_1 , Y_2 , Y_3 , and Y_4 have wavelengths λ_{C_0} , λ_{C_1} , λ_5 , λ_6 , λ_0 , λ_1 , λ_2 , λ_3 , and λ_4 , respectively. To get desired logical functions, power, wavelength detuning, and polarization of C_0 , C_1 , $\overline{C_0}$, $\overline{C_1}$, and Y_4 are controlled properly by tuning the corresponding bias current, temperature, and polarization controller in such a way that, in the case of output Y_0 , the SMFP-LD0 is fully locked when either C_0 or C_1 is logic "1". Under such condition, the SMFP-LD0 is also locked when both C_0 and C_1 are logic "1". In general, the self-locking mode of SMFP-LD0 (at λ_0) is suppressed when (C_0, C_1) is (0,1), (1,0), or (1,1) and not suppressed when both C_0 and C_1 are logic "0". Hence, the output Y_0 has a logic function of NOR gate. In the case of output Y_1 , the self-locking mode of SMFP-LD1 (at λ_1) is suppressed when $(C_0, \overline{C_1})$ is (0,1), (1,0), or (1,1) and not suppressed when $(C_0, \overline{C_1})$ is (0,0). When C_1 is logic "1", the SMFP-LD6 is fully locked and there is logic "0" at output Y_6 ($\overline{C_1}$ at wavelength λ_6). In other words, Y_1 is logic "0" when (C_0, C_1) is (0,0), (1,1), or (1,0) and is logic "1" when (Y_5, C_1) is (0,1), (1,0), or (1,1) and is logic "1" when (C_0, C_1) is (0,0). In other words, Y_2 is logic "0" when (C_0, C_1) is (0,1), (1,0), or (1,1) and is logic "1" when (C_0, C_1) is (1,0). In

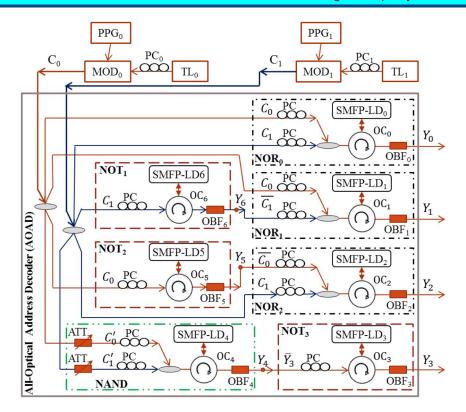


Fig. 3. Experimental setup of a 2×4 AOAD where, TL: Tunable Laser, OBF: Optical Bandpass Filter, PC: Polarization Controller, OC: Optical Circulator, MOD: Modulator, PPG: Pulse Pattern Generator, ATT: Optical Attenuator.

the case of output Y_3 , the power of C_0 , C_1 , and Y_4 are adjusted so that the SMFP-LD₃ is not suppressed when (C_0, C_1) is (0,0), (0,1), or (1,0) (the power of single-input beam is not enough to lock the SMFP-LD₃), and the SMFP-LD₃ is fully locked when (C_0, C_1) is (1,1) (multi-input injection-locking). In other words, Y_4 is logic "0" when only (C_0, C_1) is (1,1) and is logic "1" for all other three cases (NAND gate). Hence, Y_3 is logic "1" only when (C_0, C_1) is (1,1) and logic "0" when (C_0, C_1) is (0,0), (0,1), or (1,0) (AND gate). Finally, the AOAD is realized under the principle of single-input and multi-input injection-locking properties of SMFP-LD. All the logic functions are verified to match with the truth table in Table 1.

3. Experimental Setup and Results

Fig. 3 shows the experimental setup for AOAD using injection-locking property of SMFP-LD. The threshold current, working current, and working temperature of SMFP-LD $_0$ to SMFP-LD $_6$ are (9 mA, 12 mA, 13.9 °C), (11 mA, 15 mA, 26.3 °C), (11 mA, 15 mA, 26.3 °C), (9 mA, 12 mA, 13.9 °C), (11 mA, 15 mA, 26.3 °C), (13 mA, 19 mA, 13.5 °C), and (12 mA, 16 mA, 13.5 °C), respectively. Under those working conditions, SMFP-LDs have the dominant modes at λ_0 (1543.44 nm), λ_1 (1538.76 nm), λ_2 (1538.76 nm), λ_3 (1543.44 nm), λ_4 (1538.76 nm), λ_5 (1548.00 nm), and λ_6 (1544.52 nm), respectively. Two input light beams from TL $_0$ and TL $_1$ are set at the wavelengths of λ_{C_0} (1550.48 nm) and λ_{C_1} (1552.80 nm). The polarization controllers PC $_0$ and PC $_1$ were used to minimize the polarization-dependent loss in the Mach–Zehnder modulator, whereas other PCs are used to get maximum possible TE optical power injected into SMFP-LDs. Due to injection-locking property of FP-LD, the more TE power is injected into the SMFP-LD, the more suppression of the SMFP-LD's side modes and the higher power at the injected mode. With TM input beams, FP-LD shows absorption phenomena that can be used for the demonstration of the positive logic units such as AND, OR, and others [10]. Optical bandpass filters (OBFs) are used to pass only desired output wavelengths at

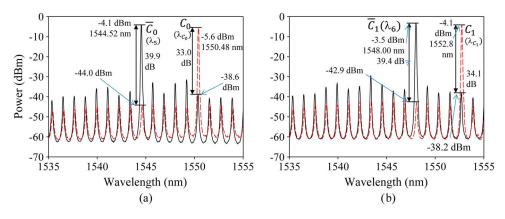


Fig. 4. Output spectra of the NOT₁ (SMFP-LD₆) and NOT₂ (SMFP-LD₅) gates of the AOAD.

the outputs. SMFP-LD $_0$ to SMFP-LD $_3$ and SMFP-LD $_5$ to SMFP-LD $_6$ work under the principle of single-input injection-locking, in which power of single-input beam is enough to suppress the dominant mode of SMFP-LD; however, SMFP-LD $_4$ works on multi-input injection-locking, in which power of single-input beam is not enough to suppress the dominant mode, i.e., two input beams are required for the SMFP-LD $_4$. The input light beams are modulated with 10-Gb/s non-return-to-zero pseudorandom bit sequences of $2^{31}-1$ that are generated from an Anritsu MP1763B pulse pattern generator.

To know the dependency of required injected power to fully lock (P_{FL}) an SMFP-LD and to release (P_{RL}), the SMFP-LD's locking state at given wavelength detuning, one side mode was selected and the input wavelength was tuned around the chosen side mode, as shown in Fig. 2. In this figure, the negative wavelength detuning corresponds to the case input wavelength that is smaller than the side mode wavelength. We found that the required powers to fully lock the SMFP-LD and to release its locking state in the experiments are about -7.5 and -9.3, respectively, given that the wavelength detuning is about 0.04 nm to 0.08 nm (their were not significantly different in required powers to lock and to release the SMFP-LD in the experiment).

Fig. 4 shows the spectra of the SMFP-LD₅ (λ_5) (a) and SMFP-LD₆ (λ_6) (b), which work as the NOT gates with the single-input C_0 and C_1 , respectively. Chosen side modes' wavelengths are 1550.44 and 1552.72 nm, which are corresponding to the wavelength detunings of 0.04 and 0.08 nm. The measured powers of inputs C_0 and C_1 before the circulators OC_5 and OC_6 are -4.9 and -5.1 dBm, respectively, which are greater than the required power (-7.5 dBm) to fully lock the corresponding SMFP-LDs. When C_0 is logic "0" (-38.6 dBm, black solid line), output $\overline{C_0}$ is logic "1" (-4.1), and when C_0 is logic "1" (-5.6 dBm, measured by OSA, red dash line), output λ_6 ($\overline{C_0}$) is logic "0" (-44 dBm). Similarly, when C_1 is logic "0" (-38.2 dBm, black solid line), output $\overline{C_1}$ is logic "1"(-3.5 dBm), and when C_1 is logic "1" (-4.1 dBm, red dash line), output λ_5 ($\overline{C_1}$) is logic "0" (-42.9 dBm).

Fig. 5 shows the output spectra of the SMFP-LD₀, Y_0 before the filter OBF₀ when (C_0, C_1) is (a) (0,0); (b) (0,1); (c) (1,0); and (d) (1,1), respectively. The chosen side modes' wavelengths are 1550.44 and 1552.76 nm, which are corresponding to wavelength detunings of 0.04 and 0.04 nm. Because powers of inputs C_0 and C_1 at logic "1", measured before OC₁, are -4.9 and -5.1 dBm, respectively, either power of C_0 or C_1 is enough to fully lock the SMFP-LD₀ when C_0 or C_1 is logic "1", and the locking state is released when both of them are logic "0". Indeed, when both C_0 and C_1 are logic "0", there is no input beam injected into the SMFP-LD₀ and the only spectrum of the SMFP-LD₀ is observed at output Y_0 , as shown in Fig. 5(a). Hence, the self-locked mode at wavelength λ_0 (1543.44 nm) is not suppressed or, in other words, Y_0 has logic high (logic "1") in this case. When C_0 is logic "0" and C_1 logic "1", the power of input beam C_1 is enough to lock the SMFP-LD₀, as shown in Fig. 5(b) (solid black). The contrast ratio (CR) is about 38.3 dB compared between with and without input C_1 to the SMFP-LD. Similarly, the SMFP-LD is fully locked with a

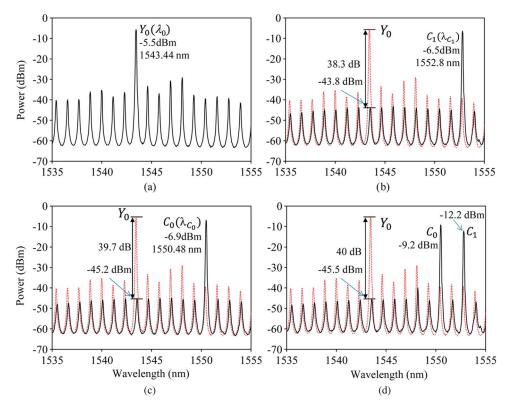


Fig. 5. Output spectra at the output port Y_0 of the AOAD in cases (C_0, C_1, Y_0) are (a) (0,0,1), (b) (0,1,0), (c) (1,0,0), and (d) (1,1,0), respectively.

CR of about 29.7 and 40 dB when (C_0, C_1) is (1,0) and (1,1), respectively. In conclusion, the output Y_0 is logic "1" only when (C_0, C_1) is (0,0).

In the case of output Y_1 , since the SMFP-LD₆ is used as the NOT₁ gate to invert the input signal C_1 , required inputs' logic states are changed, as compared with the case output Y_0 , to get the output Y_1 to be logic "1". Indeed, Fig. 6 shows the spectra before filters OBF₁ (black solid line) and OBF₆ (red dot line) when (C_0, C_1) is (a) (0,0); (b) (0,1); (c) (1,0); and (d) (1,1), respectively, and the spectrum of the SMFP-LD₁ without any injection (black dot line). The chosen side modes' wavelengths with respect to the inputs C_0 and $\overline{C_1}$ are 1547.96 and 1550.40 nm, which are corresponding to wavelength detunings of 0.04 and 0.08 nm, respectively. The powers of inputs C_0 and $\overline{C_1}$ measured before OC₁ are -4.9 and -5.2 dBm, respectively. Hence, all the modes of SMFP-LD₁ are fully suppressed when either C_0 or $\overline{C_1}$ is logic "1", and the locking state of SMFP-LD₁ is released only when both C_0 and $\overline{C_1}$ are logic "0". Fig. 6(a) shows that when both C_0 and C₁ are logic "0", there is no input beam injected into the SMFP-LD₆ and the self-locked mode of the SMFP-LD₆ is not suppressed; hence, C₁ is logic "1", which causes SMFP-LD₁ to be locked fully at wavelength λ_6 . Therefore, Y_1 is logic "0". The power of the side mode at λ_2 (1538.76 nm) is about -37.5 dBm, and the CR is about 30.9 dB. When C_0 is logic "0" and C_1 is logic "1" [see Fig. 6(b)], the SMFP-LD₅ is locked by C_1 ; therefore, $\overline{C_1}$ is logic "0". The self-locked mode at wavelength λ_2 (1538.76 nm) is not suppressed or, in other words, Y_1 is logic "1". When C_0 is logic "1" and C_1 is logic "0" [see Fig. 6(c)], the SMFP-LD₆ is not locked by the input C_1 ; therefore, $\overline{C_1}$ is logic "1". Hence, the SMFP-LD₁ is locked by both inputs C_0 and $\overline{C_1}$, which cause the output Y_1 to be logic "0". The CR is about 34.2 dB compared to SMFP-LD₁ when there is no input. In case (C_0, C_1) is (1,1), the SMFP-LD₅ is fully locked by the input C_1 , which causes the output $\overline{C_1}$ to be logic "0"; therefore, the SMFP-LD₂ is injection-locked by only input C_0 and the output Y_1 is logic "0" with a CR of about 34.3 dB. In conclusion, the output Y_1 is at logic high with only one case (C_0, C_1) is (0,1).

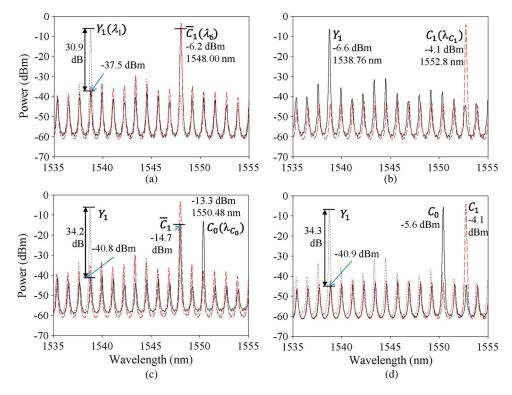


Fig. 6. Output spectra at the output port Y_1 of the AOAD in cases (C_0, C_1, Y_1) are (a) (0,0,0), (b) (0,1,1), (c) (1,0,0), and (d) (1,1,0), respectively.

In the case of output Y_2 , the SMFP-LD₅ is used as a NOT₂ gate to invert the input signal C_0 (1550.48 nm). Fig. 7 shows the spectra before OBF₂ (black solid line), the spectra before the filter at output $\overline{C_0}$ (1544.52 nm) of the SMFP-LD₅ (red dot line) when (C_0, C_1) is (a) (0,0); (b) (0,1); (c) (1,0); and (d) (1,1), respectively, and the spectrum of the SMFP-LD₂ without any injection (black dot line). Powers of inputs $\overline{C_0}$ and C_1 measured before OC₃, when $\overline{C_0}$ and C_1 are logic "1", are -4.8 and -5.1 dBm, respectively. Due to the similarity between this part and the previous Y_0 and Y_1 parts, we just show some specific values that belong to this part. The chosen side modes' wavelengths are 1544.44 and 1550.40 nm, which are corresponding to wavelength detunings of 0.08 and 0.08 nm. The output Y_2 is logic high only when $(\overline{C_0}, C_1)$ is (0,0) or (C_0, C_1) is (1,0), in other words. In other cases of inputs (C_0, C_1) ((a) (0,0), (b) (0,1), and (d) (1,1)), the outputs of Y_2 are logic low because the SMFP-LD₂ is locked by $\overline{C_0}$ or/and C_1 . CRs are about 27.0, 40.6, and 40.5 dB in the cases of (0,0), (0,1), and (1,1), respectively.

Fig. 8 shows the spectra before the filter OBF₃ (black solid line), the spectra before the filter OBF₄ (red dash line) when (C_0, C_1) is (a) (0,0); (b) (0,1); (c) (1,0); and (d) (1,1), respectively, and the spectrum of the SMFP-LD₃ without any injection (black dot line). The chosen side modes of the SMFP-LD₄ have wavelengths 1550.44 and 1552.76 nm and wavelength detunings are 0.04 and 0.04 nm, respectively. Powers of inputs C_0 and C_1 are attenuated to about -10.1 dBm (C_0') and -10.3 dBm (C_1') , respectively, by using optical attenuators, which are lower than the released power (-9.6 dBm) and are not enough to lock the SMFP-LD₄ $(\lambda_4 = 1543.44)$. Only one input C_0' or C_1' cannot lock the SMFP-LD₄; however, the total power of C_0' and C_1' , about -7.2 dBm, is enough to fully lock the SMFP-LD₄. Further, the output power of the SMFP-LD₄ measured at Y_4 is about -6.9 dBm (enough to fully lock the SMFP-LD₃) corresponding to the side mode wavelength of SMFP-LD₃ that is 1543.40 nm (0.04-nm wavelength detuning) in case (C_0, C_1) is (0,0), (0,1), and (1,0), respectively, and is less than -40 dBm (not enough to fully lock the SMFP-LD₃) in case (C_0, C_1) is (1,1). Fig. 8(a) shows that when both C_0 and C_1 are logic "0", there is no input beam

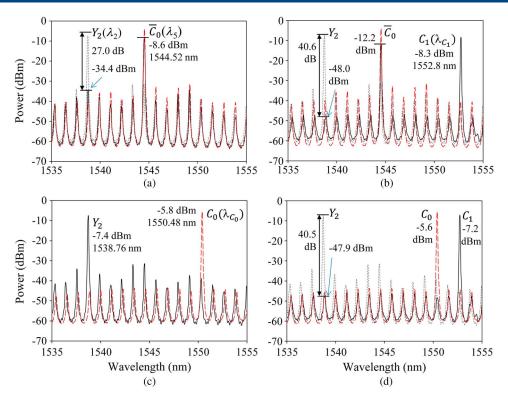


Fig. 7. Output spectra at the output port Y_2 of the AOAD in cases (C_0, C_1, Y_2) are (a) (0,0,0), (b) (0,1,0), (c) (1,0,1), and (d) (1,1,0), respectively.

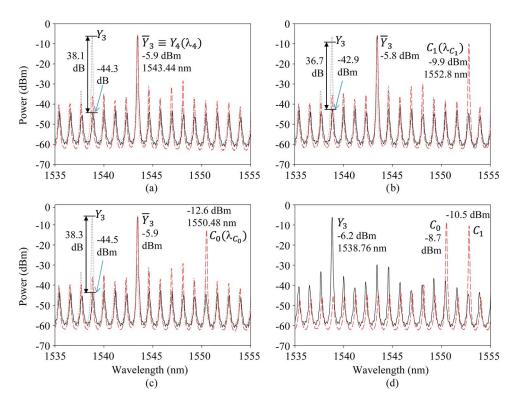


Fig. 8. Output spectra at the output port Y_3 of the AOAD in cases (C_0, C_1, Y_3) are (a) (0,0,0), (b) (0,1,0), (c) (1,0,0), and (d) (1,1,1), respectively.

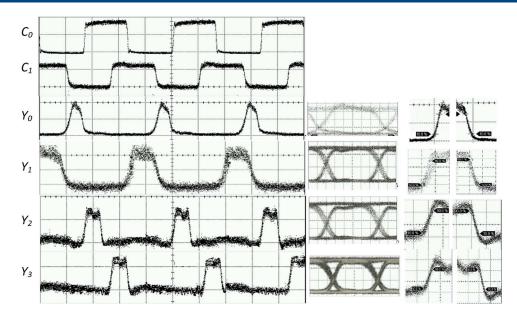


Fig. 9. Waveforms, eyes diagrams and rising/falling edges of the AOAD at output ports Y_0 , Y_1 , Y_2 Y_3 ; measured with the time scale of 500 ps/div, 20 ps/div and, 100 ps/div respectively.

injected into the SMFP-LD₄ and the self-locked mode of the SMFP-LD₄ is not suppressed; hence, Y_4 (at λ_4 1543.44 nm) is logic "1", which causes SMFP-LD₃ to be fully locked at wavelength λ_4 . Therefore, Y_3 is logic "0". The power of the side mode at λ_3 (1538.8 nm) is about -44.3 dBm, and the CR is about 38.1 dB.

When (C_0, C_1) is (0,1) and (1,0) [see Fig. 8(b) and (c)], the SMFP-LD₄ is not locked or the self-locked mode at wavelength λ_4 is not suppressed; in other words, the powers of C_0 and C_1 are adjusted in such a way that single input power is not enough to lock the SMFP-LD₄. Hence, the SMFP-LD₃ is locked by Y_4 (considered as $\overline{Y_3}$), which causes the output Y_3 to be logic "0". The CRs are about 36.7 and 38.3 dB, respectively, compared to SMFP-LD₃ when there is no input. In case (C_0, C_1) is (1,1) in Fig. 8(d), the SMFP-LD₄ is locked by the combined powers of both C_0 and C_1 , which results in logic "0" at output Y_4 . Hence, the SMFP-LD₃ is not locked and Y_3 is logic "1". In conclusion, the output Y_3 is logic "1" with only the case (C_0, C_1) is (1,1). In conclusion, the proposed AOAD using the injection-locking property of SMFP-LD is successfully verified in the spectrum domain for all the cases of inputs (C_0, C_1) .

Fig. 9 shows the output waveforms, eyes diagrams, and rising–falling times at the corresponding outputs of the AOAD. Two input data (C_0 and C_1) were modulated with 16-bit NRZ signals at 10 Gb/s. The PRBS signal length was $2^{31}-1$. From the output waveforms, we can see that Y_0 has logic "1" only when both inputs are at logic "0", Y_1 has logic "1" only when $C_0=0$ and $C_1=1$, Y_2 is logic "1" only when $C_0=1$ and $C_1=1$. For all other conditions, the corresponding outputs are logic "0", which are matched with the results in the spectrum domain and prove the logic function of the 2×4 AOAD. The extinction ratios of outputs' eyes diagrams measured at ports Y_0 , Y_1 , Y_2 , and Y_3 are 10.94, 12.12, 10.8, and 10.68 dB, and the corresponding rising–falling times of outputs' waveforms are about (45,46), (47,43), (43,49), and (47,47) ps. The waveforms of all cases are clear enough to have good BER, as shown in Fig. 10.

Fig. 10 shows the BER measurements of AOAD. All the outputs have no noise floor up to BER of 10^{-12} at the data rate of 10 Gb/s. The highest BER power penalty is measured about 1.64 dB for output port Y_2 . The little difference in power penalty between different outputs of the decoder may come from the differences in polarization controller and nonidentical wavelength detuning.

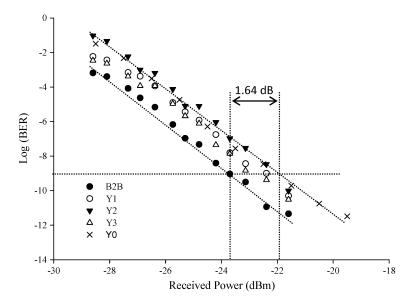


Fig. 10. BER and power penalty measurements for the AOAD.

4. Discussion and Conclusion

The key issues with the implementation of AOAD are single-input and multi-input injection-locking properties of SMFP-LDs and the cascading of different logic gates to form the desired functional device. Hence, proper power management and wavelength detuning should be considered carefully. Since injection locking is dependent on wavelength detuning, wavelength matching is considered as one of the critical parameters. However, this can be overcome with the management of input beam powers that are injected to respective SMFP-LDs. Since SMFP-LDs are used, external probe beams are not required as needed in conventional FP-LDs and SOAs. In addition, the maximum bias current for the SMFP-LDs that we have used is below 19 mA, which is low compared with that of other optical technologies.

In this paper, we have proposed and experimentally demonstrated an AOAD using an SMFP-LD. The decoder has clear spectra, waveform, eyes diagram, reasonable rising–falling time, and BER for all the outputs. The output spectra and waveforms satisfy the desired logic functions of an address decoder, as shown in the truth table in Table 1. Since SMFP-LD is made from cheap commercial FP-LD, which requires small bias current, and the scheme using SMFP-LD does not require additional probe beam and associated components to have injection locking, the proposed scheme is power and cost efficient and has simple configuration features compared with other technologies, including commercially available FP-LD technology. The experiment is carried out with a data rate of 10 Gb/s; however, the speed can be increased to a higher data rate [11]. The proposed AOAD can be used for all-optical control unit, all-optical address decoding, label swapping based on the time-to-wavelength converter [12], and other signal processing. Since several components such as optical waveguide [13], polarization controller [14], circulator [15], coupler [16], [17], and tunable filter [18] have been successfully integrated as reported in respective references [13]–[18], the AOAD can be integrated after finding the proper solution for SMFP-LD integration, which we are considering in near future works.

Acknowledgment

The authors are deeply thankful to all interested persons at MKE and the Korea Evaluation Institute of Industrial Technology (KEIT).

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