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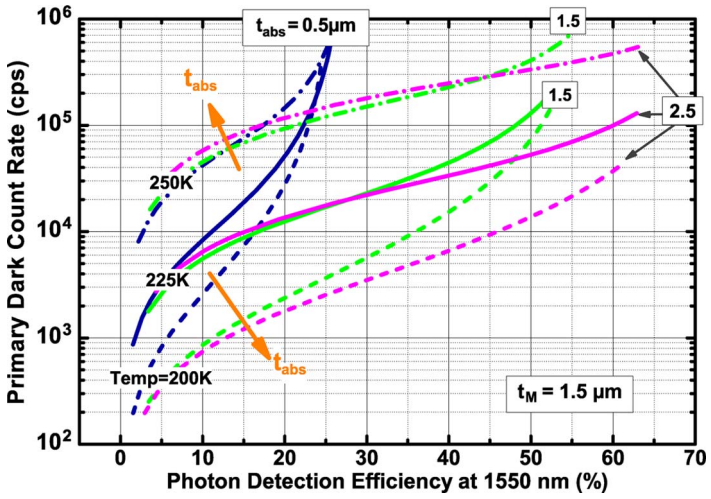


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# Design Criteria for InGaAs/InP Single-Photon Avalanche Diode

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**Abstract:** We provide a detailed insight on the design of InGaAs/InP single-photon avalanche diode (SPAD) for 1.55-$\mu$m photon detection. In order to lower SPAD noise [the dark count rate (DCR)] without lowering photon detection efficiency (PDE) or increasing afterpulsing, it is important to optimize detector vertical layer structure and diffusion profiles. We present simulations of SPAD structures with different models, including custom ones. We discuss the influences of multiplication region thickness and doping, absorption region thickness, and electric-field distribution on SPAD performance. Multiplication region thickness strongly affects tunneling generation, whereas a thicker absorption region gives higher absorption efficiency but reduces trigger efficiency. Their optimal values depend on InP and InGaAs material quality and on device operating conditions. We show how electric field within InGaAs must be chosen as a tradeoff between heterobarrier transit efficiency and carrier generation.

**Index Terms:** Avalanche photodiodes, dark count, detection efficiency, InGaAs, single-photon avalanche diode (SPAD), performance simulation, photon counting.

## 1. Introduction

Single-photon detectors for the near-infrared wavelength region, such as photomultiplier tubes (PMTs), superconducting single-photon detectors (SSPDs), single-photon avalanche diodes (SPADs), etc., are receiving increasing interest in a growing number of photon counting applications, including, for example, 3-D laser ranging (LIDAR) [1], quantum cryptography [2], optical VLSI circuit inspection [3], time-resolved spectroscopy [4], etc. SPADs have the distinctive advantages of solid-state detectors (small size, low bias, low power consumption, and reliability) and are frequently the best choice for applications that require high detection efficiency, very good time resolution, and ease of operation [5], [6]. $In_{0.53}Ga_{0.47}As$/InP SPADs are used for single-photon counting and photon timing [also known as time-correlated single-photon counting (TCSPC)], typically at 1550 nm, and they can efficiently detect photon even up to 1700 nm [7].

A SPAD is a p-n junction operated in the so-called Geiger mode: the avalanche photodiode is biased above breakdown, operating in a metastable state where the generation of an electron–hole pair causes the diode to break down, producing a fast current rise (limited by series resistance and internal space-charge effects) that has to be quenched by front-end electronics [8]. In order to improve SPAD performance, i.e., to reduce both dark count rate (DCR) and afterpulsing without impairing photon detection efficiency (PDE), it is important to optimize detector's vertical layer structure, to properly tailor doping and depths of diffusions, and to operate the SPAD in proper electrical and thermal conditions.

In this paper, we analyze the vertical structure of an InGaAs/InP SPAD, for 1.55-$\mu$m photon detection. Although its structure is similar to InGaAsP/InP SPAD for 1.06-$\mu$m photon detection,

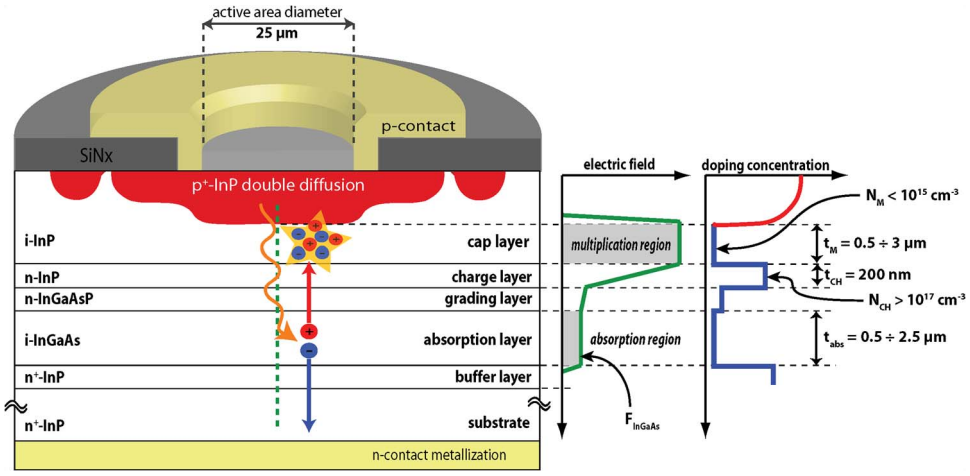


Fig. 1. Internal structure of a front-illuminated planar InGaAs/InP SPAD, with double diffusion and floating guard ring (FGR). The doping profile and the electric field along the center of the active area are also shown.

where tunneling dominates DCR over almost all operating conditions [9], thermal generation in InGaAs/InP SPAD is significantly higher, giving different trends at the same temperatures, hence requiring different design choices. We simulate and analyze the influence of multiplication region thickness and doping, absorption layer thickness, and electric-field distribution.

## 2. InGaAs/InP SPAD Structure and Performance

Typically, planar front-illuminated InGaAs/InP SPADs have a separate absorption, grading, charge, and multiplication (SAGCM) heterostructure, as shown in Fig. 1. The electron–hole pair photogenerated in the $In_{0.53}Ga_{0.47}As$ layer ($E_G \sim 0.75$ eV at 300 K) region is separated by the electric field: the hole is drifted to the InP multiplication region ($E_G \sim 1.35$ eV at 300 K), where it can trigger a self-sustaining avalanche. Between absorption and multiplication regions, a charge layer causes a drop in the electric field, thus keeping it high only in the multiplication region, and an InGaAsP layer (or few graded layers) avoids hole pile-up at the InGaAs–InP heterointerface. A double p-type diffusion, made by both deep (smaller diameter) and shallow (larger diameter) Zn diffusions [10], confines the high field region and reduces edge effects. InGaAs/InP SPADs and APDs have similar layers structure, but there are important differences in design criteria: i) SPADs are designed to operate above breakdown voltage and at relatively low temperature (even below 230 K); thus, electric-field profile must be tailored for such conditions. ii) The positive feedback of the above-breakdown avalanche process is not a drawback for SPADs, since it is the fundamental condition for SPAD operation. iii) Peripheral leakage (which contribute to dark current and is an important noise source in an APD) does not get multiplied, and it does not trigger any self-sustaining avalanche process; hence, it does not contribute to SPAD DCR.

It is possible to identify some key parameters that mainly affect InGaAs/InP SPAD performance: i) multiplication region thickness (that impacts tunneling generation and electric-field uniformity in the active area [11]); ii) multiplication region doping; iii) absorption region thickness; iv) electric field in the absorption region; v) difference between shallow and deep diffusion depths; and vi) quaternary layer composition (for optimizing photon-timing performance).

Four independent parameters must be optimized during detector design: a) PDE; b) DCR; c) minimum hold-off time ($T_H$); d) photon-timing jitter. PDE is given by the product of: i) absorption probability; ii) transit probability (i.e., the probability that the photogenerated hole successfully crosses the heterobarrier and reaches the multiplication region); iii) self-sustaining avalanche trigger probability. DCR is the rate of "false" avalanche ignitions, caused by carrier generation due to thermal and tunneling processes. The minimum hold-off time is the time interval during which the detector has to be kept OFF after each avalanche ignition, in order to limit the afterpulsing effect: in

InGaAs/InP SPADs, due to the relatively long afterpulsing time constants, it is of the order of some or tens of microseconds [6]. Photon-timing jitter is the time spread between photon absorption and avalanche pulse detection by the front-end electronics: it depends both on readout circuitry [12] and on SPAD design, mainly on the electric-field shape [11]. We simulated the performance of a 25 $\mu$m InGaAs/InP SPAD, with typical thicknesses and doping levels shown in Fig. 1.

## 3. Models

We developed a custom "SPAD simulator" [13], which integrates several models (either custom made or taken from literature) for avalanche build-up, thermal and tunneling generation, photon absorption, afterpulsing, and so on, in order to be able to properly estimate main performance parameters (not just the electrical ones) of InGaAs/InP SPAD. We performed mono-dimensional simulations on the SPAD structure, along the device's central axis.

Many SPAD parameters depend on breakdown voltage, which can be properly estimated once a correct model for ionization coefficients is employed. Among various formulations reported in literature [14]–[17], we employed those by Okuto and Crowell [18], including temperature dependence [19], with parameters reported in [17]. These models proved to fit well, down to 150 K, the breakdown voltage of both test structures and SPAD devices [7] that we fabricated, with a minor mismatch of about 1 V. For computing avalanche triggering probability $PA(x)$, we employed the model by Oldham *et al.* [20], and we computed it at every point $(x)$ along the SPAD's central axis, although for the quaternary and the absorption regions, we considered it constant, i.e., equal to $PA(0)$. We included also carrier generated inside neutral regions but just up to at a distance from the depleted region closer than the diffusion length.

In the PDE calculation, we neglected the reflection at the air–semiconductor interface and any effect of AR coating. The wavelength-dependent and temperature-dependent absorption coefficient for InGaAs was calculated with the model by Zielinski *et al.* [21], whereas for InP, that of Adachi [22]. Since we considered a front-illuminated structure, we did not take into account the influence of substrate, and we neglected the reflection at the cathode metallization.

Concerning noise, three different carrier generation mechanisms were taken into account: thermal generation, band-to-band (direct) tunneling, and trap-assisted tunneling (TAT). Other effects like Poole–Frenkel and phonon-assisted tunneling through defect [23], [24] were neglected for simplicity. Thermal generation is mainly determined by Shockley–Read–Hall (SRH) processes, and we considered an unique dominant deep level. Moreover, following Donnelly *et al.* [25], we employed an effective lifetime $\tau_{eff}$ independent of electric field and temperature, which instead play a role in energy-gap and intrinsic concentration $(n_i)$ values. Thermal generation can be written as $n_i/\tau_{eff}$. The effective lifetime was estimated as a fitting parameter in [9] and [25] data for InGaAsP/InP SPADs, and its value was 70 $\mu$s and 40 $\mu$s, respectively, for the two data sets. Since this parameter is an important signature of material quality (particularly for InGaAs), we fitted primary DCR of different SPAD structures (see [7]), and from our data-set, we extracted values from 2 $\mu$s to 60 $\mu$s; in the following, we chose 50 $\mu$s. For band-to-band tunneling, we employed the formulations reported in [25] and [27], and for TAT the model reported in [25], which uses two fitting parameters, i.e., the trap position inside the energy gap ($a \cdot E_G$, where $a$ is the ratio between trap energy level and energy gap, $E_G$) and the concentration of traps $(N_T)$. As obtained by fitting in [25] and as employed in [9], [24], and [26], we considered one trapping center at $0.75 \cdot E_G$ for InP. This was in accordance to the fitting of primary DCR that we measured on several SPAD structures, which resulted in values ranging from $0.7 \cdot E_G$ to $0.85 \cdot E_G$.

Finally, concerning afterpulsing probability, we employed our own custom model, described in [28], which takes into account different trap families, each one with its capture and release time constant (whose temperature dependence is given by the activation energy) and its concentration inside the multiplication region. These values were obtained by fitting afterpulsing probability curves of commercially available InGaAs/InP SPADs [29], measured at different temperatures with the "double-pulse" method described in [30]; we obtained 4 trap families with release time constants from 0.02 $\mu$s to 2.4 $\mu$s (at 300 K) and activation energies from 0.2 to 0.28 eV.

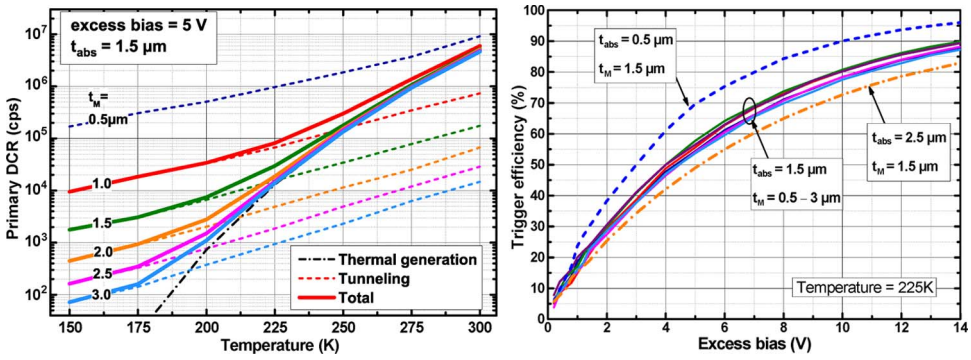


Fig. 2. Estimated primary DCR as a function of temperature, for different multiplication region thicknesses (left) and trigger efficiency as a function of excess bias, for SPAD with different multiplication and absorption region thicknesses (right).

## 4. Considerations on the Multiplication Region

Multiplication region thickness is a very important parameter. We simulated electric field, breakdown voltage, and primary DCR of some SPAD structures with same structure but changing the multiplication region thickness $(t_M)$. We changed the charge layer doping in order to keep the same electric field in both quaternary and absorption regions, thus keeping constant the other contributions to DCR due to the InGaAs region. Fig. 1 shows the typical electric-field profile in the central axis; in the following, the "peak electric field" refers to the maximum field inside the multiplication region.

Breakdown voltage increases linearly with the multiplication region thickness, being 48 V, 88 V, 125 V, and 144 V (at 300 K) when $t_M$ is 0.5 $\mu$m, 1.5 $\mu$m, 2.5 $\mu$m, and 3.0 $\mu$m, respectively. Instead, the peak electric field (at breakdown) decreases with $t_M$ and has stronger dependence at lower thickness, being 518 kV/cm when $t_M$ is 0.5 $\mu$m, 451 kV/cm at 1.5 $\mu$m, and 427 kV/cm when $t_M$ is 2.5 $\mu$m. Its slope can be fitted approximately with $t_M^{-0.117}$.

Concerning primary DCR, its temperature dependence usually gives an indication of the dominant carrier generation contribution: high slope means dominant thermal generation, while low slope means dominant tunneling generation processes [11]. Fig. 2 (left) shows the estimated primary DCR at 5-V excess bias. In these simulations, we took into account all contributions (thermal generation, direct tunneling, and TAT) from InP, InGaAsP, and InGaAs. Results confirm that the dominant ones are: i) thermal generation from InGaAs absorption region and ii) TAT in InP multiplication region. The latter is the dominant contribution at low temperatures and is strongly dependent on multiplication region thickness; DCR lowers by almost 3 decades when $t_M$ increases from 0.5 $\mu$m to 2.5 $\mu$m. As for the peak electric-field value, the dependence is stronger with lower thickness values. Conversely, thermal generation in InGaAs has almost no variation: it is dominant at temperatures higher than 230 K (for a thickness larger than 1.5 $\mu$m). Therefore, the total DCR decreases with $t_M$, but it reaches a lower limit given by the thermal generation contribution, which however has a high slope and decreases of about 1 decade every 25 K. Only at temperatures lower than about 200 K, thermal generation is no longer dominant.

Concerning the DCR dependence on excess bias $(V_{EX})$, tunneling generation has a marked bias dependence (it increases of about one order of magnitude when $V_{EX}$ grows from 1 V to 5 V and two orders when $V_{EX}$ reaches 13 V) and distinctly decreases when $t_M$ is increased. Conversely, thermal generation (considering SRH model) shows lower dependence (less than one order of magnitude between 1 V and 13 V of $V_{EX}$) and does not change with thickness. Therefore, at 225 K, in a thick multiplication region SPAD, thermal generation is the main contribution and there is weak dependence on excess bias, whereas with thin multiplication region, TAT is greater and DCR significantly increases with $V_{EX}$. Since PDE has almost a fixed dependence on bias, when DCR slope is low, higher excess bias gives higher efficiency without increasing DCR too much.

It is important to note that thermal and tunneling contributions strongly depend on InGaAs and InP quality, in terms of deep-level (i.e., traps) concentrations, which can change between one

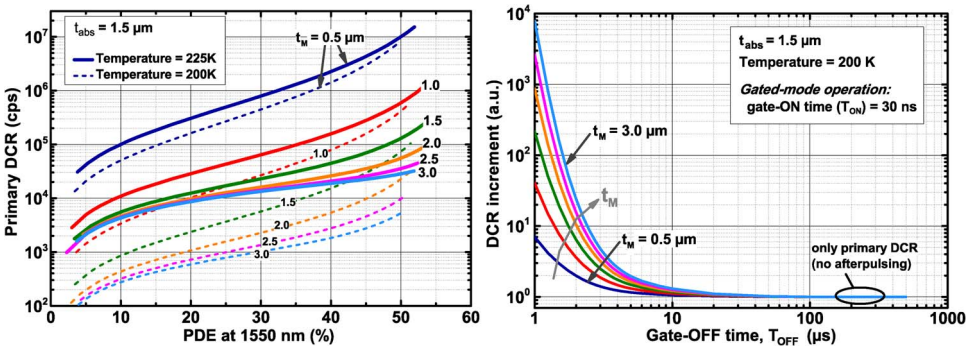


Fig. 3. Primary DCR as a function of PDE at 1550 nm, for SPADs with different multiplication region thickness, at 225 K and 200 K (left) and estimated DCR dependence on gate-OFF time (SPAD operated in gated mode, at 200 K, with a gate-ON time of 30 ns) (right).

production run to another and from one fabrication process to another. Therefore, even though trends and considerations here reported are always valid, the actual cross-point values of excess bias and temperature can slightly differ.

Regarding PDE, the variation of multiplication region thickness has a minor effect on absorption efficiency and on avalanche trigger efficiency: as shown in Fig. 2 (right), despite the large breakdown voltage variation with multiplication region thickness, there is only a low dependence of trigger efficiency on $t_M$ (with a maximum at 1.5 $\mu$m). Conversely, variations in absorption region thickness have a greater effect on trigger efficiency, as discussed in Section 6. Hence, as shown in Fig. 3 (left), when a PDE of 20 $\div$ 30% is needed (at 1550 nm), primary DCR reduces as multiplication region thickness increases, reaching a lower limit (of about $10^4$ cps at 225 K, given by thermal generation) at about $t_M = 2$ $\mu$m. At lower temperatures (200 K), such limit is much lower and DCR reduces to $10^3$ cps with $t_M = 3$ $\mu$m.

Therefore, as far as PDE and primary DCR are concerned, SPAD performance gets better with thicker multiplication region and lower operating temperatures. However, there are other aspects that should be considered: i) timing jitter of InGaAs/InP SPAD (i.e., photon-timing performance) significantly worsen as multiplication region thickness increases, due to increased spread in the avalanche build-up time (see [5]); ii) afterpulsing probability depends on the number of traps inside multiplication region, which depends linearly on $t_M$ for a given trap concentration; and iii) release time constants of traps considerably increase when temperature is lowered; thus, usually, the operating temperature is a tradeoff between primary DCR (as low as possible) and maximum count rate (limited by afterpulsing). We simulated SPAD afterpulsing with different multiplication region thickness, at 200 K, and estimated the DCR when SPAD is operated in gated mode with passive quenching, at different gate-OFF times and with 30-ns gate-ON time: during gate-ON time, any triggered avalanche is passively quenched by a series resistor, while during gate-OFF time, no avalanche can be ignited; hence, if there are populated traps, they can release carriers without creating an afterpulse. In such conditions, the DCR increment at short $T_{OFF}$ gives a rough estimation of afterpulsing probability and maximum gate frequency. As shown in Fig. 3 (right), by increasing the multiplication region thickness from 0.5 $\mu$m to 3.0 $\mu$m, afterpulsing (i.e., the number of traps) grows linearly, and the maximum gate frequency reduces by a factor of about 4. Therefore, while primary DCR decreases, afterpulsing grows with $t_M$, thus reducing the SPAD maximum count rate.

Fig. 4 (left) shows the estimated DCR, when the SPAD is operated in gated mode with 5-V excess bias and 50-ns gate-ON time, as a function of temperature and gate-OFF times. With 500 $\mu$s, only primary DCR is present; conversely, by reducing $T_{OFF}$ (i.e., when increasing gate frequency), afterpulsing becomes evident at low temperature. For example, when operated at 10-$\mu$s and 5-$\mu$s gate-OFF times, SPAD should not be used at temperatures lower than about 200 K and 225 K, respectively. As an overview, Fig. 4 (right) represents level curves of DCR and afterpulsing probability as a function of temperature and gate-OFF time. Afterpulsing probability is computed as the probability to have an ignition due to afterpulsing in a subsequent gate-ON time slot, when an avalanche was

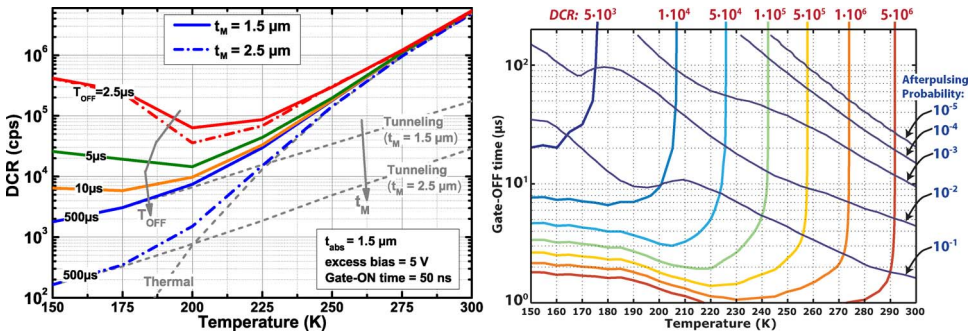


Fig. 4. DCR dependence on temperature, at different gate-OFF times ($T_{OFF}$), for $t_M$ of 1.5 $\mu$m and 2.5 $\mu$m (left) and level curves of DCR and afterpulsing probability, as a function of temperature and gate-OFF time estimated with a 50 ns gate-ON time, for a SPAD with $t_M = 1.5$ $\mu$m (right).

triggered in the previous gate-ON (one gate-OFF time before) [30]. For example, in order to keep afterpulsing probability lower than 10% and to have a count rate of at least 100 kcps, it is mandatory to operate the SPAD at temperatures higher than $\sim$220 K, which imply a minimum DCR of $1-5 \cdot 10^4$ cps.

In conclusion, the multiplication region thickness should be chosen as a tradeoff between primary DCR, afterpulsing probability, and timing jitter, considering the target SPAD operating conditions. In order to attain moderately low noise and sufficiently high count rate, we found that SPADs should be operated between 200 K and 230 K, where thermal generation is dominant for $t_M$ greater than 2 $\mu$m; a wider thickness gives no performance improvement but would impair timing jitter.

Another important parameter is the multiplication region doping; in InGaAs/InP SPADs, multiplication region (as well as absorption region) has a very low doping concentration. Indeed, higher doping levels give more peaked electric field in the multiplication region, thus causing stronger tunneling. However, the lowest doping level achievable depends on the fabrication process. In order to quantify the effect of a not-flat field profile, we estimated peak electric field (at breakdown) and DCR for doping levels between $1 \cdot 10^{15}$ cm$^{-3}$ and $9 \cdot 10^{15}$ cm$^{-3}$. As shown in Fig. 5 (left), the electric-field peak rises linearly (at 200 K and 225 K, trends are similar, so only one is shown), while DCR increases exponentially (particularly at low temperatures); at 200 K, it grows more than one order of magnitude, while at 225 K, the dependence is reduced, since DCR is limited by thermal generation.

## 5. Temperature Dependence of Detection Efficiency

As shown in Fig. 5 (right), the slope of PDE versus wavelength depends on temperature, due to: i) variations of absorption coefficients, mainly the InGaAs one, which reduces the cutoff wavelength of about 50 nm every 75 K decrease; and ii) breakdown voltage variations, which give different electric-field increments (thus trigger efficiency) at a given excess bias (as can be particularly noted in the 1000- to1200-nm range). The plot in the inlet shows the variation of absorption efficiency and of overall PDE at 1550 nm, as a function of temperature. While PDE drops at low temperatures due to the absorption efficiency decrease, at high temperature, it is almost flat because avalanche trigger probability reduces when temperature increases. In conclusion, the operating temperature can be decreased in order to reduce DCR but not below about 175 K for avoiding a marked PDE fall.

## 6. Considerations on Absorption Region

Concerning the absorption region, an important design parameter is the electric field, which depends on the overall charge within the charge layer. In previous works [24], it was reported that it is essential to minimize such a field, in order to reduce field-enhanced carrier generation, hence keeping absorption region barely depleted. However, transit efficiency at the heterobarrier (thus photon-timing jitter) strongly depends on the electric field within InGaAs and quaternary layers. Thus, electric field should be kept high to improve heterobarrier transit efficiency, though high electric field causes tunneling and field-enhanced thermal generation. Therefore, its value must be properly traded off.

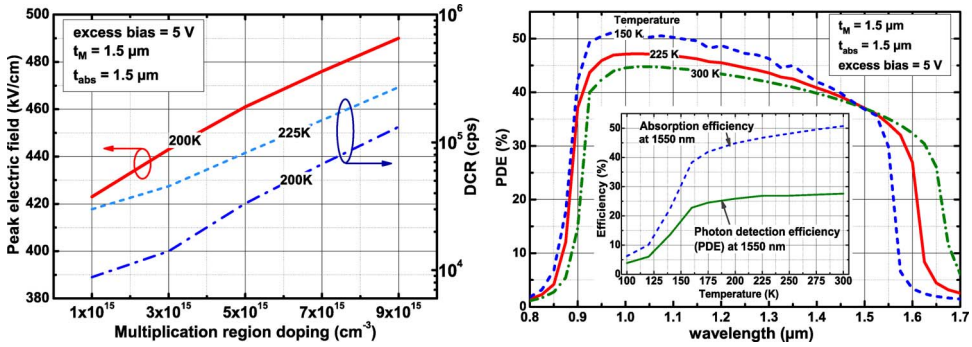


Fig. 5. (left) Peak electric field (at breakdown) and primary DCR for SPAD with different doping concentrations inside multiplication region; (right) Photon detection efficiency as a function of wavelength, at different temperatures.

Tunneling contributions depend on electric field and have little dependence on temperature, whereas thermal generation highly depends on temperature. Therefore, the electric field at which tunneling in InGaAs becomes important depends on temperature. Fig. 6 (left) shows an example, where simulated thermal generation and tunneling are reported at 225 K; here, the maximum allowable field value is about 140 kV/cm.

We investigated also the role of absorption region thickness, in the 0.5- to 2.5-$\mu$m range. Fig. 6 (right) reports the primary DCR for SPAD with a multiplication region thickness of 1.5 $\mu$m. At temperatures higher than 230 K, thermal generation is the dominant contribution and DCR increases with absorption layer thickness; with a given deep-level concentration in InGaAs, the generation rate is proportional to the depleted volume and thus to $t_{abs}$. Instead for trap-assisted tunneling (TAT), thickness lowers DCR since, by increasing $t_{abs}$, the breakdown voltage proportionally increases (of about 20 V moving from 0.5 $\mu$m to 2.5 $\mu$m) and electric field, as well as the trigger efficiency at a given excess bias, significantly decreases [as shown in Fig. 2 (right)]. Both electric field and trigger efficiency lowering contribute to reduce tunneling-generated DCR. However, lower triggering efficiency means also lower PDE, as discussed below.

Concerning the excess bias dependence of primary DCR, at low temperatures (200 K), tunneling is always dominant and DCR decreases with $t_{abs}$ (about fivefold from 1 V to 5 V of excess bias and tenfold with 13 V); conversely, at 250 K, thermal generation is dominant for excess bias lower than $\sim$8 V, while at 225 K, it is dominant at excess bias lower than $\sim$4 V. In this condition, DCR increases with $t_{abs}$. Thermal generation dependence on bias is lower than tunneling one; thus, at higher excess bias values, tunneling becomes dominant.

We also estimated the PDE as a function of wavelength, at different $t_{abs}$ values; as shown in Fig. 7 (left), when increasing $t_{abs}$, detection efficiency depends less on wavelength, giving more flat curves (since, at longer wavelengths, where absorption coefficient is lower, higher $t_{abs}$ gives higher absorption efficiency). Moreover, at short wavelength, PDE increases from $t_{abs} = 0.5$ $\mu$m to 1.5 $\mu$m and then decreases due to the lowering of trigger efficiency (at a constant excess bias). Therefore, absorption efficiency increases when $t_{abs}$ gets thicker (especially at longer wavelength), but trigger efficiency PA(0) reduces; thus, the expected increment on overall PDE is reduced at wavelength shorter than $\sim$1350 nm. Since both PDE and DCR depend on $t_{abs}$, we propose the plot in Fig. 7 (right) for evaluating the optimal value. At 225 K, with a PDE of 20%–30%, DCR reduces when $t_{abs}$ increases from 0.5 $\mu$m to 1.5 $\mu$m, while at higher PDE values, thicker absorption region gives lower DCR (since tunneling becomes dominant). At 250 K, the optimal thickness value is between 1.0 $\mu$m and 1.5 $\mu$m, while performance slightly worsens if $t_{abs}$ is increased. Instead, at low temperatures (e.g., 200 K), tunnel-dominated DCR significantly lowers by increasing $t_{abs}$, while PDE increases, thus improving SPAD performance.

Therefore, as for multiplication region, the optimal absorption region thickness value depends on the target operating conditions of the SPAD (temperature and excess bias). However, taking into account typical operating conditions, optimal absorption layer thickness is 1.5–2.0 $\mu$m.

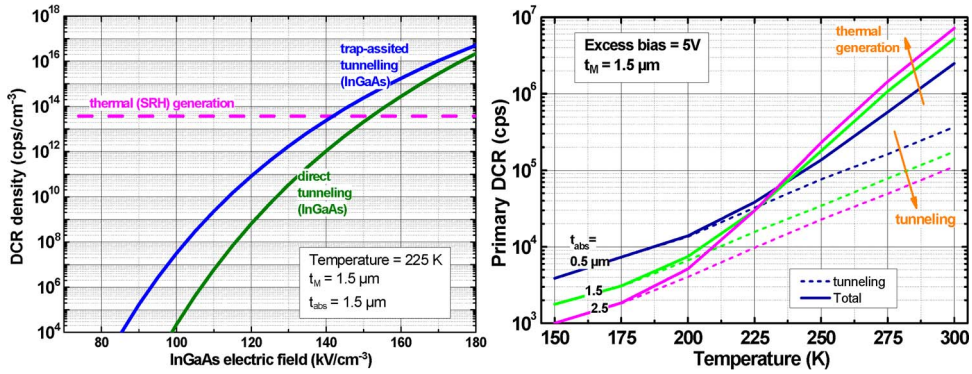


Fig. 6. Simulated contribution to DCR in InGaAs absorption region as a function of electric field, at 225 K (Poole–Frenkel effect was neglected for simplicity) (left). Simulated primary DCR as a function of temperature of SPAD with different absorption region thickness, at 5 V of excess bias (right).

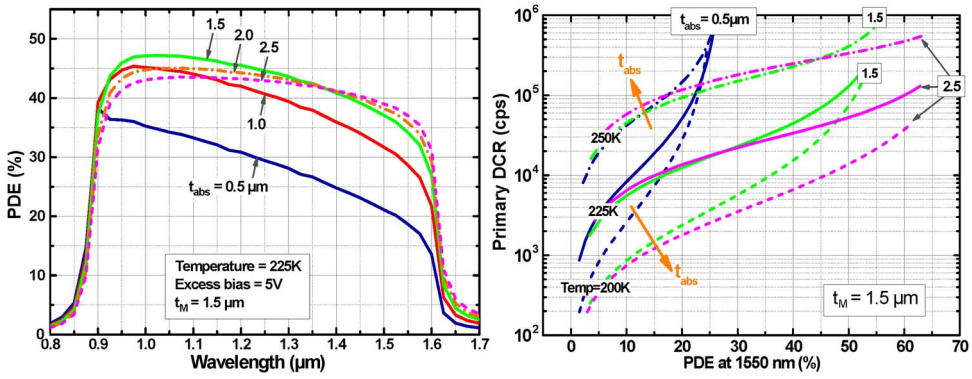


Fig. 7. Simulated PDE as a function of wavelength of SPAD with different absorption region thickness, at 5 V of excess bias (left) and DCR as a function of PDE (at 1550 nm) of SPAD with different absorption region thickness (right).

## 7. Conclusion

We have presented simulation results and discussions on the design of InGaAs/InP SPADs for single-photon detection up to 1700 nm. Breakdown voltage increases and primary DCR significantly lowers as the multiplication region thickness $(t_M)$ is increased, but a lower limit is set by thermal generation; afterpulsing increases, while triggering efficiency is quite constant with $t_M$. We have shown how to tradeoff performance, based on target operating temperature and excess bias, set by application requirements. Instead, the doping level of the multiplication region must be as low as possible $(< 10^{15}\ \text{cm}^{-3})$. Concerning the absorption region, the electric field should be high to improve heterobarrier transit and thus photon-timing response, but there is an upper limit that dependents on operating temperature.

Finally, we have discussed the effect of absorption region thickness $(t_{abs})$. Thicker layer gives not only higher absorption efficiency but also lower avalanche trigger efficiency, thus limiting PDE and reducing primary DCR when tunneling is dominant. Conversely, when thermal generation is the main contribution, DCR increases with $t_{abs}$. Considering a SPAD structure with a 1.5-$\mu$m-thick multiplication region operated at 200–225 K, the optimal range is between 1.5 $\mu$m and 2.0 $\mu$m.

All these simulations and detailed trends can be a valuable tool for getting a better insight on SPAD working conditions, device parameters, and final detection performance.

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