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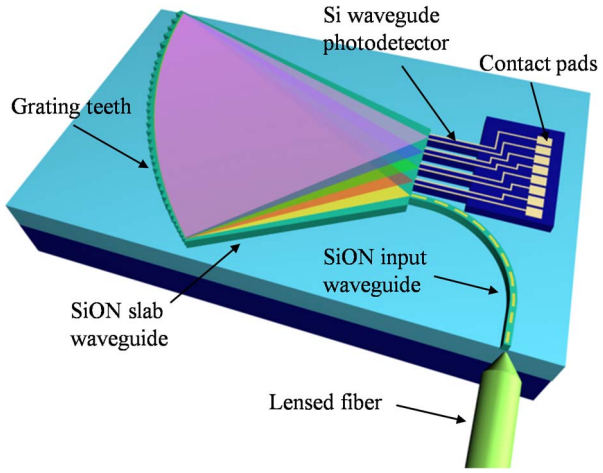

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CMOS-Compatible Integrated Spectrometer Based on Echelle Diffraction Grating and MSM Photodetector Array

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Abstract: We demonstrate an integrated spectrometer-on-a-chip composed of an echelle diffraction grating (EDG) and metal–semiconductor–metal (MSM) waveguide photodetector array based on silicon-on-insulator (SOI). In the passive section, silicon oxynitride (SiON) is chosen as the material for the waveguide core and is deposited after selectively removing the top silicon layer of the SOI wafer. The buried silicon dioxide layer of the SOI wafer functions as the lower cladding for the SiON core waveguide. In the active section, the MSM photodetector array is fabricated on the top silicon layer of the SOI waveguide with a pitch width of 7.5 μm. With the butt-coupling structure, a responsivity of 0.41 A/W is obtained at 850 nm. Based on the CMOS-compatible fabrication process, we have fabricated a 60-channel spectrometer with a chip size of 9 mm $\times$ 6 mm operating around 850 nm. The measured channel spacing is 0.494 nm, with an adjacent channel crosstalk around 18 dB. The channel nonuniformity is less than 1.5 dB. The CMOS-compatible spectrometer with integrated silicon photodetector array can provide a low-cost solution for high-resolution on-chip spectral analysis for visible and near-infrared light with the wavelength below 1100 nm.

Index Terms: Spectrometer-on-a-chip, optoelectronic integration, echelle diffraction grating (EDG), metal–semiconductor–metal (MSM) photodetector array.

1. Introduction

Integrated spectrometer has received great attention in recent years, due to its broad application prospect and inherent advantages such as low cost, compactness, portability, stability, freedom from cumbersome assembly, and suitability for versatile lab-on-a-chip systems. Many different structures have been proposed, including arrayed waveguide grating (AWG) [1], [2], echelle diffraction grating (EDG) [3]–[6], superprism-based photonic crystal [7], microresonator array [8], and so on. Among these different types of structures, planar waveguide gratings, including AWG and EDG, have made great progress along with the fast evolution of optical communication technology. They have a relatively solid and mature research foundation and excellent overall performance in terms of resolution, operating bandwidth, chip size, and fabrication tolerance. Therefore, they are rather promising for practical applications.

Abundant excellent research results with respect to planar-waveguide-grating-based integrated spectrometers have confirmed the competitive strength of such structures. However, most of the work merely focused on the grating structure itself. Few of them have addressed the issue of the

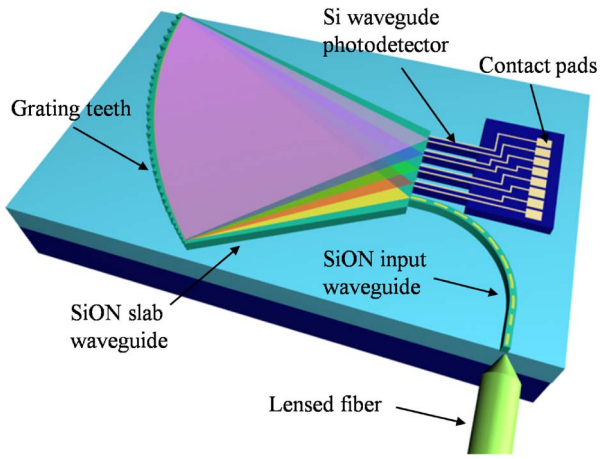


Fig. 1. Schematic of the integrated spectrometer.

integration of photodetector array or more photonic elements on the spectrometer chip, while as a matter of fact, the integration is very desirable to achieve a more robust and practical device. As a pioneering example, J. Brouckaert et al. have demonstrated a 30-channel integrated spectrometer fabricated on a nanophotonic SOI substrate, which consists of an EDG microspectrometer with heterogeneously integrated III–V photodetectors operating around 1550 nm, the commonly used communication wavelength [9]. A channel spacing of 3.2 nm was achieved. Due to its excellent optical detection performance, InGaAs photodetector was chosen and integrated on the SOI-based spectrometer chip using bonding process [10], which is an efficient way to realize the integration of passive and active photonic elements in the wavelength range of 1550 nm. However, the bonding process is not CMOS compatible, thus resulting in a complex and expensive fabrication process.

High-index-contrast silicon waveguide constitutes an excellent waveguide platform for compact spectrometer-on-a-chip operating in the wavelength range above 1100 nm, which is the absorption edge of silicon. Meanwhile, for wavelength range below 1100 nm, it is also very useful to perform spectral analysis with miniaturized chip in many circumstances, such as the plant health monitoring [11], disease diagnosis, [12] and so on. In such situations, high-index-contrast SiON waveguide can play an important role due to its good transparent characteristics from 400 nm to 2000 nm and its widely variable refractive index from 1.47 to 2.3 [13]. Besides, it has a long-term stability and can be integrated with silicon photodetector working below 1100 nm by CMOS-compatible process.

In this paper, we propose and demonstrate an EDG-based CMOS-compatible integrated spectrometer-on-a-chip with SiON as the waveguide core, SiO_2 as the waveguide cladding, and silicon as the photodetector on a SOI wafer. Metal–semiconductor–metal (MSM) structure is chosen here for the photodetector because of its simple fabrication process. Although the device is designed to operate in the wavelength range around 850 nm, the CMOS-compatible structure with integrated photodetector array can provide a general solution for compact high-resolution on-chip spectral analysis at any visible and near-infrared wavelength below 1100 nm.

2. Principle and Design of Device

The schematic of the integrated spectrometer is shown in Fig. 1. Through the input waveguide, light with spectral signal arrives at the boundary of the slab waveguide where the light diverges into the slab waveguide area, then illuminates the grating facets, diffracts back, and converges to the designated waveguide photodetectors according to the wavelength. The MSM silicon photodetector array is butt coupled to the SiON slab waveguide and converts the optical signal to electrical signal, which is then conducted to the readout contact pads by electrical lines.

In contrast to conventional EDG designs [3], [14], [15], the waveguide photodetector array is directly positioned along the output focal line of the echelle grating to receive the diffracted spectral

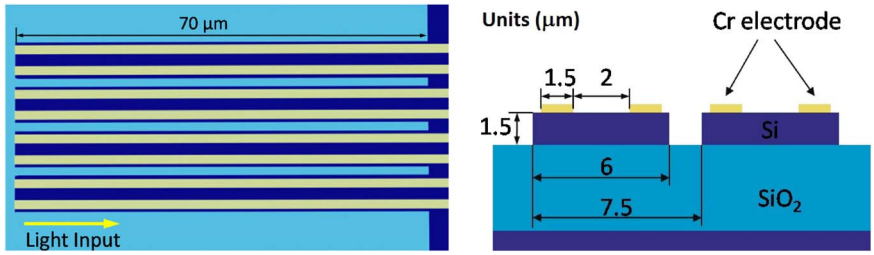
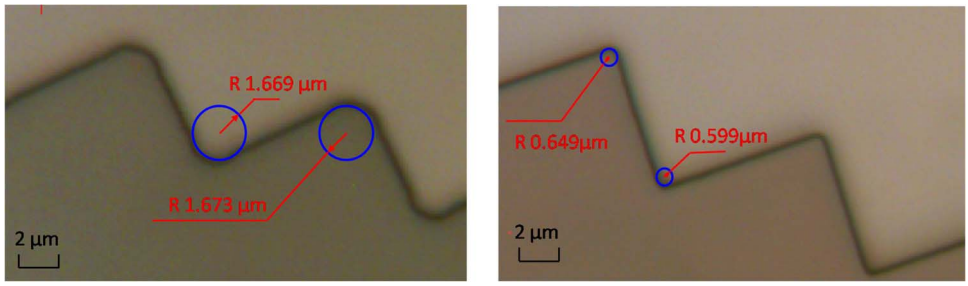


Fig. 2. Top-view (left) and cross-sectional structure (right) of the MSM waveguide photodetector array.

signal. By eliminating the output waveguide array, the chip size and the insertion loss caused by the output waveguides are significantly reduced. Besides, the output channel uniformity is increased by avoiding loss difference resulting from the length difference of the output waveguides. Flat-field design, which means that the input waveguide and the output waveguide photodetector array are aligned in a straight line along the edge of the slab waveguide area of the EDG, is adopted using two-stigmatic point method [16], to facilitate the chip layout. SOI, with a buried oxide layer between the silicon substrate and the top silicon layer, is used as the base wafer for three reasons. First, for the passive section, the buried oxide layer is used as the lower cladding layer of SiON waveguide core, thereby simplifying the fabrication process by eliminating the deep silicon etching and the lower cladding layer deposition step, which would be necessary if a silicon wafer is used to realize butt coupling between silicon photodetector and SiON waveguide. Second, for the active section, the buried oxide layer helps to form the thin silicon waveguide photodetectors to prevent the light from leaking into the silicon substrate, and to confine electron generation in an area with a strong electrical field, thereby enhancing the photodetector responsivity, as well as the response speed. Third, by using the buried oxide layer as the insulating layer, the electron conduction between adjacent waveguide photodetectors is avoided, thus reducing the adjacent channel crosstalk.

The detailed design parameters for the EDG are as follows: the grating diffraction order m is chosen to be 35 so that the free spectral range is more than 24 nm at 850-nm wavelength band, while at the same time, minimizing the negative effect from rounded corners of the grating teeth. To effectively diffract the majority of the input optical power, the grating teeth number N is set to be 510. Considering the operating wavelength of 850 nm and the Rayleigh criterion (λ/mN), the theoretical spectral resolving power of 0.05 nm is obtained. To enhance the reflectivity of the grating, aluminum is coated on the back facets of the grating teeth. Sixty waveguide detectors, with a pitch width of 7.5 μm, are arrayed along the output edge of the slab waveguide. The width of each waveguide detector is 6 μm, leaving a 1.5-μm-wide gap between the adjacent waveguide detectors. The channel spacing is 0.5 nm, corresponding to a dispersion coefficient of 15 000. The height of the SiON slab waveguide and input channel waveguide is chosen to be 1 μm with the refractive index of 1.52 for the SiON core layer and 1.46 for the SiO_2 cladding layer. Although the slab waveguide is marginally multimode at the wavelength shorter than 845.6 nm based on eigenvalue equation for the three-layer structure, the high order mode is very lossy due to leakage to the high-index silicon substrate. Both simulations with the beam propagation method (BPM; by Rsoft Corporation) and the experimental results showed no indication of multimode excitation for the wavelength range investigated. The width of the input waveguide is 1.5 μm. The overall device size is 7 mm $\times$ 9 mm. Scalar diffraction theory [16] is used to simulate the light propagation and to optimize the geometrical structure design.

For the MSM waveguide photodetector, as shown in Fig. 2, two 1.5-μm-wide electrodes are situated on both sides on the top of the 6-μm-wide waveguide detector. As the Si absorption constant is 660 cm^{-1} at 850 nm, the length of the detector is chosen to be 70 μm to ensure that more than 99% of the light is absorbed, which is calculated by the BPM. The absorption of light in the metal electrode is very limited, because the light is well confined inside the silicon waveguide due to its large dimension.



(a) (b)

Fig. 3. Comparison of rounded corners of grating teeth (a) without and (b) with planarization.

3. Fabrication

We fabricate the integrated spectrometer on a SOI wafer with a 3-μm-thick buried oxide layer and a 1.5-μm-thick top silicon layer with a p-type doping concentration of 10^{15} cm^{-3}. The 3-μm-thick oxide layer is sufficient to avoid light leakage from the SiON core waveguide to the silicon substrate. First, chromium is sputtered on the top silicon layer to form the electrodes, connective electrical lines, and readout contact pads by a liftoff process. Then, the 1.5-μm-thick top silicon layer in the passive area is etched by inductively coupled plasma (ICP) with SF_6 and C_4F_8 as the etching gases. A step is created between the etched passive area and the unetched active area. This would degrade the subsequent photolithography resolution due to the existence of an air gap between the low-level passive area and the photomask, which can cause severe diffraction. Therefore, after the 1-μm-thick SiON core layer and 1.5-μm-thick SiO_2 upper cladding layer are deposited on the wafer by plasma-enhanced chemical vapor deposition (PECVD), the wafer is planarized by selectively etching the dielectric layers in the high stage active area with another photolithography step to improve the subsequent contact lithography resolution. Fig. 3 shows that, by adding the planarization process, the radius of the rounded corners of the grating teeth in the low passive area is significantly reduced from 1.7 μm to about 0.6 μm after the development of photoresist, confirming the effectiveness of such process. Thereafter, grating teeth and waveguides are formed through deep etching of SiO_2 and SiON by ICP with CHF_3 and CF_4 as the etching gases. Vertical sidewall with a tilt angle of less than 1° is achieved, which is very important to reduce the insertion loss caused by the reflective coupling-mode mismatch at the grating teeth. A 200-nm-thick aluminum layer is then coated by using a liftoff process on the back facets of the grating teeth to enhance the reflectivity. Finally, the covering SiO_2 layer is deposited by PECVD, and the electrical pads are bared through ICP etching of the deposited film. The microscope image of the fabricated chip is shown in Fig. 4, with expanded views of the grating teeth (a), the photodetcetor array and the electrical lines (b), and the readout contact pads (c).

4. Measurement Results and Discussions

A tunable laser (New Focus 6316 Velocity Laser Diode) was used to measure the spectral response of the device. One-milliwatt TE-polarized light was coupled into the input waveguide via a polarization-maintaining lensed fiber, and the output electrical signal was read out by a current meter (Thorlabs Instrument photocurrent module PDA8000) by probing the readout contact pads on the chip.

We first characterized a reference photodetector connected to a butt-coupled straight SiON waveguide. The loss of the straight SiON waveguide was measured to be 10 dB/cm by cutback method, which is very high due to sidewall roughness caused by nonideal quality of the etching. When characterizing the photodetector, the butt-coupled straight waveguide was cut to 100 μm long to reduce the effect of the waveguide loss. The current–voltage characteristic for various input power levels measured at 850 nm are shown in Fig. 5. A good linearity between the input power and corresponding photocurrent is obtained at 5-V bias voltage, as shown in Fig. 6. The measured

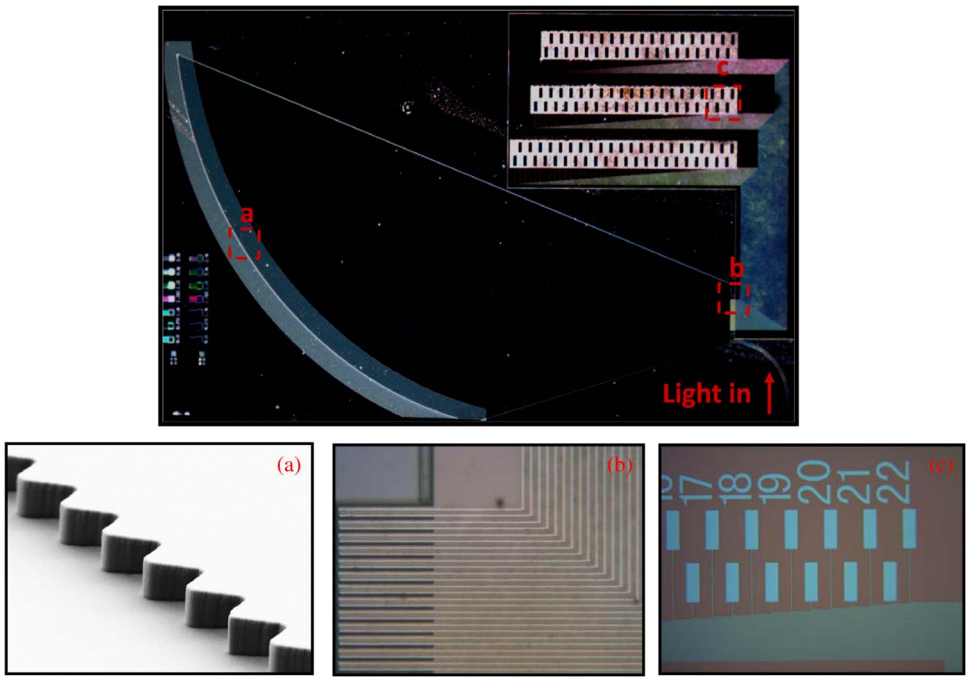


Fig. 4. (Top) image of the spectrometer chip and (bottom) the expanded views: (a) SEM image of the grating teeth; (b) microscope image of the electrode and electrical line; (c) microscope image of contact pads.

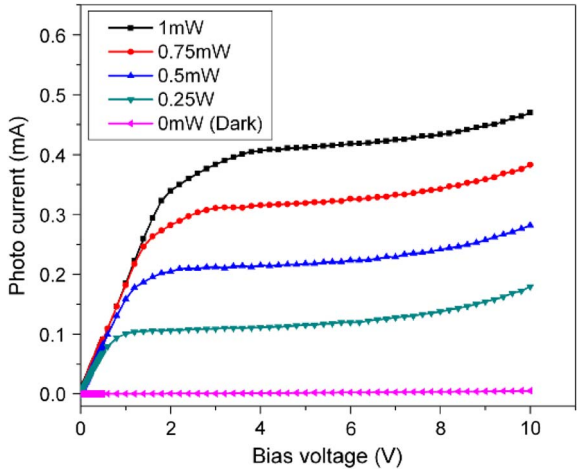


Fig. 5. *I–V* curves of the MSM waveguide photodetector for different input power levels.

responsivity of the reference photodetector is 0.41 A/W, corresponding to an external quantum efficiency of 60%. The 40% loss is mainly attributed to the fiber-waveguide coupling loss, as well as the reflective loss at the interface of the SiON waveguide and the silicon photodetector. The dark current of the photodetector is 2 μA at 5 V bias, and its fluctuation with the time is about 3 nA.

We also characterized the dark currents of the photodetector array at the output focal line of the EDG. The measured values vary from 2.5 μA to 2.8 μA at 5-V bias. The larger values compared with the dark current of 2 μA for the reference photodetector are attributed to the longer electrical lines, which are necessary for facilitating the layout of contact pad arrays. Similarly, the nonuniformity of the dark currents is due to the different lengths of electrical lines in the array.

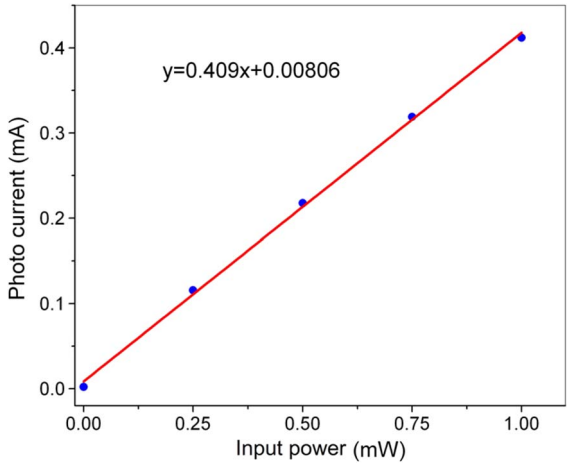


Fig. 6. Photocurrent versus input power at 5-V bias voltage. The straight line gives the linear fit of the photocurrent as a function of the input power.

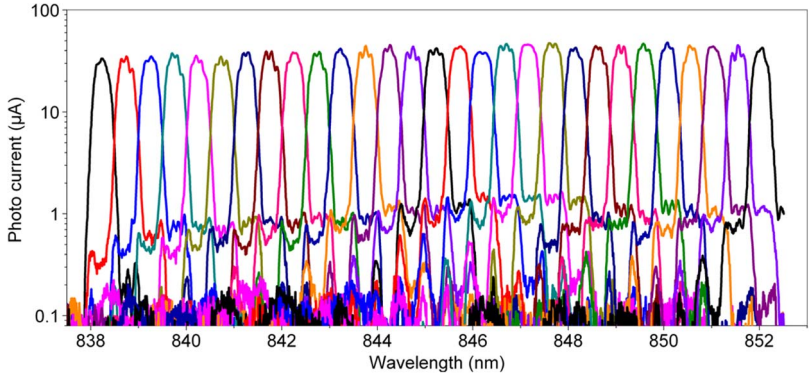


Fig. 7. Overlapped transmission spectra of 29 channels of the integrated spectrometer.

The transmission spectrum was measured by scanning the 838-nm to 852-nm wavelength range of the tunable laser. The light was injected into the input waveguide with TE-polarized mode. Fig. 7 shows the measured spectral responses for 29 channels limited by wavelength range of the tunable laser. It shows that the measured channel spacing is 0.494 nm on average, which is very close to the design value of 0.5 nm. The 3-dB bandwidth is 0.4 nm. The measured channel nonuniformity is rather good for less than 1.5 dB. The adjacent channel crosstalk is around −18 dB. For the central channel, the overall responsivity is 0.046 A/W, corresponding to an external quantum efficiency of 4.82%. Compared with 60% external quantum efficiency of the reference photodetector mentioned above, we can estimate the on-chip loss of the EDG to be about 11 dB.

Shoulders can be observed on both sides of the spectral response peak of each channel. These shoulders may be caused by two mechanisms. One is the light coupled from adjacent waveguide photodetectors due to scattering. The other possibility is that the absorption coefficient of the silicon is not high enough for the waveguide photodetector with the designed length to absorb all the light; thus, the remaining light at the end of the photodetector may diffract into the absorption zone of the adjacent channel. A simple way to lower the shoulders is to increase the length of the photodetectors in the future design. Improving the sidewall roughness in the fabrication will also reduce the crosstalk due to scattering.

The on-chip loss of the designed EDG structure is estimated to be 11 dB. Several factors contribute to the relatively large on-chip loss. First, based on the measured straight waveguide loss

of 10 dB/cm mentioned above, 2500-μm-long input straight waveguide leads to a 2.5-dB loss. Second, sidewall roughness existing in the bend part of the input waveguide causes a large loss. From our simulation, a 60-nm sidewall roughness produces about 3-dB additional loss for the 1200-μm-long bend waveguide with a bend radius of 800 μm. Third, due to the resolution limit of the contact photolithography method, 0.6-μm radius rounded corners of the grating teeth were produced, resulting in a 2.5-dB loss [6]. The remaining loss can be attributed to the sidewall roughness of the grating teeth, the quality of the metal reflective coating, the slab waveguide loss, etc. The loss can be reduced with improvements in the fabrication process.

5. Conclusion

We have reported our first experimental demonstration of a CMOS-compatible 60-channel integrated spectrometer based on EDG and MSM waveguide-photodetector arrays fabricated on SOI wafer. The chip size is 6 mm $\times$ 9 mm. The channel crosstalk is around 18 dB. A spectral resolution of about 0.5 nm has been achieved with a pitch width of 7.5 μm. Although further improvements on the design and fabrication process are required to enhance the performance of the device, the initial results have demonstrated its potential as a low-cost compact solution for photodetector-integrated high-resolution on-chip spectral analysis below the silicon absorption edge of 1100 nm.

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