Silicon Photonics for Inter/Intra-Chip Wireless Communication Using RF On-Chip Antennas

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***Abstract*—This study experimentally demonstrates both inter-chip and intra-chip RF transmission for short-range microwave communication using on-chip antennas, implemented on a silicon photonic platform. The unification of antenna with photonic integrated circuits (PICs) reduces system loss for high data rate communication by eliminating parasitics. We designed, fabricated, and measured two antenna topologies (blade and triangular) for intra-chip communication and one (meander antenna) for both inter-chip as well as intra-chip communication. The three on-chip antenna topologies have resonance at 15.7 GHz, 13.2 GHz, and 12.6 GHz, and maximum transmission coefficient (S21) value above −30 dB for all antennas. Their operation is further validated by low return loss value (S11 ≤ -20 dB), indicating strong impedance matching with minimal power reflection. The intra-chip RF data transmission has been confirmed with bit- error-rate (BER) measurements of below 10^{-9} up to a data rate of 4 Gbps. We have also performed inter-chip communication between two on-chip antennas separated by a distance of upto 18 mm and accomplished 4 Gbps transmission with BER $< 10^{-9}$. Our findings indicate that on-chip antennas integrated onto silicon photonic chips provides a seamless conversion between electrical and optical signals. This integration enables various on-chip RF wireless applications such as chip-to-chip and off-chip communication, along with wireless sensing off-chip. Furthermore, the incorporation of an integrated antenna facilitates the realization of integrated RF photodetector-antenna emitters on a silicon photonic chip, thereby significantly reducing size, weight, area, and power requirements.**

***Index Terms*—Antenna on-chip (AoC), blade antenna, inter-chip and intra-chip wireless communication, integrated microwave photonics (IMWP), meander antenna, monopole antenna, radio frequency photonics (RF Photonics), silicon photonics (SiPh), triangular antenna.**

I. Introduction

THE microwave photonics (MWP) technology has come a long way towards establishing itself as a critical research discipline for microwave application, prominently in telecommunications and sensing systems [1], [2], [3], [4], [5], [6], since its potential realization in 1990s [7], [8]. By processing high frequency microwave signals in the optical domain, MWP offers key advantages such as frequency-independent low-loss behavior, reconfigurability, advanced functionality, and abundant bandwidth (BW). However, the widespread adoption of MWP is hindered by cost, reliability issues, and bulky size due to discrete components. Integrated photonics technologies offer a solution by miniaturizing these components onto a single chip in various material platforms such as indium phosphide (InP), silicon on insulator (SOI) (i.e., silicon photonics), silicon nitride (Si_3N_4), and lithium niobate on insulator (LOI) [3], [4], [5]. Out of these, silicon photonics (SiPh) offers practical advantages such as mature process, low cost, small footprint, and strong optical confinement [9], [10]. The resulting monolithic technology is termed integrated microwave photonics (IMWP), which has gained significant attention in recent years. We expect its proliferation into next-generation applications such as 5G transceivers, wireless sensors, and Internet of things (IoTs). Achieving this requires a complete high-level integration of active/passive photonics components with electronic blocks as envisioned in Fig. 1.

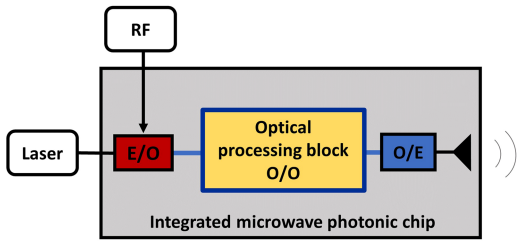

Fig. 1. Envisioned integrated microwave photonics (IMWP) transmitter.

Recently there has been a keen interest in implementing front-end electronics and passive electronics on SiPh platform. For instance, authors in [11] integrated a low-pass RC filter coupled to a photodetector on a SiPh chip. A narrowband LC matching network is monolithically integrated with a germanium photodetector in [12] to convert the output impedance to 50 Ω for efficient power transfer. Similarly, in [13], clock generation blocks of a conventional electronic receiver were enabled by optical passive delay lines and in [14], on-chip peaking inductor is used to improve photodetector bandwidth. A possible driving force behind this trend is the potentially lower cost per surface area of SiPh compared to the contemporary complementary metal-oxide-semiconductor (CMOS) technology nodes [11]. Further, the high resistivity substrate of some

Manuscript received 5 December 2023; revised 27 February 2024; accepted 5 March 2024. Date of publication 12 March 2024; date of current version 29 March 2024. This work was supported in part by the Canadian Microelectronic Corporation (CMC) through the subsidized MPW fabrication and in part by the Natural Sciences and Engineering Research Council of Canada (NSERC) Discovery Program. *(Corresponding author: Ajaypal Singh Dhillon.)*

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Digital Object Identifier 10.1109/JPHOT.2024.3376368

SiPh process has been shown to suppress substrate noise and improve the quality factor (Q) of RF passives [15], [16].

With the rise of integrated radio-over-fiber (RoF) applications in the commercial sector, a case can be made for direct and efficient integration of RF antenna and photonics components. Antenna models for the optimization of such RF-photonics links have been discussed in [17]. An antenna implemented onto a SiPh chip is a significant step in extending the advantages of monolithic integration towards higher frequencies, thereby considerably enhancing the range of achievable integrated photonics functionalities. At microwave and millimeter frequencies, the wavelength is sufficiently short to fit an antenna on chip. Additionally, an antenna on-chip (AoC) will reduce electrical power loss by averting the frequency dependent off-chip parasitic interconnects between the photodetector and the antenna. Also, AoC will eliminate the need for a matching network to transform the system impedance to 50 Ω. This will further improve the design flexibility by making antenna impedance as an additional design parameter [18]. While recent years have seen a rise in hybrid integration for such systems, most implementations have stopped short of integrating the antenna on-chip, preferring off-chip solutions [19], [20].

In this work, we have developed two planar on-chip antenna topologies using a passive SiPh process with one metal layer, demonstrating intra-chip communication. Additionally, we have designed a planar meander monopole on-chip antenna for inter-chip and intra-chip communication, utilizing an active SiPh technology. Such wireless links find use in RoF applications and provide scalable and seamless short-range chip to chip/module to module high speed wireless communication. They facilitate enhanced interaction between networks of sensors and communication networks. In intra-chip communication (in mm), the wireless links do not require high-gain antennas.

We previously demonstrated a proof of concept with a 15 GHz on-chip antenna design in SiPh [21], and we also conducted simulation of planar antennas for intra-chip communication [22] and inter/intra-chip communication [23]. In contrast to [21], this work not only achieves three times the data transmission capacity (from 650 Mb/s to 4 Gb/s), but also demonstrates intra-chip communication. Additionally, it investigates three different antenna topologies, each of which is more compact than previously demonstrated.

The inter/intra chip communication demonstrated here using on-chip antennas on a SiPh chip finds application in clock synchronization/distribution [24], network on chip [25], and wireless tagging [26]. Moreover, the proposed system can be utilized as a last-mile local photonic emitter solution for short-range RoF wireless communication [27], such as in Kiosk communication scenarios. In the later, a user's portable device can transfer high-speed files to or from the content provider via a non-contact wireless communication system with a transmission in millimeter range or less. Further, at millimeter-wave (mmW) frequencies, antenna arrays become feasible on-chip, making the envisioned IMWP system (Fig. 1) particularly attractive for demonstrating photonic-assisted mmW transmission and beamforming [19]. Additionally, the high-speed ultra-short distance wireless interconnects (<5 mm) communication is an appealing use case [28].

TABLE I
MONOPOLE VERSUS OTHER ON-CHIP ANTENNA TOPOLOGIES

Parameters	Antenna Types			
	Meander Monopole [This work]	**Yagi [29]**	**Dipole [30]**	**Patch [31]**
No. of Metal layers/ Process	2/220 nm AMF SOI	6/0.18 µm CMOS	11/65 nm CMOS	8/0.13 µm CMOS
Antenna Area (mm^2)	0.462	1.05	1.8	1.92
Resonant frequency (GHz)	12	60	10	60
S11 (at resonance) (in dB)	-20	-	-19	-17
Bandwidth (GHz)	2	10	23	1
Substrate resistivity (Ω cm)	750	Lossy Substrate	Low-κ Substrate	Lossy Substrate
Demonstrated data rates	4 Gbps	-	2 Gbps	200 Kbps
Design details	No AMC	6 Metals layers (2 used) + Air bridge	High-κ Interposer with PCB used under the chip	Freq. locked loop + AoC

The manuscript is organized as follows: Section II explains the structure of the designed antenna topologies. Next, Section III describes the experimental performance evaluation with S-parameter characterization and RF data transmission results. Section IV outlines challenges of on-chip antenna design. Section V presents a discussion on the results, while Section VI conclude the work.

II. ANTENNA DESIGN CONSIDERATIONS

Monopole antennas are a popular choice for on-chip antennas as they offer several advantages. Firstly, monopole antennas are straightforward to integrate onto a chip due to their simple geometry, which consists of a single element above a ground plane. This approach allows for a smaller antenna footprint and easier to engineer design compared to other types of antennas like Yagi, dipole, and patch antennas. These benefits are summarized in Table I, comparing meander monopole with reports of other on-chip antenna topologies. The demonstrated monopole design occupies the smallest area, even when operating at larger wavelength. Further, it achieves the highest data rates and features a compact layout geometry, utilizing two available metal layers without the need for post processing techniques, such as air bridge, as used in [29] and high-κ interposer combined with a Printed circuit board (PCB) base [30]. Additionally, monopole antennas have a desirable omnidirectional radiation pattern parallel to the ground plane and are well isolated from interference, thanks to the ground plane. In contrast to a dipole antenna (Fig. 2(a)), a monopole antenna (Fig. 2(b)) has a single

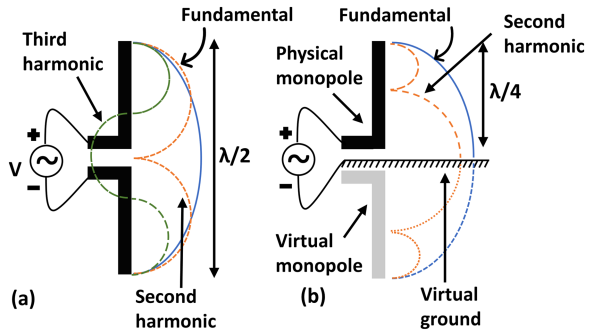

Fig. 2. (a) Current distribution (shown in colored lines) of a dipole antenna and (b) monopole antenna.

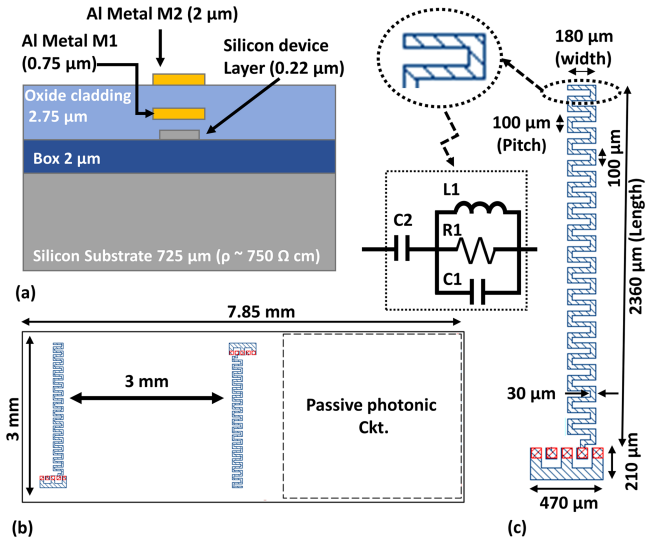

Fig. 3. (a) AMF silicon photonics process stack. (b) Layout of two meander antennas on the same chip. (c) Detailed structural top view of the meander monopole antenna with inset showing the lumped model for the meander section.

pole. The monopole antenna ground plane reflects the electromagnetic wave and creates a virtual mirror image of the antenna element below the ground plane. This creates the virtual effect of a longer dipole antenna (λ/2), though the actual physical length is quarter-wavelength (λ/4), which results in compactness, better radiation pattern and efficiency. Without the ground plane, the radiation pattern of the monopole would be directional and limited in its coverage area.

We have selected three different topologies of the monopole antenna: meander, triangular and blade, for inter and intra-chip communication on a SiPh chip. The unavailability of multiple metal layers in the conventional SiPh process limits the development of advanced antenna topologies. These antennas are designed and optimized using the commercial computer-aided design (CAD) tool ANSYS high-frequency structure simulator (HFSS).

A. *Meander Antenna*

The Advanced Micro Foundry (AMF) SiPh fabrication layer stack used for designing and fabricating the meander antenna is shown in Fig. 3(a). The antenna is implemented on the top aluminum metal (M2), while the ground plane is implemented on both metal layers M1 and M2 connected through an electrical via. A critical challenge to an efficient AoC implementation in silicon is the high dielectric constant of the substrate, which causes a significant portion of the electromagnetic energy to be absorbed into the substrate instead of being radiated into the air [32]. The selected AMF SiPh process has the merit of high resistivity substrate, which reduces the radiated electromagnetic power into the dielectric. This highlights the technological advantage of AMF SiPh technology as an antenna-supportive, and cost-effective process.

The antenna arrangement for investigating the intra-chip communication using meander monopole on an AMF SiPh chip with area 3×7.85 mm^2 is depicted in Fig. 3(b), while Fig. 3(c) shows the labelled structural layout of the meander antenna with its lumped model in the inset. To use RF probes in exciting the fabricated antenna, probe pads of size 70 µm × 70 µm with a pitch of 100 µm are incorporated. Here, the two antennas are placed at a far field distance. The far field starts at the distance of $2D^2/\lambda_{\text{eff}}$ [33], where D is the antenna length and λ_{eff} is the effective wavelength. In the case of the meander antenna resonating at 12.6 GHz, the far field distance is 0.96 mm. In our design, the separation between the two antennas is 3 mm. The meander shape is used to increase the total length of the antenna, allowing it to resonate at lower frequencies than a straight-line antenna of the same size. In the HFSS simulation, a lumped port is used for exciting the co-planar waveguide (CPW) feed of the on-chip antennas.

The inset in Fig. 3(c) shows the lumped model for the meander section, derived from the antenna's geometry. This equivalent model utilizes a four-element lumped circuit consisting of a RLC parallel circuit connected in series with a capacitor [34], [35]. The model demonstrates a good convergence, indicating consistency between simulation and results, when the antenna has three or more bends. The meander-line in this model is considered a parallel RLC circuit, while the top of the radiation element is represented by a series capacitor (C2) resulting from the end effect [36]. The capacitances C1 and C2 are determined by the antenna's reactance when excited at its fundamental frequency. Their value depends on the physical dimensions of the antenna, including the antenna length (L), width (W), and the pitch (P) between the meandered antenna layers [35]. On the other hand, L1 represents the inductance and R1 represents the resistance at the antenna's fundamental frequency. Both L1 and R1 depend on the length (L) and width (W) of the antenna.

For a 12.6 GHz RF transmission, the starting length of the planar monopole antenna is initially set to a quarter of the effective wavelength $(L = \lambda_{eff}/4)$, where $\lambda_{eff} = \lambda_0/\sqrt{\varepsilon_r}$, λ_0 is the resonance in the free space and ε_r (3.9) is the relative permittivity of the oxide cladding below the metal layer. Afterwards, the resonance is optimized by varying the longitudinal length of the antenna. The meandering is then done

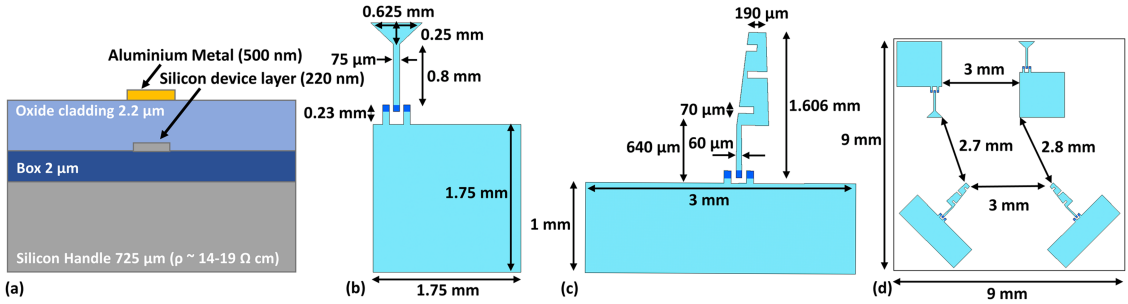

Fig. 4. (a) Stack layers of the ANT SiPh fabrication process. (b) Layout structure of triangular antenna. (c) Blade antenna layout. (d) Layout representation of intra-chip communication arrangement.

for a more compact footprint. When any of the tuning parameters (L, P, or W) is increased independently while keeping the other two constant (either L and P, P and W, or L and W), the resonance frequency decreases. Additionally, increasing L or P independently enhances the antenna efficiency, while an independent increase in W decreases the antenna efficiency [37].

B. Triangular Antenna

The planar triangular monopole antenna is designed and fabricated using the Applied Nanotools Inc. (ANT) SiPh process shown in Fig. 4(a). The three distinct differences in the ANT process over AMF are: 1) reduced thickness of the top metal layer, 2) availability of only one metal layer and, 3) the low resistivity silicon substrate. The lower resistivity of the silicon substrate results in more radiated electromagnetic power going into the dielectric. Fig. 4(b) shows the structural layout of the triangular antenna. The antenna and the ground-signal-ground (GSG) pads are implemented using the aluminum metal layer of thickness 500 nm. The GSG pads are squares of 75 $\times$ 75 µm^2 with a pitch of 125 µm, shown as the darker blue shades on the layouts in between the ground plane and the antenna. The flare angle of the triangular antenna plays an important role in optimizing the bandwidth of the antenna [38].

The two on-chip triangular antennas are fabricated on a 9 $\times$ 9 mm^2 chip area. The antenna orientation on the ANT SiPh chip is depicted in Fig. 4(d). As before, all the antennas are placed at a far field distance. In the case of the triangular antenna resonating at 15.5 GHz, the far field distance is 1.83 mm. In our design layout, the minimum separation between any two antennas is not less than 2.7 mm.

The triangular planar monopole antenna offers advantages over a simple monopole antenna of the same length. Its increased effective current path allows for a reduction in the required monopole length at a fixed operating frequency. The length of the monopole decreases as the flare angle increases, and the equilateral triangular monopole provides the maximum attainable bandwidth. As with any monopole, the starting point of designing the antenna involves setting the length to be approximately $\lambda_{eff}/4$. Afterwards, the antenna performance is tuned using HFSS and the design strategies detailed in [38], [39].

C. Blade Antenna

Finally, we investigate the implementation of on-chip blade antennas as the third antenna topology. Blade antenna use is dominant in airborne applications due to its compact and aerodynamic shape. These antennas are integrated on the same ANT SiPh chip that we used for triangular antennas. Blade antenna detailed layout geometry is shown in Fig. 4(c), and its arrangement on the ANT chip is illustrated in Fig. 4(d). As seen from Fig. 4(d), blade antennas are designed with a 45° rotation with respect to the vertical axis to maximize S21 transmission. This 45° rotation, though useful, leads to a challenging antenna probing approach during characterization, which we will discuss in the next section.

The miniaturized blade antenna is designed to resonate at the frequency of 13.2 GHz. Initially, the antenna length is set to be $\lambda_{eff}/4$. As seen from Fig. 4(c), horizontal slots are inserted in the radiating element to lengthen the current path, thereby decreasing the antenna resonance. The resonant frequency decreases further with the depth of the horizontal slots. These slots also facilitate better broadband performance [40]. The far field distance for blade antenna starts at 1.17 mm and the separation between the two-blade antenna is 3 mm. The GSG probe pad area and pitch are the same as used in triangular antenna.

III. Experimental Results

To validate the proposed monopole antenna topologies, we carry out S-parameter characterization, inter-chip, and intra-chip data transmission experiments for each antenna. The measurements were carried out on a SemiProbe LA-150 high frequency (HF) probe station placed on an antivibration table as shown in Fig. 5. The antenna under test is placed horizontally on the chuck base. To increase measurement accuracy, short-open-load-thru (SOLT) calibration is done using the Picoprobe CS-5 calibration substrate. This method eliminates the errors due to the vector network analyzer (VNA), the RF cables, and the RF probes, and move the reference measurement plane to the tip of the feeding probe.

A. Meander Antenna

1) S-parameter Characterization: S-parameters are measured with the VNA (Keysight N5247B) by placing two identical

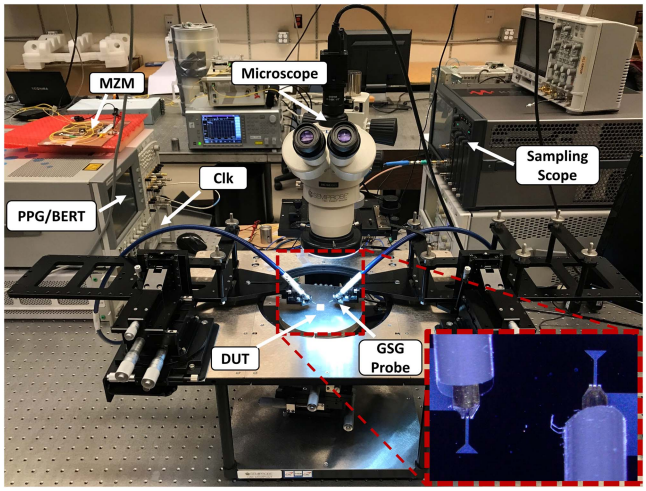

Fig. 5. Photograph of the probe station used for on-chip antenna S-parameter and transmission measurement. MZM: Mach-Zehnder modulator, PPG: Programmable pattern generator, BERT: Bit error rate tester. Clk: Clock.

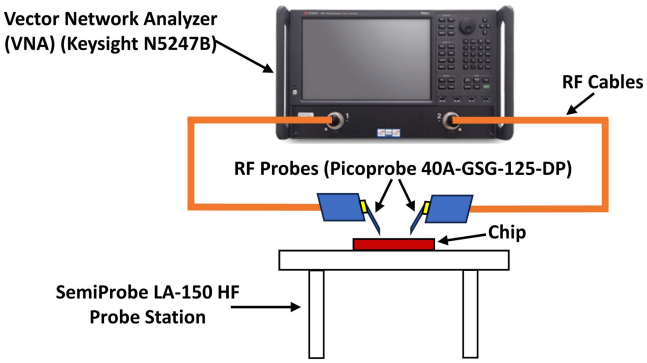

Fig. 6. S-parameter experimental measurement setup.

RF probes (Picoprobe 40A-GSG-125-DP) (see Figs. 5 and 6) onto the same pair of antennas. Measured and simulated reflection coefficient (S11) along with transmission coefficient (S21) for intra-chip communication are shown in Fig. 7(a). The distance between the two meander antennas during this measurement is approximately 3 mm.

Note that there are discrepancies between the simulated and measured values. This is because of the influence of the RF probes and the measurement environment on on-chip antenna characterization. Adding an accurate probe model into the antenna simulation leads to increased level of agreement in simulation and measured S-parameter response. This will be further elaborated in sub-section D. The measured transmission (S21) peak for various inter-chip distances is also shown in Fig. 7(b).

2) Intra-Chip Data Transmission: Figure 7(d) depicts the experimental setup for RF intra-chip data transmission using meander antennas. In this setup, a 1550 nm continuous wave signal from a tunable C-band laser source (Thorlabs TLX1) is modulated with a Mach-Zehnder modulator (MZM, iXblue MX-LN-40). A 12.6 GHz RF carrier signal (with 18 dBm power) generated by a clock synthesizer (Anritsu MG3692A) is halved using a 50:50 RF splitter. One RF splitter (API Weinschel 1575, RF bandwidth of 40 GHz) output is modulated with a pseudorandom binary sequence (PRBS) of length of 2^7-1, generated by a programmable pattern generator (PPG, Keysight N4903B) using an RF mixer (Marki M1R-0726, RF bandwidth of 26.5 GHz). This signal acts as the RF input to the MZM. The PPG data rates vary from 650 Mbps to 4 Gbps. The selected data rates are within the bandwidth capability of the on-chip antenna being tested. The selected carrier frequency (12.6 GHz) corresponds to the maximum S21 measured (Fig. 7(a)). The output of the MZM modulator is amplified by an erbium doped fiber amplifier (EDFA, Keopsys), then filtered with an optical filter (−3 dB bandwidth of 0.69 nm) centered around 1550 nm, followed by a variable optical attenuator (VOA, JDS Uniphase), before reaching an off-chip photodetector (PD, Finisar XPDV2120R-VF-FA, bandwidth of 50 GHz with responsivity of 0.65 A/W) through a 10/90 coupler, with 10% of the output being monitored by an optical power meter (EXFO, FPM-600). Next, we connect the GSG pads of the on-chip antenna to the PD output via a 40 GHz RF probe.

On the receiver side, the received signal from the second antenna is mixed with the same carrier frequency signal (12.6 GHz) by making use of the second part of the RF splitter output. The mixer output is then amplified ($\sim$ 50 dB) and filtered (cut off frequency $f_c = 2$ GHz), before connecting to the error-detector (ED, Keysight N4903B) or sampling oscilloscope (Keysight, DCA-X N1000A).

Eye diagrams were captured at the output using the sampling scope (DCA), while BER values were noted using the bit error rate tester (BERT). As per our setup, eye diagram and BER value cannot be observed at the same time. So, the eye diagram included in the Fig. 7(c) is taken few minutes later than the corresponding BER values. Fig. 7(e) and (c) shows the measured eye diagram and BER performance for intra-chip communication. A data rate of up to 3 Gbps was achieved over an on-chip distance of 3 mm with a BER less than 10^{-9}. As seen from Fig. 7(c), the BER worsens as the optical power at the PD input decreases and as data rate increases, as expected.

3) Inter-Chip Data Transmission: For demonstrating inter-chip transmission, the experimental setup shown in Fig. 7(d)(explained in the previous section) is used. Here, the output of the low-pass filter is connecting to the sampling scope (DCA) to visualize and capture the eye diagrams at the input signal data rate. In contrast to intra-chip communication, we employ two antenna chips with varying distance (S) in between. This inter-chip arrangement is depicted in the top right of Fig. 7(d) above the antenna pair. Data transmission is carried out from data rate at 620 Mbps to 4 Gbps with the chip separation (S) varied (5, 8, 10, 13, and 18 mm). The power levels and the frequency used is the same as in the last case.

Figure 8 illustrates the measured eye diagrams at different data rates for each distance. All the eye diagrams are labeled with signal to noise ratio (SNR), peak to peak voltage and data rate information. At a fixed separation S, the quality of the eye understandably decreases with increasing data rate as the loss increases. Also, the eye quality deteriorates with increasing separation S, and this effect is more prominent at higher data rates. Maximum data rate of 4 Gbps was achieved for inter-chip

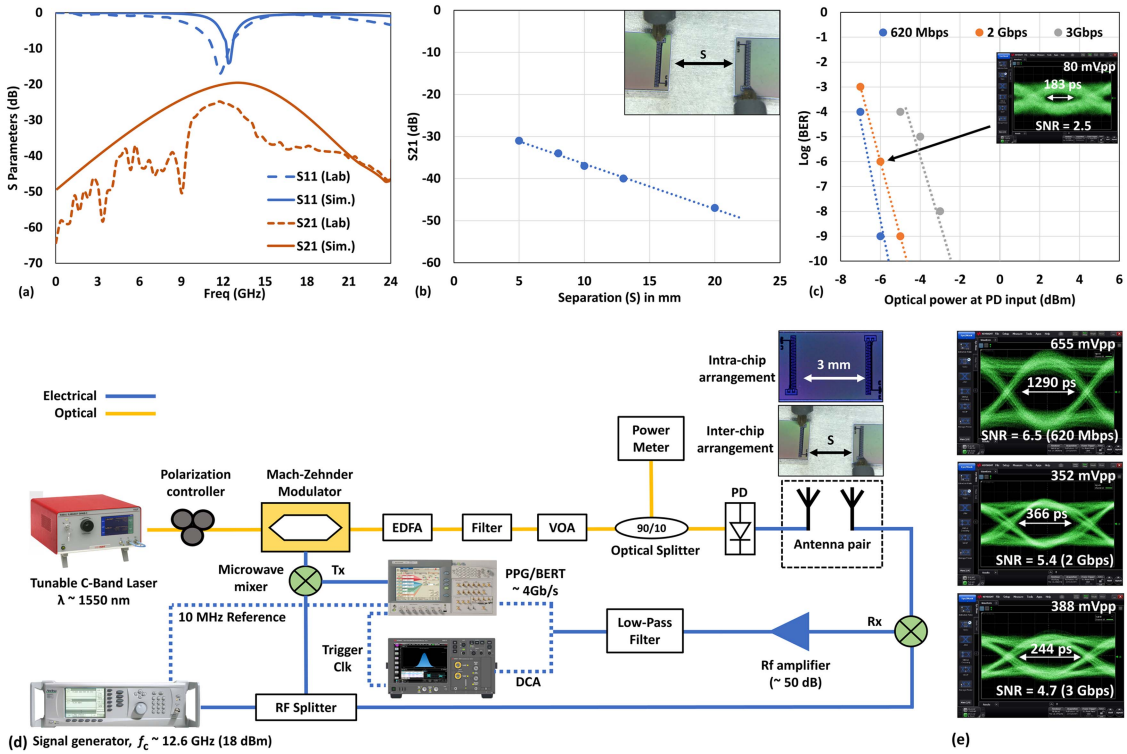

Fig. 7. (a) S-parameters of the meander antenna. (b) Measured S21 variation of the meander antenna with distance. (c) Measured BER for intra-chip communication. (d) Measurement setup for inter and intra-chip communication. (e) Measured eye diagrams for intra-chip transmission of upto 3 Gbps. EDFA: Erbium doped fiber amplifier, VOA: Variable optical attenuator, PD: Photo-detector.

Fig. 8. Measured eye diagrams for inter-chip transmission using the meander antenna.

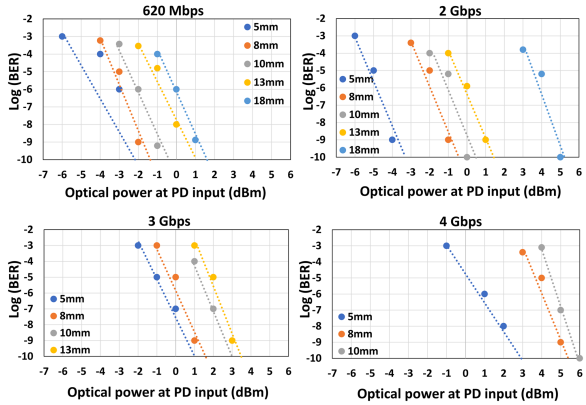

Fig. 9. Measured BER for inter-chip communication using the meander antenna.

transmission. Accordingly, the BER curves for 5, 8, 10, 13, and 18 mm separation at 620 Mbps, 2 Gbps, 3 Gbps, and 4 Gbps are shown in Fig. 9. These BER values are measured by connecting the output of the low-pass filter to the BERT (Keysight N4903B) instead of the DCA. The antenna achieves a BER $< 10^{-9}$ for all distances at 620 Mbps and 2 Gbps. For 18 mm separation, there was no transmission above 2 Gbps, while for 13 mm, no open eye at 4 Gbps. The PD's limited ability to convert the optical input into a detectable electrical signal is the cause of its inability to drive the antenna at these distances. Further, it is assumed that with proper forward error correction (FEC), greater distance and data rates could be obtained [41].

B. Triangular Antenna

1) S-parameter Characterization: Fig. 10(a) and (b) shows the microphotograph of the on-chip triangular monopole antenna with RF probe placed on the GSG pads while conducting S-parameters and data transmission measurements (Fig. 5),

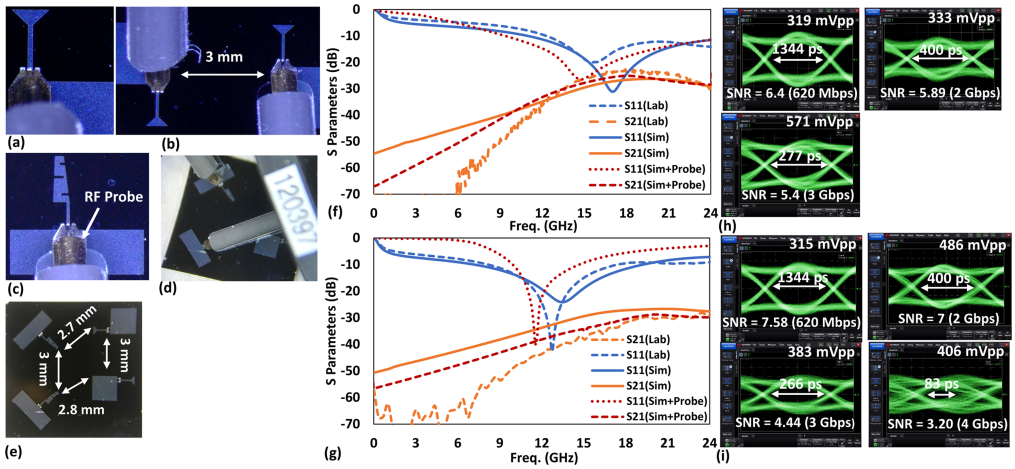

Fig. 10. (a) S11 probing configuration of the triangular antenna. (b) S21/intra-chip data transmission probing configuration of the triangular antenna. (c) S11 probing configuration of the blade antenna. (d) S21/intra-chip data transmission probing configuration of the blade antenna. (e) Micro-photograph of the entire ANT chip. (f) Simulated (with/without RF probe model) and measured s-parameters of the triangular antenna. (g) Simulated (with/without RF probe model) and measured s-parameters of the blade antenna. (h) Measured eye diagrams for intra-chip transmission using triangular antenna. (i) Measured eye diagrams for intra-chip transmission using blade antenna.

whereas Fig. 10(e) shows arrangement of all antennas fabricated on the ANT SiPh chip. S-parameters are measured using the VNA and 40 GHz RF probes. Measured and simulated (including RF probe model) reflection coefficient (S11) and transmission coefficient (S21) for the triangular antennas are shown in Fig. 10(f). The measured S21 validates the intra-chip transmission between the on-chip antennas. For both S11 and S21, simulation including probe model shows a better agreement with the lab measured values compared to the simulation results without RF probe model. The remaining deviations likely stem from uncertainties in the RF probe CAD model and unavoidable inaccuracies in probe positioning during measurement. Further, the inability to fully simulate the entire test setup for ease of computation, fabrication variabilities and RF probe crosstalk along with the challenge of accounting for the coupling between the probe tip and the dummy metal (to meet the metal-density requirement) that cannot be entirely de-embedded, contributes to the disparities seen in the results.

2) Intra-Chip Communication: We use the experimental setup shown in Fig. 7(d) to validate the intra-chip data transmission for triangular on-chip antenna. Fig. 10(b) shows the microphotograph of the chip with RF probes placed on the antenna pads while data transmission was being carried out. The resulting measured and labelled eye diagrams are presented in Fig. 10(h). A data rate of upto 3 Gbps was achieved with BER $< 10^{-9}$. At a data rate of 4 Gbps, the eye diagram exhibits closure due to bandwidth limitation. The relative positioning of antennas to each other also dictates the quality of data transmission. The corresponding BER curves by varying the optical input power of the PD are shown in Fig. 11(a).

C. Blade Antenna

1) S-parameter Characterization: The measured and simulated (including RF probe model) S11 and S21 values for the on-chip blade antenna are shown in Fig. 10(g). Fig. 10(c) and (d) show the on-chip antenna setup photos with RF probe placement during the measurement process (Fig. 5). In contrast to Fig. 10(b), one distinction to note in Fig. 10(d) is that during probing, one RF probe comes from the bottom of the antenna whereas the second one comes from the top. This is because of the arrangement of blade antennas with an angle of 45° rotation with respect to the vertical axis. The design of the probe station made it impossible to probe the antennas from the same side in this case. Simulated and measured results agree well in terms of resonance frequency in the frequency range of interest.

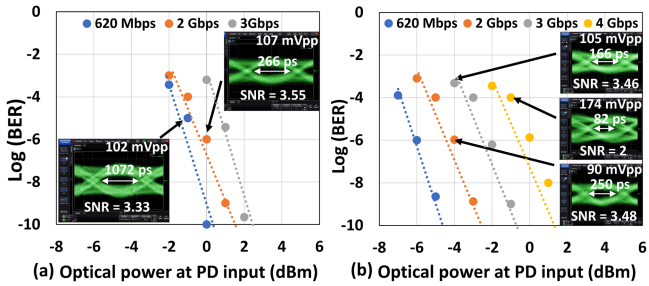

Fig. 11. Measured BER for Intra-chip communication in (a) triangular antenna, (b) blade antenna.

2) Intra-Chip Communication: Using the same experimental setup shown in Fig. 7(d), the measured eye diagrams for intra-chip data transmission are shown in Fig. 10(i). We were able to achieve data rates upto 4 Gbps with BER $<10^{-9}$. The corresponding BER curves for all data rates with varying input optical power at PD are presented in Fig. 11(b). Labelled eye diagrams observed at certain optical power levels are also added to the BER curves. As expected, the number of errors increases with a decrease in PD's optical input.

D. RF-Probe Model Design

To mitigate the impact of the RF probe on the antenna's characteristics, a probe model (Fig. 12(a)) was developed using

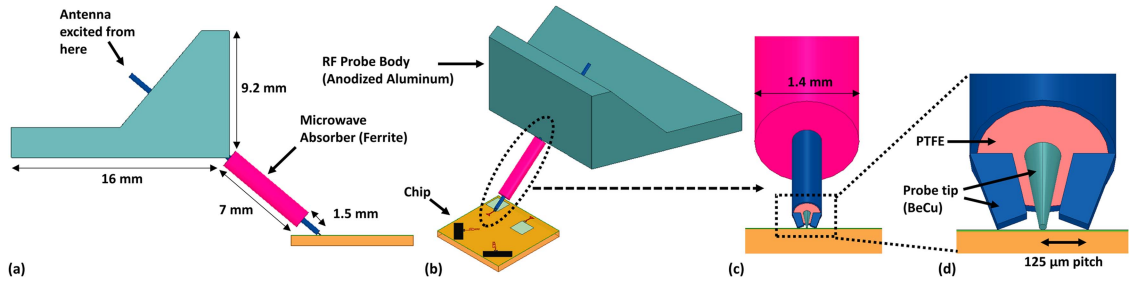

Fig. 12. GGB probe CAD model (a) sideview (b) diagonal from above view (c) front view (d) zoomed front view. PTFE: polytetrafluoroethylene, BeCu: Beryllium-Copper.

ANSYS HFSS and accounted for in the antenna simulation (Fig. 10(f) and (g)). In the model presented in Fig. 12(a), the feeding port was relocated to the top of the probe to excite the entire structure. GGB Inc. does not provide CAD models and other proprietary information. The limited information is available in [42]. The model depicted in Fig. 12(a) to (d) is based on a combination of microscopic photographs, correspondence with GGB engineers, and educated assumptions.

To prevent unwanted propagation along the outside of the coaxial cable, the conductor is surrounded by an absorptive material (Ferrite, as suggested by GGB). The inner conductor is isolated with polytetrafluoroethylene (PTFE) as the dielectric. The centre contact pin is an extension of the inner conductor and is sharpened (as shown in Fig. 12(d)) to ensure a small contact area with reliable connection to the antenna under test. Beryllium-Copper (BeCu) is chosen as the material for the probe tips due to its superior strength, hardness, and spring properties compared to pure copper, while demonstrating high electrical conductivity [42]. Further, anodized aluminum is utilized for the probe body. To reduce the size of the electromagnetic simulation volume, and thus to make it solvable with the available computational power, the back portion of the probe body is omitted, and metal chuck is represented as a ground plane in the simulation.

However, the simulation of the meander monopole antenna, incorporating the RF probe model, could not be demonstrated due to the limited computational resources.

IV. On-Chip Antenna Challenges

The on-chip antenna environment presents distinctive challenges that adversely impact the performance of the antenna. The majority of these issues stem from the silicon substrate itself [43]. Firstly, the high permittivity of the silicon substrate directs the antenna's radiation predominantly into the substrate instead of the air, which diminishes antenna efficiency. Secondly, the low resistivity of the silicon substrate exacerbates this issue by providing a low-resistance path for electromagnetic waves, causing a reduction in radiation efficiency. Consequently, a significant portion of RF power is absorbed by the silicon substrate as heat rather than being radiated into the air. In addition, a thicker substrate introduces surface modes that result in power loss. When the substrate exceeds one-tenth of a free space wavelength, substantial surface waves are supported [44]. These high order surface waves distort the desired antenna radiation pattern and polarization characteristics.

Furthermore, the design rule check (DRC) rules, associated with satisfying the minimum metal density requirement, may necessitate the insertion of dummy metal blocks into the layout. Consequently, this inclusion can cause a shift in the performance parameters of the antenna design [18]. Compared to conventional CMOS technology, silicon photonics enabled SOI on-chip antennas presented in this study lack the flexibility of multiple metal layer. This limitation restricts both complex antenna designs and the use of efficiency-enhancing techniques such as artificial magnetic conductors (AMCs) [45] and partially reflective surfaces (PRSs) [46].

Another significant challenge in on-chip antenna design is mitigating parasitic coupling between the antenna and neighboring structures, such as inductors, capacitors, bond pads, transmission lines, and active devices such as photodiode, MZM modulator, and transistor. These structures are often placed in close proximity to conserve chip area and reduce interconnect lengths. Passive components like inductors, capacitors, and transmission lines are more susceptible to crosstalk due to their larger size compared to active devices.

The coupling intensity depends on the operating frequency, separation distance, and the proximity of the structure (near field or far field). For example, authors in [47] found that the coupling between on-chip monopole antenna and the spiral inductor is strongly frequency dependent. The integrated antenna slightly reduces the inductance and the quality factor of the inductor, while the inductor changes the input impedance and increases the cross-polarization radiation of the antenna. Similarly, the coupling between coplanar waveguide (CPW) lines and on-chip monopole antennas is less frequency sensitive but increases with separation distance due to larger magnetic coupling [47].

Several strategies can mitigate coupling such as ensuring opposite current directions between the antenna and nearby inductors [48], implementing isolation via's and guard shields [49], [50], using surface wave suppressing techniques [44], and carefully optimizing the placement of sensitive structures relative to the on-chip antenna using electromagnetic simulation tools. It is worth noting that, compared to the conventional radio frequency integrated circuits (RFICs), silicon photonics chips use fewer passive elements like inductors, capacitor, and transmission lines.

TABLE II
PERFORMANCE COMPARISON OF ON-CHIP ANTENNAS TOPOLOGIES

Parameter	Meander				Triangular			Blade	Monopole (SOI)	
	This Work	Ref [51]	Ref [52]	Ref [21]	This Work	Ref [45]	Ref [46]	This Work	Ref [53]	Ref [54]
Technology	AMF 220 nm SOI SiPh	NTU 1.2 µm CMOS	TSMC 65 nm CMOS	AMF 220 nm SOI	ANT 220 nm NanoSOI SiPh	TSMC 0.18 µm CMOS	IBM 0.13 um BiCMOS	ANT 220 nm SOI	Trap-rich high-resistivity (HR) SOI	180 nm SOI CMOS
Area (mm^2)	0.462	~ 0.08	0.075	6.7	5.3	1.51	0.858	7.8	~ 5	1.87
Resonant Frequency (GHz)	12	24	28/60	15	13	60	69	15	6	29.5-51
S11 (at resonance) (in dB)	-20	-12	-12	-40	-20	-20	-17	-42	-27	-30
Bandwidth (GHz)	2	6	2	0.2	8	10	>10	9	0.68	21.5
Substrate resistivity (Ω cm)	750	5000	13.5	750	14-19	-	-	14-19	> 3000	1000
Demonstrated data rate (Gbps)	4	3.33	-	0.65	3	-	-	4	-	-
Integration with PD and other photonics blocks	Achievable	NA	NA	NA	Achievable	NA	NA	Achievable	NA	NA
Design details	2 metals, No AMC	1 metal, Doping, No AMC	9 metals, Packaging substrate	2 metals, No AMC	1 metal, No AMC	6 metals, AMC on metal 1	7 metals, including PRS, Antenna glued to PCB	1 metal, No AMC	Folded Monopole	Monopole antenna with on-chip switches

V. DISCUSSION

The surging trend toward higher operational frequencies opens exciting possibilities for integrated antennas on silicon photonics (SiPh) chips. These antennas have the potential to revolutionize high-volume applications by overcoming the power, reliability, and cost limitations of conventional electronics. Monopole on-chip antennas have gained popularity due to their simplicity, versatility, low cost, and compactness of the design. The demonstrated monopole on-chip antenna structures on SiPh chip validates inter and intra-chip wireless RF transmission of up to 4 Gbps with quality eye diagrams and low return loss value ($S11 \leq -20$ dB). 18 mm is the maximum distance over which inter-chip communication (up to 2 Gbps) has been established.

Table II presents the performance comparison of state of art on-chip antennas. Among the list, the meander antenna design presented in this work demonstrates the highest transmission data rate without requiring substrate doping [51] or packaging substrate [52]. While our proposed antenna design utilizes a slightly larger footprint compared to [51] and [52], it is important to note that its operating frequency is lower. Transitioning the same design to higher frequency would consequently reduce the antenna size. Similarly, the triangular and blade antenna designs are simplistic, requiring only one metal layer, and with no need of AMC (as in [45]) or partially reflective surface (PRS) along with PCB as employed in [46]. While other SOI topologies exist, they rely on complex techniques such as trap-rich high-resistivity substrates [53], which involves introducing a defect layer rich in traps to enhance the effective resistivity of substrate, leading to reduced RF losses and substrate crosstalk. Alternatively, some utilize reconfigurable on-chip switches with chip glued onto a PCB [54]. These techniques are used to improve the on-chip antenna gain and minimize RF losses. Furthermore, the ease of integration with photodiode (PD) and other photonics components enhances the practicality of our designs, ensuring versatile applicability in Si-based integrated photonic systems. Given the absence of any comparable on-chip blade implementation in the existing literature or patent information, the column dedicated to the blade antenna presents only the details of our proposed design. Table III summarizes the results for the three designed on-chip antennas. With an area of only 0.462 mm^2 and an optical sensitivity at an input optical power of -6 dBm at the PD for BER below 10^{-9}, the meander monopole antenna is an attractive choice.

TABLE III
SUMMARY OF MONOPOLE ON-CHIP ANTENNA PERFORMANCE

Parameter	Antenna Type		
	Meander	Triangular	Blade
No. of metal layers/Process	2/AMF	1/ANT	1/ANT
Area Occupied (mm^2)	0.462	5.30	7.8
Optical sensitivity (in dBm) at PD for BER < 10^{-9} at 620 Mbps/4 Gbps	-6/-	0/-	-5/2
S11 (at resonance) (in dB)	-20	-22	-45
S21 (Maximum) (in dB)	-25	-23	-30

Ideally, all the components of microwave photonics including the photodetector (PD) with the antenna should be on one monolithic chip for the best optimized system. Yet, the recent integrated microwave photonics system implementations [19], [20] avoid on-chip antennas, as silicon substrate is considered not optimum for antenna implementation due to its high permittivity and low resistivity. However, these shortcomings can be overcome by utilizing SiPh technologies with high resistivity substrate (as in AMF SiPh used here). AMF SiPh with provision of two different substrate thicknesses (725 µm and 120 µm (used in [21]) also allows for further optimization of antenna performance. Further, as we move to millimeter wave (>30 GHz, 60 GHz systems) and terahertz range (> 100 GHz) applications,

the size of antenna reduces, and antenna arrays become feasible. Such arrays can be used to achieve better gain for more efficient inter-chip and intra-chip communication. Additionally, selecting antenna topologies with directional antennas instead of uniform pattern antennas depending upon the application enhances performance. All these merits along with low loss due to the elimination of off-chip parasitic interconnects, and flexibility in terms of antenna impedance makes an encouraging case to integrate antenna on a single SiPh chip for very short-range wireless communications and sensor applications.

Effective integration of the proposed SOI antenna with a SiPh system requires careful mitigation of electromagnetic interference with nearby SiPh components, selecting a high-responsivity photodetector for improved sensitivity, and minimizing coupling loss for optimal power delivery. The data rate is limited by the antenna's bandwidth and can be improved by employing wider BW antenna structures, or higher carrier frequency of operation, such as in [55], [56], where a millimeter-wave wideband bond-wire antenna demonstrates 11 Gb/s wireless data transmission with a BER of less than 10^{-11} at 56 GHz. Using a PD with improved responsivity also leads to better antenna and system performance. In the case of a PD with lower responsivity, higher optical power would be necessary. For example, as demonstrated in [57], a Ge-on-Si PD with 1.14 A/W responsivity at 40 Gb/s improves the optical sensitivity and hence the link budget by 1.82 dB compared to a PD with 0.75 A/W responsivity. Hence, it is anticipated that the possible integration of complete Si-based IMWP wireless systems (with on-chip antenna) will lead to application of integrated photonics in near future technologies like 5G, airborne and autonomous vehicles, and the work presented in this paper is useful for those interested in emerging high speed short-range wireless communication systems.

VI. Conclusion

In summary, this paper demonstrated for the first time, intra-chip communication in a commercial SiPh platform using on-chip antennas resonating at 15.7 GHz and 13.2 GHz. Along with that, inter-chip communication with maximum separation of 18 mm has been demonstrated with on-chip antenna resonating at 12.6 GHz. Successful data communication (BER $<10^{-9}$) with quality eye diagrams validate the feasibility of intra and inter-chip wireless transmission in SiPh chip with data rates of upto 4 Gbps. The three on-chip monopole antenna topologies implemented are: meander, triangular and blade. Their respective sizes are: 2570 µm $\times$ 180 µm (0.462 mm^2), 3.03 mm $\times$ 1.75 mm (5.30 mm^2) and 3 mm $\times$ 2.6 mm (7.8 mm^2). Out of three, meander monopole takes the least area. This is mainly due to the meandering of the antenna structure. As expected, the BER performance degrades with interconnect distance and data rate. The quality BER performance, open eye diagrams, and low return loss (S11 $\leq -$ 20 dB) at resonant frequencies validate the possible integration of on-chip antenna with an on-chip PD on a Si- based IMWP system.

With the race towards adopting higher operational frequencies, and the potential implementation of antenna with PD on SiPh chip, dense integration is achievable in IMWP, thereby leading to a cost-effective, area-effective solution for inter/intra-chip and RoF applications. One such RoF application could be a highly integrated photonics assisted beamforming system with on-chip antenna array at millimeter wave frequencies.

Acknowledgment

The authors would like to thank James Miller and James Dietrich of CMC Microsystems for providing us with the SemiProbe high frequency probe station and guiding us in its assembly and use. A special thanks to Dr. Jocelyn Bachman of ANT, Alberta for assistance in the fabrication process, and to Milad Mokhtari for help with the HFSS simulation. The authors would also acknowledge undergraduate capstone students Sabrina Chan, Lara Ghanem and Andrea Haniak for assisting in this research.

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