Designing a Sub-20V Breakdown Voltage SPAD With Standard CMOS Technology and n/p-well Structure

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***Abstract*—We have proposed a structural design for a single photon avalanche diode with a low breakdown voltage. This diode is fabricated using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm HV CMOS technology, and it can maintain a high operating excess voltage in an n-on-p design without requiring any additional customized well layers. The n-on-p type device is particularly advantageous for a 3D-stacked backside illuminated structure and offers excellent photon detection capabilities at longer wavelengths. By incorporating a high doping concentration PDD well layer, we can significantly increase the excess bias, resulting in enhanced photon detection probability in the near-infrared wavelength range, all while maintaining a lower voltage due to a reduction in breakdown voltage. This design also leads to power consumption savings. As a result, our designed device is well-suited for consumer applications such as 3D image rendering and LiDAR technology.**

***Index Terms*—Single photon avalanche diode, photo detector, CMOS sensor, LiDAR.**

I. Introduction

GEIGER-MODE operation of single-photon avalanche diodes (SPADs) promises single-photon level sensitivity and picosecond timing resolution [1], [2], [3]. As a result, SPAD devices have found applications in various fields requiring high-resolution weak light timing signals. These applications include direct time-of-flight single-photon imaging and high-performance LiDAR [4], [5], [6], [7], non-line-of-sight imaging [8], [9], [10], time-correlated quantum imaging [11], [12], [13], [14], long-distance free-space quantum communication [15], quantum key distribution [16], indoor light fidelity (LiFi) [17], Raman spectroscopy [18], [19], and fluorescence lifetime imaging microscopy (FLIM) [20], [21]. More recently, SPAD devices with low breakdown voltage have been developed for consumer products where low power consumption is crucial [22]. The low breakdown voltage SPAD not only results in low power consumption but also reduces breakdown emissions, minimizing the crosstalk effect in array image applications [23]. Additionally, the avalanche emissions can be utilized for high-performance CMOS microdisplay [23]. In optics, diffraction structures with pyramid surfaces, microlenses, and metasurfaces are typically employed [24], [25], [26], [27]. Moreover, there is an increasing focus on Terahertz-driven amplification of coherent optical phonons coupled to a metasurface [27] to enhance the photon detection probability (PDP) at near-infrared (NIR) wavelengths, which is typically low for a CMOS SPAD. In the context of LiDAR systems, lasers with NIR wavelengths are often utilized to address eye-safety concerns and ambient light considerations [28]. In addition to optical methods, the choice of carrier type for triggering avalanche events affects the resulting PDP value [29]. For instance, the electron-initiated multiplication process in n-on-p type SPADs yields a higher avalanche gain, enabling them to achieve a higher PDP at NIR wavelengths compared to p-on-n type SPADs with a similar breakdown voltage [30], [31]. Charge-focusing SPADs, which are based on the n-on-p type and feature backside illumination (BSI), have achieved an impressive PDP of 21.8% at a wavelength of 940 nm with a pixel size of 2.5 μm [32]. Simulation results also indicate significantly reduced timing jitter due to the improved mean time to breakdown when compared to the p-on-n SPAD design [33].

In our prior work [34], we introduced a design based on the n-on-p type structure with a deep-p-well (DPW) layer serving as the isolation layer which improves the limited operating excess voltage for an n-on-p design without any other customized well layer, in addition to improving the PDP as proposed [35], [36]. These SPADs were fabricated using the TSMC 0.18-μm high-voltage BCD CMOS technology without the need for any other customized well layer. They exhibited much lower dark count rates (DCR) and a higher PDP in comparison to the published n-on-p SPAD structures created with a standard CMOS process, without any custom layers [35], [36]. However, it's worth noting that the breakdown voltage slightly exceeded 30 V, and the circular layout had a suboptimal filling factor for applications involving high-array pixel configurations for consumer products [34].

In this letter, we introduce a modified structure design based on our previous work [34] that utilizes the existing layers of standard CMOS technology to achieve a low breakdown voltage and a high filling factor for n-on-p type SPAD. This approach improves upon the design presented in Ref. [50], [51], where the inclusion of the DPW layer necessitates additional space, thus reducing the filling factor.

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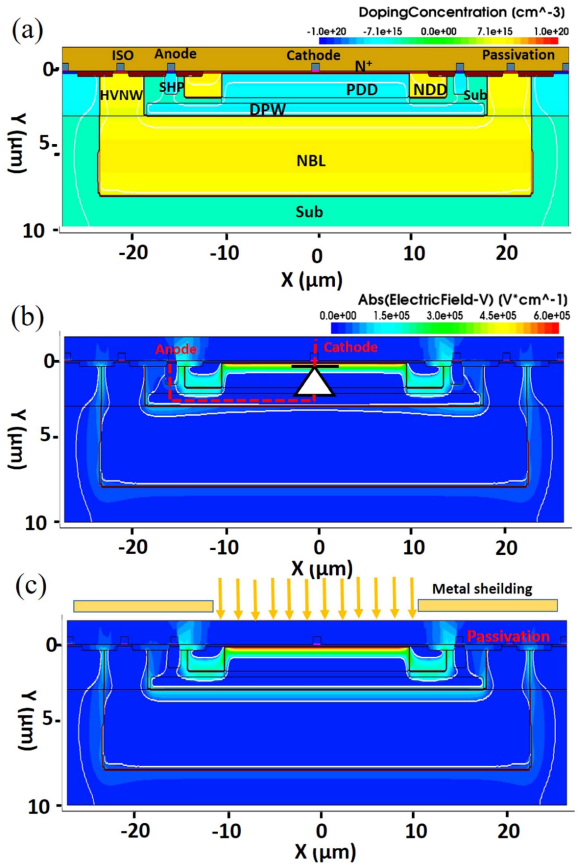

Fig. 1. (a) Cross sectional picture and (b) The electric field distribution of a reported n-on-p type SPAD structure was calculated at the breakdown voltage (18.2 V). A diode symbol was added in the active region (c) The electric field distribution was calculated at V_{ex}=15% with metal shielding and photon illumination direction.

II. Structure Design and Simulation

The chips were fabricated by TSMC, and we designed the devices using computer-aided software according to the design rules provided by TSMC. Base on general understanding of the process flow from the Process Design Kit (PDK) supplied by TSMC, aiding in the design structure for Synopsis Technology Computer Aided Design (TCAD) simulation, specific parameters such as depth and doping concentration were derived from material analyses based on our previous designs. In this work, all parameters used adhere to the standard TSMC 0.18um HV process. Therefore, this structure design for further circuit integration in various applications and seek chip fabrication services from TSMC. The device structure has been modified based on our previous work [34] to achieve a low breakdown voltage for the SPAD device, as shown in Fig. 1(a), was simulated by TCAD tools. Single or multiple Gaussian distribution doping profiles were used for the wells to match the doping profile and depth information obtained from the Secondary Ion Mass Spectrometer (SIMS) analysis. The n_plus/PDD well was used to create the active junction, with a guard-ring formed by the NDD well. In the simulation of electrical properties, the avalanche model (Okuto-Crowell model) was applied to determine the breakdown voltage, and the simulation was terminated when the current reached 100 μA [29], [30]. Thanks to the DPW layer acting as an isolation layer between the NDD well, which serves as the guard-ring of the active region, and the NBL layer, it provides a hole carrier conduction path to the cathode contact. Additionally, the lowest doping concentration well (substrate doping) functions as a low-resistance pathway for hole carrier conduction, maintaining a low peripheral electric field. So that The electric field strength in the active region reaches as high as $5x10^5$ V/cm, exceeding the critical field that can induce impact ionization in silicon (typically $2x10^5$ V/cm at a temperature of 300 K). The high doping PDD well is used to replace the low doping concentration HVPW as the active junction, reducing the breakdown voltage from over 30 V to 18 V. The electric field distribution when the device is biased at the breakdown voltage (18.2 V) is shown in Fig. 1(b). The SPAD is a diode with a pn junction designed to withstand ultra-high electric field operations. Structural features, such as guardring structures, are incorporated to prevent leakage currents and corner breakdown. To enhance understanding in the simulation, we have represented the SPAD using the diode symbol in Fig. 1(b). Additionally, to prevent photon carriers from being induced in areas far from the active region, a photon metal shielding has been applied around the device, as illustrated in Fig. 1(c).

A higher bias voltage above the breakdown voltage, referred to as the excess bias voltage (V_{ex}), expressed as a percentage of V_{br}, was simulated by deactivating the avalanche mode to examine whether the device could operate in Geiger mode. A V_{ex} equal to 15% was simulated and is shown in Fig. 1(c). In this case, the electric field is higher, and the depletion region is wider compared to Fig. 1(b). The electric field can increase with Vex, indicating that the device can operate in Geiger mode. However, during Geiger mode operation, an additional bias voltage beyond V_{ex} should be applied to the ISO contact to ensure the stable buildup of avalanche signals in the SPAD. This is demonstrated by the breakdown current distribution at the breakdown voltage in Fig. 2(a), where the ISO bias is set to 6 V, and it illustrates that the current remains confined to the active region. Without this additional bias, the breakdown current would conduct from the NBL layer to the substrate, leading to an unstable buildup of avalanche signals in the SPAD, as shown in Fig. 2(b).

III. Device Measurement Results

The current-voltage characteristics of the SPAD device under dark and illuminated conditions were measured using a Source Measure Unit (SMU) instrument (Keithley 2400) and are plotted in Fig. 3(a). The calculated IV curve from TCAD simulation is also shown in Fig. 3(a). In the simulation curve, there is a noticeable leakage current when the bias voltage is near V_{br}. As demonstrated in Fig. 3(b), even though the highest impact ionization occurs in the active region, the electric field strength in the active region can increase with V_{ex} beyond the V_{br}. This implies that the device does not suffer from corner breakdown, lateral junction breakdown, or electrical short circuits among junctions. The impact ionization distribution shows that there is a non-negligible effect in the guard ring and DPW layer.

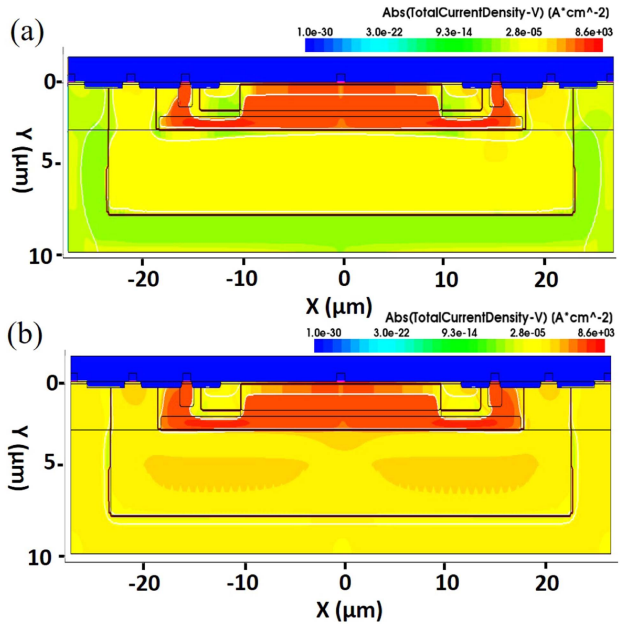

Fig. 2. (a) The current distribution was calculated with the ISO contact at a 6 V bias. (b) The current distribution was calculated with the ISO contact at a 0 V bias.

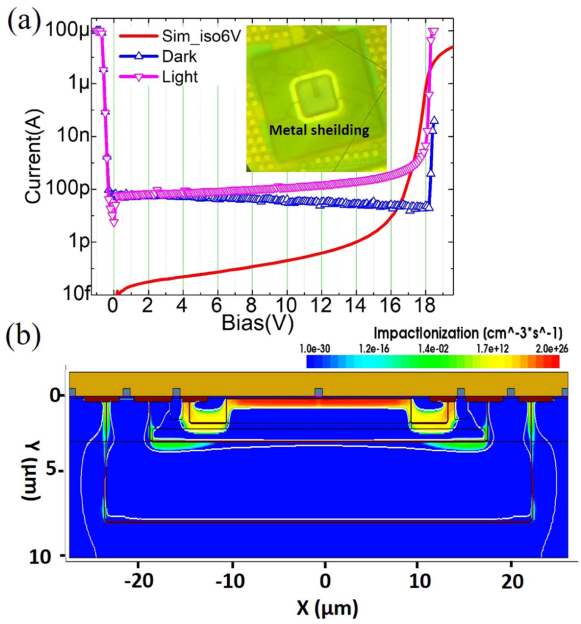

Fig. 3. (a) Dark, illuminated, and calculated I-V curves are shown. Inset: A top view of the device using an optical microscope (OM). (b) The impact ionization distribution was calculated at the breakdown voltage.

However, there is a clear distinction between the dark and illuminated IV curves. Even in the region above V_{br}, the more abrupt increase in current indicates low DCR and effective confinement of the high electric field region [52], [53]. We have adopted a rectangular active region layout design in addition to the circular layout used in previous work to improve the filling factor. As shown in the inset picture in Fig. 3(a), there are only slight blunted edges in a square pattern of 20 μm diameter.

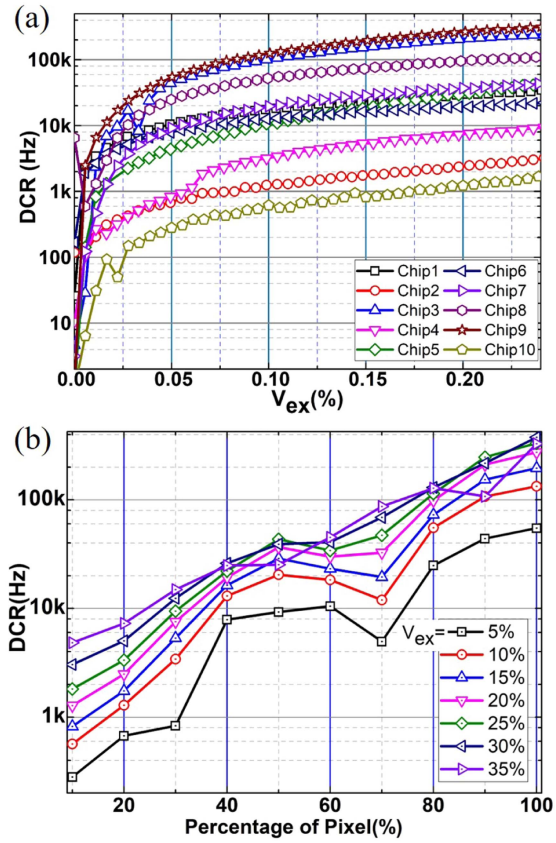

Fig. 4. (a) DCR measurement results versus excess bias for ten SPAD chips. (b) DCR measurement results versus excess bias distribution of the ten chips.

The SPAD device was mounted on a printed circuit board (PCB) containing a 100 kΩ passive quenching circuit (PQC), positioned between the voltage supply (GW6323) and the cathode. The DCR was determined by extracting avalanche signals through a 10 nF capacitor connected to a 50 Ω resistor between the anode and ground. The DCR was then recorded using a trigger frequency counting oscilloscope (GW 3235). The oscilloscope's trigger level was optimally adjusted to match the bias voltage.

The DCRs for ten chips were recorded as a function of excess bias and are presented in Fig. 4(a). Most chips exhibited a DCR value below 40k Hz (100 cps/μm^2) at $V_{ex} = 35\%$, which outperforms previous reports [50], [51]. It should be noted that there was a significant range of DCR variation among the ten chips. Some chips exhibited much higher DCR values, especially at the initial bias, which is referred to as the sub-Geiger mode. All the chips exhibited similar trends in DCR with V_{ex}. We believe that this variation may be attributed to the blunted edges of a square pattern, in addition to the circular layout for high filling factor design. The higher electric field at the corners may induce increased tunneling effects. Even though the V_{br} was designed to be much lower, it still leads to higher tunneling effects and consequently higher DCR, as compared to the 30 V V_{br} in our previous work. Due to sharing the area with another project and the utilization of a multi-project wafer (MPW) for chip tapeout, we measured the DCR of only 10 chips. However, having more

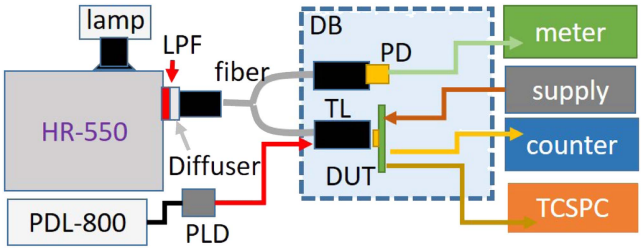

Fig. 5. Schematic of the SPAD parameter measurement demonstration. Our modifications: LPF, long pass filter; PLD, picosecond laser diode; DB, dark box; PD, calibrated photodiode; TL, telecentric lens; DUT, device under test; TCSPC, time-correlated single-photon counter.

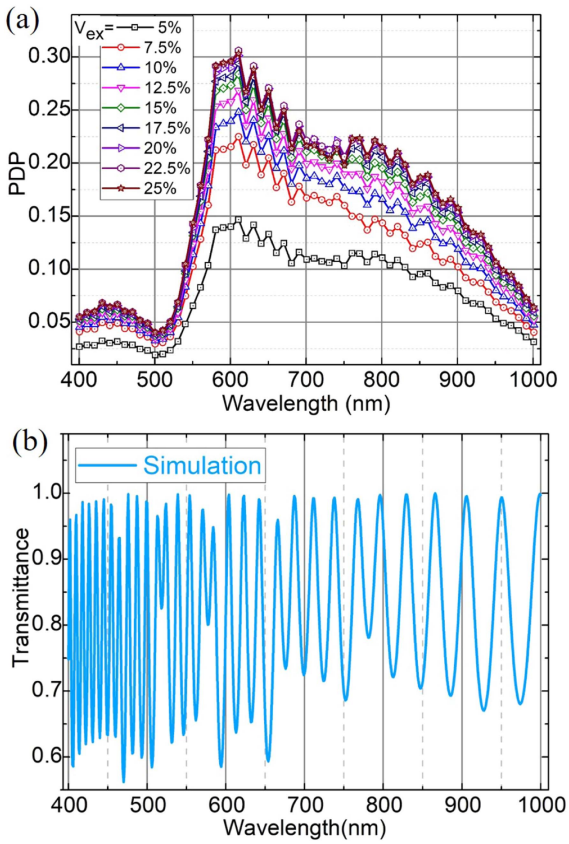

Fig. 6. (a) PDP measurement results versus wavelength for various V_{ex}, (b) optical simulations of the reflectance of the passivation layer.

than 10 chips would be beneficial for analyzing the fluctuation in the DCR distribution.

Although the DCR is not exceptionally low, it is not a significant issue in Lidar applications employing direct time-of-flight technology. DCR can be averaged over time bins, and 10 kHz DCR corresponds to 1 signal for every 10000 bins in a time-to-digital converter circuit.

A broadband light source (Halogen lamp) disperses light into various wavelengths through a monochromator and is then split into two output fibers. A diffuser is employed in front of a lens to collimate the light, and a glass light tunnel and a telecentric lens are used in the setup. One of these fibers is used to illuminate the device under test (DUT), while the other is directed towards a calibrated photodiode (FDS1010-CAL) for PDP measurement. This arrangement aims to prevent coupling loss and achieve uniform illumination. However, reflections may arise due to interference from the passivation layer. This layer is formed with multilayer dielectric materials, such as SiO_2 and Si_3N_4, used to isolate various metal layers beneath the chip through CMOS technology. This phenomenon leads to wavelength-dependent fluctuations in the PDP measurement spectrum [38].

To measure light with a wavelength exceeding 700 nm, a long-pass filter is employed to block second harmonic reflections from the monochromator. The photon current from the calibrated photodiode is measured using a semiconductor parameter analyzer (HP 4145b), and the output signal from the SPAD is registered by an SR-400 photon counter. The schematic of the SPAD parameter measurement demonstration is presented in the Fig. 5. To ensure an accurate measurement and to account for the recharging time of the passive quenching circuit (approximately 5 μs), the incident power is maintained at a low level to limit the photo-counts to no more than 100 kHz. Subsequently, the PDP is calculated by taking the ratio of photocounts measured from the SPAD to the photon count derived from the photodiode. This PDP is plotted as a function of wavelength, as illustrated in Fig. 6.

The PDP represents the probability of an incident photon triggering an avalanche breakdown, where the carrier trigger probability increases with V_{ex}. In higher CMOS technology nodes, more metal layers are employed, resulting in reduced photon transmittance through the passivation layers. Therefore, optical design methods, such as nanostructure implementation [39], should be considered to enhance device performance. In this study, passivation on the top of the chip and the silicide layer, which not only reduces photon transmittance but also increases the DCR of the device [40] in the active region of SPAD, has been removed through layout design to improve the photon transmission rate. Thickness and index information from the Process Design Kit (PDK) were utilized for photon transmittance calculations. The optical simulations of the reflectance of the passivation layer to clarify the oscillations observed in the PDP measurement spectrum results [38], [41], [42].

The peak PDP exceeds 30% at a wavelength of 600 nm for $V_{ex} = 25\%$, which is higher than in our previous work. Moreover, there is a PDP exceeding 15% in the NIR wavelength range, which is significantly higher than our previous work. This improvement may be attributed to the broader depletion region with a high vertical and lateral electric field, leading to a higher trigger probability [37] compared to our previous work [34], as indicated in the TCAD simulation results plotted in Fig. 1.

A low repetition rate operation (32 kHz) picosecond laser at a wavelength of 780 nm (PicoQuant LDH P-C-780) is employed to measure the jitter. The laser signal and the output signal from the SPAD respectively serve as the start and stop signals for the PicoHarp 300 Time Correlated Single Photon Counting (TCSPC) module, which offers a timing bin resolution of 4 ps. To measure weak light with long integration time jitter and to prevent the pile-up effect [54], a 100x neutral density (ND) filter is used. Pile-up effects can distort the timing distribution of

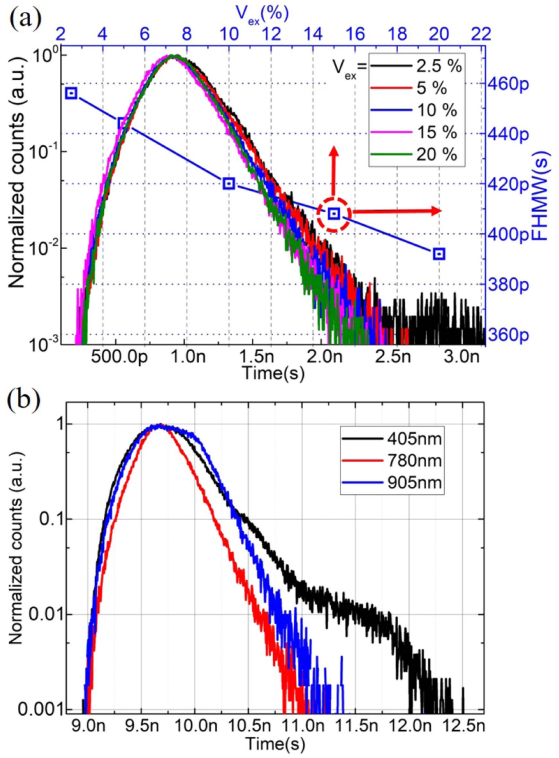

Fig. 7. (a) Timing distribution for various V_{ex} values measured with a 780 nm picosecond laser and the full width at half maximum (FWHM) value of the timing distribution versus V_{ex} is plotted with a blue curve .The corresponding axes are respectively on the right and upper sides. (b) The timing distribution was also measured with 405 nm, 780 nm, and 905 nm at $V_{ex} = 15\%$.

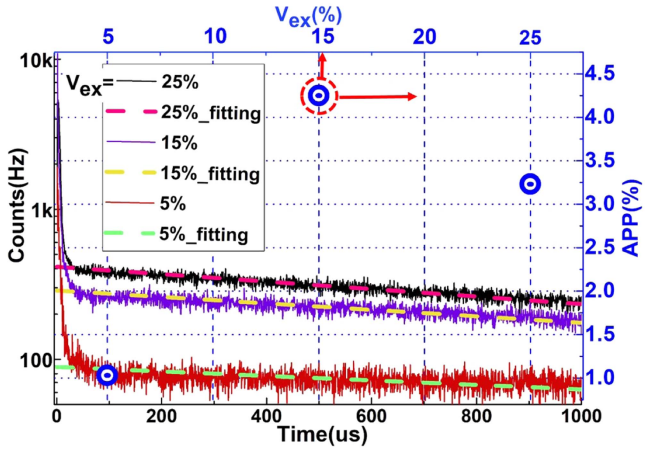

Fig. 8. Time histogram of the APP measurement using the TTTR method and the corresponding axes of the IAT fitting curve for various values of V_{ex} are respectively on the right and upper sides.

the SPAD. The timing distributions for different V_{ex} values are shown in Fig. 7(a), and the full width at half maximum (FWHM) of each curve is plotted as a function of V_{ex}, indicated by the blue curve in Fig. 7(a).

We used various wavelengths of picosecond lasers to examine the different electric field distributions at various depths of the device. The device exhibited the largest jitter value when subjected to the 405 nm wavelength, commonly used in FLIM applications [43], [44], and the 905 nm wavelength, commonly used in automotive Lidar applications [45], [46], also showed a significantly larger jitter value compared to the 780 nm wavelength, commonly used in pulsed Lidar imaging and high spectral resolution Lidar applications [47], [48], [49], as shown in Fig. 7(b).

The after-pulsing probability (APP) of the SPAD limits the maximum count rate for Lidar applications. Even if the device maintains a high PDP, the APP value must be considered, as a high APP value renders the detector unsuitable for high-count rate applications. In APP measurements, we adopted the Time-Tagged Time-Resolved (TTTR) mode in the TCSPC instrument. The SPAD device's DCR signal was connected to channel 1 of the TCSPC instrument with varying V_{ex} values, and TTTR measurements were conducted with a one-thousand-second integration time. By comparing the inter-arrival times (IAT) of events in a one-thousand-second TTTR measurement, we calculated the APP value. As the DCR generated from thermal effects should follow a Poisson distribution, in timing-correlated measurements, the APP value can be determined by summing up the non-Poisson distribution counts to obtain the total counts, as depicted in Fig. 8 [55], [56], [57]. The measured APP value is 0.8% and 4.2% at $V_{ex} = 5\%$ and $V_{ex} = 15\%$, respectively. While the APP value of our SPAD is somewhat elevated at high V_{ex}, there are methods for improvement, such as utilizing a higher quenching resistor [58] or integrating a fast quenching circuit with the SPAD on-chip [59], [60], [61] to reduce the avalanche current.

IV. Performance Summary and Comparison

The performance of the low V_{br} n-on-p type SPAD is summarized in Table I, and a comparison is made with recent literature, including n-on-p and p-on-n type SPADs. Based on our previous work, we added a p-type well with a higher doping concentration layer, which is the standard p-type layer in the TSMC 0.18 HV technology. This modification successfully reduced the V_{br} from 30.8 V to 18 V. Additionally, with the layout design, the device's filling factor has significantly improved in the array application. Furthermore, the PDP has improved from 2% to 15% at the detection wavelength of 905 nm. Therefore, our proposed device design is much more suitable for consumer three-dimensional LiDAR applications. While the low V_{br} SPAD device exhibits a higher DCR compared to our previous work, it achieves significantly higher PDP values in the NIR wavelength range. However we believe that the higher DCR should come from the layout design for obtuse angle at the edge replace with the circle layout design which used in the previous work for demonstrates a higher filling factor in the array architecture. The propose low V_{br} SPAD design exhibits a much higher PDP at the NIR wavelength (900 nm), commonly used in automotive LiDAR, with a notably low DCR compared to other reported n-on-p type SPADs. In addition to the high PDP at the NIR wavelength, our proposed low V_{br} SPAD design maintains a low APP even at much higher V_{ex}. This feature enables the LiDAR system with our proposed device design to operate effectively in high ambient conditions compared to other works. Furthermore, it

TABLE I
COMPARISON OF THIS WORK TO THE RECENT LITERATURE

Ref., Year	Tech (nm)	Junc.	V_{BR} (V)	DCR / V_{ex}(cps/μm^2)/ (%)	PDP (%) [nm]	APP / V_{ex} (%)/(%)
[50] 2013	65	N^+ / Pwell	9.1	15.6 k @ 4.4	~0.4 [900]	1 @ 4.4
[51] 2022	180	N^+ / Pwell*	12.1	629 @ 4.1	~2.4 [900]	4.9 @ 4.1
[62] 2021	65	N^+ / Pwell	9.52	138k @ 3.1	~0.1 [900]	< 1 @ 3.1
[63] 2020	180	P^+ / Nwell	11.6	6.34 @ 8.7	-	-
[63] 2020	180	P^+ / Nwell*	11.4	2.37 @ 8.7	-	-
[64] 2015	180	P^+ / Nwell	14.6	16 @ 27	~9 [850]	0.2 @ 27
[65] 2019	180	P^+ / Nwell	16.8	3.86 @ 30	~22 [700]	-
[58] 2018	180	N^+ / Sub	12.1	23.5 @ 4.1	~1.1 [800]	-
[58] 2018	180	P^+ / Nwell	11.2	965 @ 4.5	~0.1 [800]	-
[34] 2023	180	N^+ / Pwell	30.8	6.48 @ 20	3 [900]	7.5 @ 8.5
This work	180	N^+ / Pwell	18.2	90 @ 20	15 [900]	4.2 @ 15

- The * mark means the structure with poly-gate depletion design

can even compete with a p-on-n type SPAD that incorporates a customized n-well and DCR suppression design.

The low breakdown voltage of the SPAD device with CMOS technology maintains the advantage of low power consumption in array applications, such as the three-dimensional range finder in this work. However, the presence of the isolation layer is necessary to prevent a short in the active region with the NBL layer, resulting in a low filling factor for this device. In this study, we have employed the square layout design to replace the circular layout used in our previous work to improve the filling factor. Nevertheless, various layout methods can still be explored further in array chip design, such as the shared well method [66], [67], [68].

V. CONCLUSION

We employed the TSMC 0.18 μm high voltage bipolar-CMOS-DMOS (HV BCD) process without any additional customized layers to design a low breakdown voltage n-plus on the PDD well SPAD structure. This structure exhibits a high PDP in the near-infrared (NIR) wavelength range with a relatively low DCR. As a result, the device is suitable for consumer product applications, such as sensor-electronics 3D integration, enhancing performance in LiDAR and high-energy physics imaging. The n-on-p well technology is utilized to create a backside-illuminated (BSI) chip for direct time-of-flight (d-TOF) 3D imagers [5], [7]. This structure offers higher PDP at NIR wavelengths compared to a p-on-n type SPAD. Furthermore, through the design of blunted edges in a square pattern layout, the device can achieve a high filling factor in array design. In addition to the layout design in this study, for achieving a higher filling factor and increased PDP at NIR wavelengths, backside-illuminated and three-dimensional stack technology can be employed with CMOS technology. Our work offers device design support for the development of applications [69], [70], [71].Although there is a broad range of DCR values from very low to slightly higher, we believe that refining the guard ring design in the corners will resolve this issue.

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