Large Active Area, Low Capacitance Multi-Dot PIN Photodiode in 0.35 μm CMOS Technology

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***Abstract*—This article presents a multi-dot PIN photodiode structure that addresses the inherent trade-off between the light-sensitive area and capacitance in conventional planar photodiodes commonly used in optical communication systems. This structure is a combination of several connected cathode dots and with a shared anode. The radial distribution of the electric field surrounding each cathode dot facilitates both vertical and peripheral charge collection, and accordingly, enables the region beneath and between the dots to function as a light-sensitive area with fast carrier drift. The key innovation of this work lies in the flexibility of the multi-dot structure for easy enlargement of the light-sensitive area by expanding the dot array, while still maintaining a small capacitance. Experimental results show that a 5 $\times$ 5 multi-dot PIN photodiode with a pitch of 20 μm corresponding to an active area of 100 μm $\times$ 100 μm achieves a capacitance of 48.8 fF, a responsivity of 0.294 A/W at a wavelength of 675 nm, and a bandwidth of 660 MHz at an operating voltage of 10 V. With a pitch of 15 μm that provides a light-sensitive area of 70 μm $\times$ 70 μm, the bandwidth increases to 930 MHz.**

***Index Terms*—CMOS, multi-dots photodiodes, light-sensitive area, low capacitance, PIN photodiodes, peripheral charge collection.**

I. Introduction

To ATTAIN high bandwidth, high transimpedance, and low noise in optical sensors and receivers, it is essential to have a photodetector with a small capacitance [1]. In image sensor pixels, there are photodiodes with an exceptionally low capacitance [2], [3], [4]. These photodiodes typically exhibit a capacitance in the order of femtofarad when employed in a small light-sensitive area of around 1 μm^2. However, many applications of optical sensors require a larger light-sensitive area to enable efficient coupling of the light signal to the photodiodes [5], [6]. The capacitance of P/N junctions in photodiodes shows a direct relationship with the photodiode's area [7]. As a result, expanding the sensitive area necessitates an increase in the size of the P/N junction, subsequently leading to an increase in the junction's capacitance. This trade-off between capacitance and detection area is commonly observed in planar photodiodes. Hence, it becomes necessary to decouple the P/N junction area from the light-sensitive area in order to achieve a larger light-sensitive region without simultaneously increasing the capacitance. This decoupling can be achieved by implementing lateral depletion techniques.

Photodiodes based on finger structure have been proposed to achieve low capacitance [8], [9], [10]. In [10] by employing a lateral PIN diode configuration with one N+ finger positioned between two P+ stripes in silicon, they could achieve a capacitance value of approximately 6 fF for a 30 $\times$ 30 μm^2 diode. However, these photodiodes offer a responsivity and bandwidth of 0.45 A/W and 110 MHz, respectively, at a wavelength of 660 nm and a reverse-bias voltage of 4 V. A further capacitance reduction can be achieved by shrinking the cathode finger to a cathode dot.

[11], [12], [13] presented spot and dot PIN photodiodes with a capacitance down to 1.14 aF/μm^2. These photodiodes possess a small hemispherical cathode dot in a thick low-doped epitaxial layer and a vertical plus radial electric field to collect lateral charge carriers from the whole diode volume towards the cathode. Capacitances down to 0.8 fF have been achieved at a light-sensitive area of 706.9 μm^2. A responsivity of 0.38 A/W and and bandwidth of 310 MHz, at a wavelength of 635 nm and and a reverse-bias voltage of 30 V are achieved for such structures.

It is worth noting that in this configuration, the active region cannot be excessively enlarged due to the gradual decrease in the electric field as the radial distance from the center increases. Consequently, at large distances away from the center, the electric field becomes too weak to effectively drive carriers [14], [15]. In [16] we introduced an n+/p-well dot avalanche photodiode in 0.35 μm CMOS technology to enhance area and bandwidth. The APD was baised at an operating voltage of 24 V.

In this article, we present a multi-dot PIN photodiode structure based on the very low capacitance single-dot PIN photodiode, which can provide a large active area with low capacitance. The motivation of this is to increase the light-sensitive area of the photodiode compared to that used in ref. [12], where an ultra-sensitive optical receiver with a single-dot pin photodiode with a light-sensitive area of 706 μm^2 was introduced. In receivers exploiting the principle of capacitive-feedback transimpedance amplifiers like in [12], the low capacitance of the photodiode is essential for achieving best sensitivities. A capacitance of 48.8 fF is achieved for a 5 $\times$ 5 multi-dot PIN photodiode with an active area of 100 μm $\times$ 100 μm. Additionally, this

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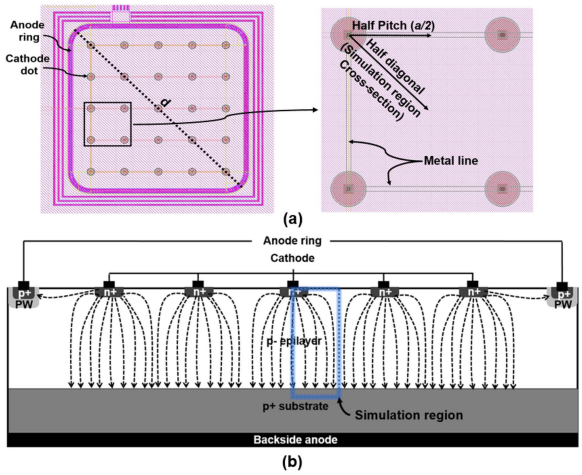

Fig. 1. (a) Top view of layout drawn in Cadence of the 5 × 5 array MD-PIN photodiode. Right is a zoomed top view of a cathode dot adjacent to other cathode dots in the array. (b) is a schematic cross-section (not to scale) of the MD-APD along the dotted line (d) in sub-figure (a-left).

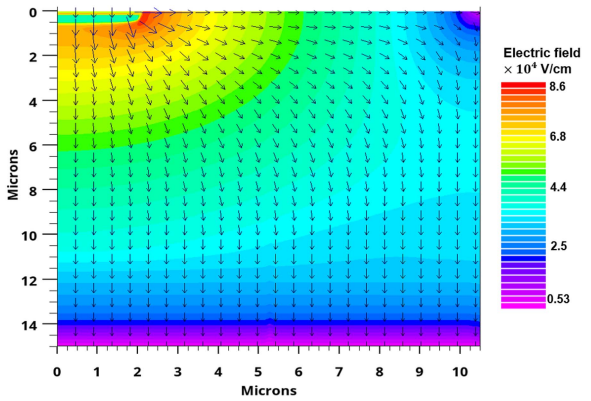

Fig. 2. (a) 2D plot of the simulated electric field distribution in the 2D cross-section indicated in Fig. 1(a) (right) with a half diagonal of 10.5 μm (i.e., a = 15 μm) at an operating voltage of 10 V. Arrows represent the local electric field direction.

photodiode demonstrates a responsivity and bandwidth of 0.294 A/W and 660 MHz, respectively, at a wavelength of 675 nm and a reverse-bias voltage of 10 V. Moreover, the active area can be readily expanded by enlarging the dot array while maintaining a small capacitance. Section II presents the device structure and design approach. In Section III experimental characterizations are discussed, and Section IV concludes the article.

II. Device Structure and Design Approach

Fig. 1 illustrates the top view (a) and a 2 d schematic cross-section (b) of the multi-dot (MD) PIN-photodiode structure. The MD-PIN configuration comprises an array (5 × 5) of semi-hemispherical high-doped n+ regions with a radius of 2 μm as cathode dots, which all are connected with tracks in metal layer 4 with a minimum width of 0.6 μm as shown in Fig. 1(a). The cathode dots are embedded in a lightly p-doped epitaxial layer (p-epi) with a doping concentration of $\sim 2 \times 10^{13}$ cm $^{-3}$ and a thickness of $\sim$12 μm. This cathode array is surrounded by a surface anode ring that defines the overall diode size. The p+ substrate serves as a shared backside anode. It should be mentioned that the MD-PIN photodiode is fabricated in the 0.35 μm CMOS modular optical sensor technology platform (XO035) of X-FAB semiconductor foundries without any process modification because this technology is a pin-photodiode process.

The electric field distribution inside the structure is studied using TCAD simulations with ATLAS [17]. It is important to emphasize that a 3 d simulation would be necessary to accurately model the entire structure of the MD-PIN configuration requiring a huge number of grid points and unacceptably long computation time. Nevertheless, a 2 d simulation focusing on a cross-section that features a half-cathode dot positioned at the corner of a half-pitch-wide region (see Fig. 1(a) (right)) can still provide valuable insights and reliable performance estimations because of symmetry reasons and boundary conditions of the simulator.

Fig. 2 shows a 2d plot of the electric field for the 2d cross-section region indicated in Fig. 1(b) by a blue rectangle at an operating voltage of 10 V (breakdown voltage = 63 V). It can be seen that, unlike planar structures that possess solely a homogenous vertical electric field, MD-PIN photodiodes feature an electric field that extends radially throughout the diode, which can be used for vertical and peripheral charge collection. When the diode is reversely biased, a spherically uniform high electric field is formed around each cathode dot, and a weaker (but still high) electric field extends radially throughout the diode to guide charge carriers from the entire diode volume towards the cathode dots.

Therefore, the region under and between all cathodes acts as a detection zone. When a photon is absorbed in these areas, the generated electron-hole pair is instantly separated by the electric field (see the field lines in Fig. 1(b)), causing them to drift in opposite directions. Then, the electron is effectively guided towards a respective cathode dot based on the local electric field direction, even that generated in the periphery between the cathode dots. This unique feature is attributed to the existence of the lateral component of the electric field. Thus, the entire diode area, including the spaces between cathode dots, functions as an extended detection zone. This characteristic significantly contributes to achieving a large light-sensitive area and efficient peripheral charge collection.

In addition, the capacitance of the MD-PIN photodiode is expected to be low because of the small areas of the p/n junctions. In fact, the total capacitance is the sum of the capacitance of all cathode dots in the array plus parasitic capacitance (of metal tracks).

It is worth knowing that the active area of the MD-PIN photodiode can be readily expanded by enlarging the cathode dot array. This can be achieved by increasing the number of cathode dot arrays or by adjusting the distance between the cathode dots, known as the array's pitch size. However, it is important to note that different array pitch sizes lead to different electric field distributions inside the structure. Fig. 3 shows a radial (at the surface) and a vertical (at r = 0) cross-sections of the electric field in the simulation region indicated in Fig. 1(b)

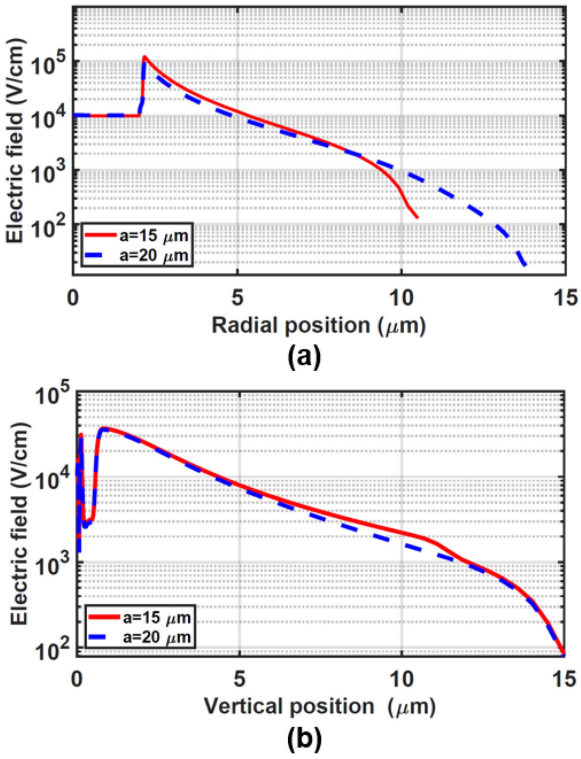

Fig. 3. (a) Radial (at the surface) and (b) vertical (at r = 0) cross-sections of the electric field in the simulation region indicated in Fig. 1 for two different pitches of $a = 15$ μm and $a = 20$ μm at an operating voltage of 10 V.

for two different pitches of $a = 15$ μm and $a = 20$ μm. It can be observed that the strength of the electric field within the detection zone decreases as the pitch size increases. Accordingly, it is crucial to optimize the pitch size of the array as it is a significant parameter that directly impacts the overall performance of the photodiode.

If the cathode spots in the MD-PIN photodiode are spaced too far apart, it can result in an insufficient electric field across the entire area between two cathodes to drive the photo-generated carriers towards the cathode spot as the electric field gradually decreases by moving away from the cathode dots' center reducing the drift velocity. Therefore, it is inaccurate to consider the entire area between two cathode spots as the detection zone when the dots are widely spaced. Furthermore, increasing the pitch size of the cathode dot array leads to a lower device's speed. This is attributed to the fact that the response speed is determined by the transit time required for photogenerated electrons to reach the cathode. The transit time relies on both the carrier drift distance and the drift velocity, which is influenced by the local electric field strength. In MD-PIN photodiodes with a larger array pitch size, the transit time is expected to be longer. This is due to the increased carrier drift distance and the weakened intensity of the electric field over the greater distance from the cathode spots (see Fig. 3(a)). An additional point that should be taken into account is that the slowest response occurs when a photon is absorbed exactly in the center between four cathode dots because it corresponds to the longest drift distance along the

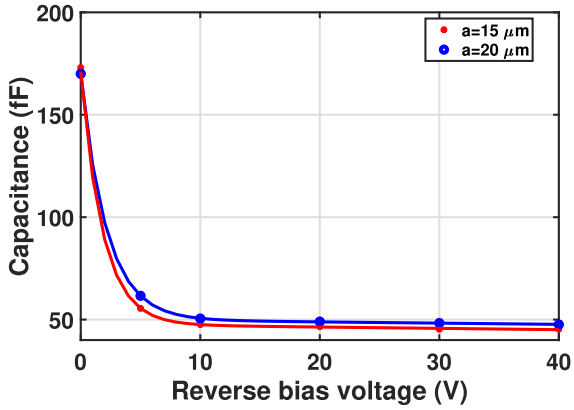

Fig. 4. Measured capacitance of the MD-PIN photodiodes as a function of reverse bias voltage.

silicon surface. The maximum lateral drift distance is calculated as $\frac{a}{\sqrt{2}}$, where a represents the pitch of the array.

Conversely, when the distance between neighboring cathodes in the MD-PIN photodiode is small, a greater number of cathode dots are required to achieve the same active area compared to an MD-PIN photodiode with larger pitch sizes. This increase in cathode dots results in a higher capacitance for the MD-PIN due to the cumulative effect of capacitance from each individual dot in the array. Moreover, MD-PIN photodiodes with small pitch sizes necessitate more metal lines to connect the cathodes, leading to a larger parasitic capacitance. Furthermore, as the pitch size decreases, a larger portion of the detection zone becomes covered by opaque metal. Consequently, this region can no longer be considered an absorption region since incident photons are reflected by the metal before reaching the silicon. Therefore, it is imperative to optimize the pitch size of the array based on the specific requirements of the intended application. TCAD simulation can be employed to determine the optimal array pitch size for the MD-PIN configuration.

III. Experimental Characterizations

In this section, the characterization of MD-PIN photodiodes, consisting of an array of 5 × 5 cathode dots with two different pitches, a = 15 μm and a = 20 μm, is presented. The active area of the photodiodes is 70 μm × 70 μm and 100 μm × 100 μm, respectively. These photodiodes were fabricated using the 0.35 μm CMOS modular optical sensor technology (XO035) provided by X-FAB semiconductor foundries. Key performance characteristics including responsivity, frequency response, and capacitance are examined. A comparative analysis is conducted between the two structures to assess the impact of the array's pitch size.

A. Capacitance

Fig. 4 depicts the capacitance characteristics of the MD-PIN photodiode, which were measured using an LCR meter (Agilent 4284 A) at various reverse bias voltages.

The measurements were performed at a frequency of 1 MHz with an AC amplitude of 100 mV. To account for the influence

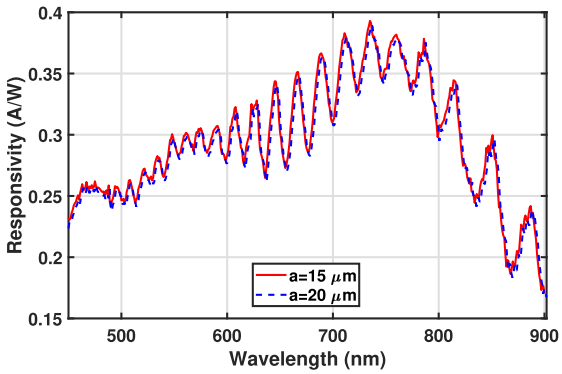

Fig. 5. Measured spectral responsivity of MD-PIN photodiodes with two pitch sizes of a = 15 μm and a = 20 μm at an operating voltage of 10 V.

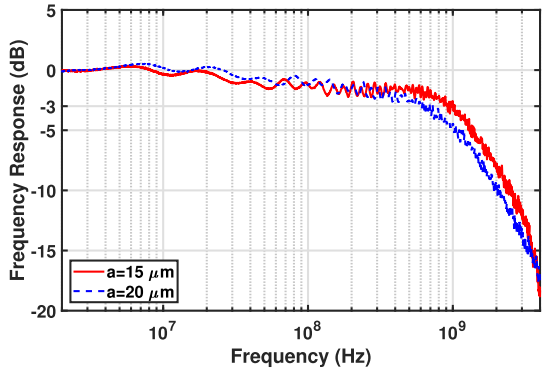

Fig. 6. Normalized frequency responses of MD-PIN photodiodes with two pitch sizes of a = 15 μm and a = 20 μm at an operating voltage of 10 V.

of pad capacitance and measurement cables, a calibration was conducted using an open structure on the same wafer, which had the same pad size and metal track outside of the MD-APD. The total capacitance of the MD-APD comprises the capacitance of the p-n junctions of each individual cathode dot and the parasitic capacitance of the metal tracks employed for interconnecting the cathode dots. The initial high capacitance of 170 fF at zero voltage primarily arises from the junction capacitance of the cathode dots. As the reverse bias voltage increases, the capacitance exponentially decreases to 46.3 fF and 48.8 fF at 10 V reverse bias for the MD-PIN photodiodes with a = 15 μm and a = 20 μm, respectively. The observed capacitance is similar for both structures since they possess an equal number of cathode spots. However, the structure with a pitch size of 15 μm exhibits a slightly lower capacitance, which can be attributed to the reduced parasitic capacitance resulting from the shorter metal paths connecting the cathode spots.

B. DC Characterization

The photodetection characterization of MD-PIN photodiodes with different pitch sizes (a = 15 μm and a = 20 μm) was conducted, as depicted in Fig. 5. For this purpose, a Digikrom CM110 monochromator was utilized to sweep the wavelength range from 400 nm to 900 nm in 1 nm increments. An optical attenuator was employed to maintain consistent optical power. The light was directed to the sample under test through a multi-mode fiber with a core diameter of 62.5 μm. To measure the current and supply the voltage, a Keysight B2987 electrometer was utilized.

Both structures exhibit nearly identical responsivity as the spotlight size (diameter= 62.5 μm) is smaller than the active area of both photodiodes. This ensures that the entire light is irradiated onto the active area, allowing all incident photons to be detected. Furthermore, despite the smaller electric field in the photodiode with a larger pitch size (a = 20 μm), there is a high enough electric field under and between the cathode dots (see Fig. 3) to guide the photogenerated carriers towards the cathode dots. However, the carriers' transit time will be longer, which will affect the speed of the device. A responsivity of 0.294 A/W is obtained at an operating voltage of 10 V for a wavelength of 675 nm, resulting in a quantum efficiency of approximately 54%. The maximum responsivity of 0.393 A/W is present at 735 nm. It should be noticed that in this technology, the entire surface of the photodiode is coated with a thick isolation oxide and a passivation stack. Consequently, incident photons must traverse these layers before reaching the silicon. Due to variations in the refractive indices of these distinct layers, a fraction of the incident photons undergo reflection at each interface. The interplay of multiple reflections of light at the interfaces of the isolation-oxide and passivation stack generates a standing wave, leading to fluctuations in the transmission profile as demonstrated in the spectral responsivity. However, some CMOS technologies provide a module of opto-window, in which the passivation and isolation stack over the photosensitive area is removed and a layer of ARC is deposited on the silicon. This can reduce the reflection and suppress the fluctuations in the spectral responsivity.

C. Frequency Response

The frequency responses were evaluated using a Rohde & Schwarz vector network analyzer ZNB8. The light from a 675 nm laser, with an average optical power of 200 μW, was coupled into the dot PIN photodiodes using a 62.5 μm multi-mode fiber. Photocurrents generated by the photodiodes were measured using a 50-ohm ground-signal probe connected to the 50-ohm input of the vector network analyzer through a Picosecond 5530B bias-tee (20 kHz-12.5 GHz).

Fig. 6 presents the measured frequency responses of MD-PIN photodiodes with different pitch sizes. The bandwidths of 660 MHz and 930 MHz are achieved for the MD-PIN photodiodes with pitch sizes of 20 μm and 15 μm, respectively. The results highlight that reducing the distance between cathode dots leads to higher bandwidth. This improvement can be attributed to the reduction in electron drift time, which is achieved by shortening the radial carrier drift distance and increasing the electric field strength across the detection zone.

In fact, the frequency response is determined by the transit time required for photogenerated electrons to reach the cathode. This transit time depends on both the carrier drift distance and the drift velocity, which in turn is directly influenced by the local electric field strength. Consequently, the MD-PIN photodiode with a larger array pitch size is expected to exhibit a higher

transit time due to the increased carrier drift distance and the weakened intensity of the electric field over the greater distance from the cathode dots. Conversely, reducing the pitch size brings the cathode dots closer, thereby shortening the radial carrier drift distance and intensifying the electric field strength throughout the detection zone. This reduction in drift time due to a shorter radial carrier drift distance and the heightened electric field strength contributes to achieving higher bandwidth.

The bandwidths of 660 MHz an 930 MHz observed at only 10 V reverse voltage are much larger than those of 520 MHz at 15 V as well as 300 MHz at 30 V of the spot and dot PIN photodiodes of [11], [13], respectively, mainly due to the thinner epitaxial layer (12 μm instaed of 24 μm). However, it is important to note that further reducing the distance between cathode dots does not provide significant additional bandwidth improvement. This is because in smaller structures, the half diagonal distance between two cathode dots, which represents the maximum radial drift path, becomes smaller than the depth of the structure (12 μm), and the vertical transition of carriers from this deep region limits the overall bandwidth. As a result, reducing the cathode dot distance beyond a certain point has a diminished impact on the bandwidth.

IV. Discussion and Comparison

The proposed MD-PIN photodiode, featuring a responsivity of 0.29 A/W and a bandwidth of 660 MHz at $\lambda = 675$ nm with a capacitance of 48 fF for an active area of 100 μm $\times$ 100 μm, demonstrates its efficacy in applications requiring low capacitance and moderate bandwidth. To provide a comprehensive perspective, we compared the MD-PIN with several commercially available silicon photodiodes. The high-speed photodiode from OSI Optoelectronics [18], with a responsivity of 0.36 A/W and a bandwidth of approximately 900 MHz at $\lambda = 850$ nm, exhibits a higher capacitance of 660 fF for an active area diameter of 150 μm. Meanwhile, the photodiode from Thorlabs [19], boasting a responsivity of 0.35 A/W and a rise/fall time of 35 ps/200 ps at $\lambda = 740$ nm, maintains a capacitance of 650 fF for the same active area diameter. Conversely, the photodiode from Hamamatsu [20] provides a significantly higher responsivity of 0.63 A/W, although with a limited bandwidth of 80 MHz at $\lambda = 870$ nm, and a substantially larger capacitance of 5 pF for an expansive active area of 880 μm $\times$ 880 μm.

To compare to a vertical pin photodiode with a single cathode having an area of 100 $\times$ 100 μm^2, we performed device simulations with ATLAS for the same fabrication process as it was used for the MD pin photodiodes. The -3 dB bandwidth obtained for 10 V reverse bias and 675 nm wavelength is 1.09 GHz and the capacitance of such a pin photodiode is 120 fF.

In addition, the ability to scale our photodiode to larger dimensions is an exciting avenue that underscores the versatility and potential of the multi-dot design. Changing the 5 $\times$ 5 photodiode array to a larger size comes with both opportunities and challenges. On one hand, increasing the array size while maintaining the number of cathode dots allows for more extensive light collection and potentially higher responsivity. This means that the photodiode can capture more incident photons, making it suitable for applications requiring enhanced light sensitivity.

However, the implications of scaling the array also involve certain considerations. As the size of the array increases, the spacing between individual cathode dots has to be increased. Maintaining the proper pitch size, however, is essential to ensure an optimal electric field distribution across the photodiode's active region. As we have discussed in Section II, different pitch sizes lead to variations in the electric field distribution, which can impact the photodiode's performance. It is crucial to balance the benefits of a larger light-sensitive area against the challenges posed by capacitance, response speed, and electric field strength.

Additionally, increasing the number of cathode dots while scaling to a larger array size can raise concerns related to capacitance. Larger cathode arrays may accumulate a higher cumulative capacitance, which can affect the whole optical sensor's bandwidth and response speed. Moreover, larger arrays with smaller cathode dots may necessitate an increased number of metal lines for interconnection, potentially leading to a larger parasitic capacitance.

To address the implications of scaling our MD-PIN photodiode to larger dimensions, we recommend a systematic analysis and optimization. This should include thorough TCAD simulations to determine the optimal pitch size, cathode dot size, and metal interconnection strategies to maintain the desired performance characteristics.

In summary, scaling the 5 $\times$ 5 array to larger dimensions presents exciting possibilities for our MD-PIN photodiode, but it also requires careful consideration and optimization to balance the advantages of enhanced light collection with the challenges related to capacitance, speed, and electric field distribution.

It is worth noting that while our current work is primarily focused on the dot photodetector concept implemented in silicon there is a strong possibility for this concept to be extended to other semiconductor materials. However, the implementation of the dot photodetector concept in other technologies would necessitate a thorough understanding of the material-specific properties and the optimization of fabrication processes. While the fundamental principles underlying the dot photodetector concept remain applicable, the device design and fabrication techniques would require adaptation to suit the unique characteristics of the specific semiconductor technology.

V. Conclusion

A characterization of the multi-dot PIN photodiode consisting of an array of single dots with interconnected cathodes and a shared anode is presented. It is shown that due to a vertical and radial distribution of the electric field around each cathode dot photo-generated carriers are accelerated towards the respective cathode dots, and thus, the region under and between each cathode dot acts as detection zone. A multi-dot PIN photodiode with an active area of 100 μm $\times$ 100 μm using a 5 $\times$ 5 multi-dot PIN photodiode with a pitch size of 20 μm is designed, which achieves a capacitance of 48.8 fF, a responsivity of 0.294 A/W, and a bandwidth of 660 MHz at an operating voltage of 10 V.

However, the active area can easily be enlarged by expanding the dot array, either by increasing the number of cathode dots or by adjusting the pitch size of the array. It is shown that it is crucial to optimize the array's pitch size based on the specific requirements of the intended application as it impacts the capacitance and speed of the diode.

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