Sub-kHz Clock Generation From Room Illumination on Standalone CMOS LSI Chips

Kenta Yamamura, Takaya Sugiura, *Member, IEEE*, Yuta Watanabe, Shiun Yamakiri, and Nobuhiko Nakano, *Member, IEEE*

***Abstract*—This study proposes a sub-kHz clock generator by the room light illumination designed on-chip CMOS LSI chips. It generates a clock from a flicker in room light by receiving on-chip integrated photovoltaic cell, and extracts by low-pass filters, a comparator, Schmidt trigger and D-flip-flop to shape to digital signal. The system implements two photovoltaic cells of a large cell for power generation and a small cell for photo-detection that enables standalone operations. The system was designed on 0.18 μm standard CMOS process, and both the simulation and experimental results validated the operation. By adding D-flip-flops at the output enables to modify the clock to $1/n$ values that expands the applications.**

***Index Terms*—Analog LSI, clock generation, Internet of Things, LED.**

I. Introduction

SIGNAL processing is the core technology for establishing the current information societies, similar to computing devices that have prevailed globally. Clock generation is one of the important function for device regulations, and clock frequencies are diverse from the sub-Hz to GHz [1].

Light sensing is achieved by silicon-based devices, such as CMOS image sensors with integrated photo-diodes and CMOS switches suitable for digital processing [2], [3], [4]. Analog LSI chips operated by self-power generations are useful for IoT (Internet of Things) applications, and hence, can be easily implemented to objects with low costs and high availabilities [5]. Silicon LSI chips can help implement the integrated photo-diodes on the chip by forming pn-junctions with the illumination window. The photo-diodes can be used as photovoltaic cells that generate electrical power to drive circuits. Additionally, this characteristic can help integrate the optical sensors and signal processors into one-chip with standalone operations.

The LED illuminations having approximately 100 Hz frequency which causes the negative effect to photographs known as flicker effect [6]. Therefore, extracting this flicker frequency by the photo-diode will work to generate sub-kHz frequency clock.

This study proposes an on-chip Hz-order flicker detection system designed on standard CMOS processes. On-chip photovoltaic cells are used as a power source and light receiver. The output from the light receiver is processed by analog LSI circuit blocks to generate the shaped digital signal for the detection of flicker. Furthermore, the proposed circuit operates standalone, and hence, can be implemented to on-chip photograph devices [7] to estimate the expanded applications. The fully integrated system is verified through simulation and experiments to generate the 50 Hz square wave from 100 Hz flicker in room light that can use as the low-frequency digital clock.

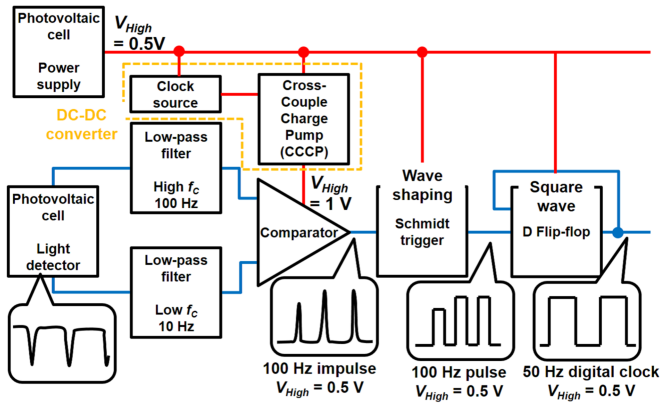

Fig. 1. Proposed on-chip digital clock generation system.

II. The Proposed System

Fig. 1 shows the block diagram of the proposed on-chip flicker detection system. The red lines are power supply, and the blue lines are signal paths. This study provides the flicker (analog signal) conversion to 100 Hz square wave (digital signal) as the digital clock. The system is expanded from our previous work, which proposed a LED illumination detector for on-chip memory writing [8]. The main advantage of the LED illumination detector is the standalone operation of the system, which was achieved by implementing the dual photovoltaic cells of each for power supply and photo-diode. The proposed system is driven on the basis of on-chip photovoltaic cells (it needs a large area). Furthermore, another photovoltaic cell is used as the

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The authors are with the Department of Electronics and Electrical Engineering, Keio University, Yokohama 223-8522, Japan (e-mail: takaya_sugiura@ieee.org).

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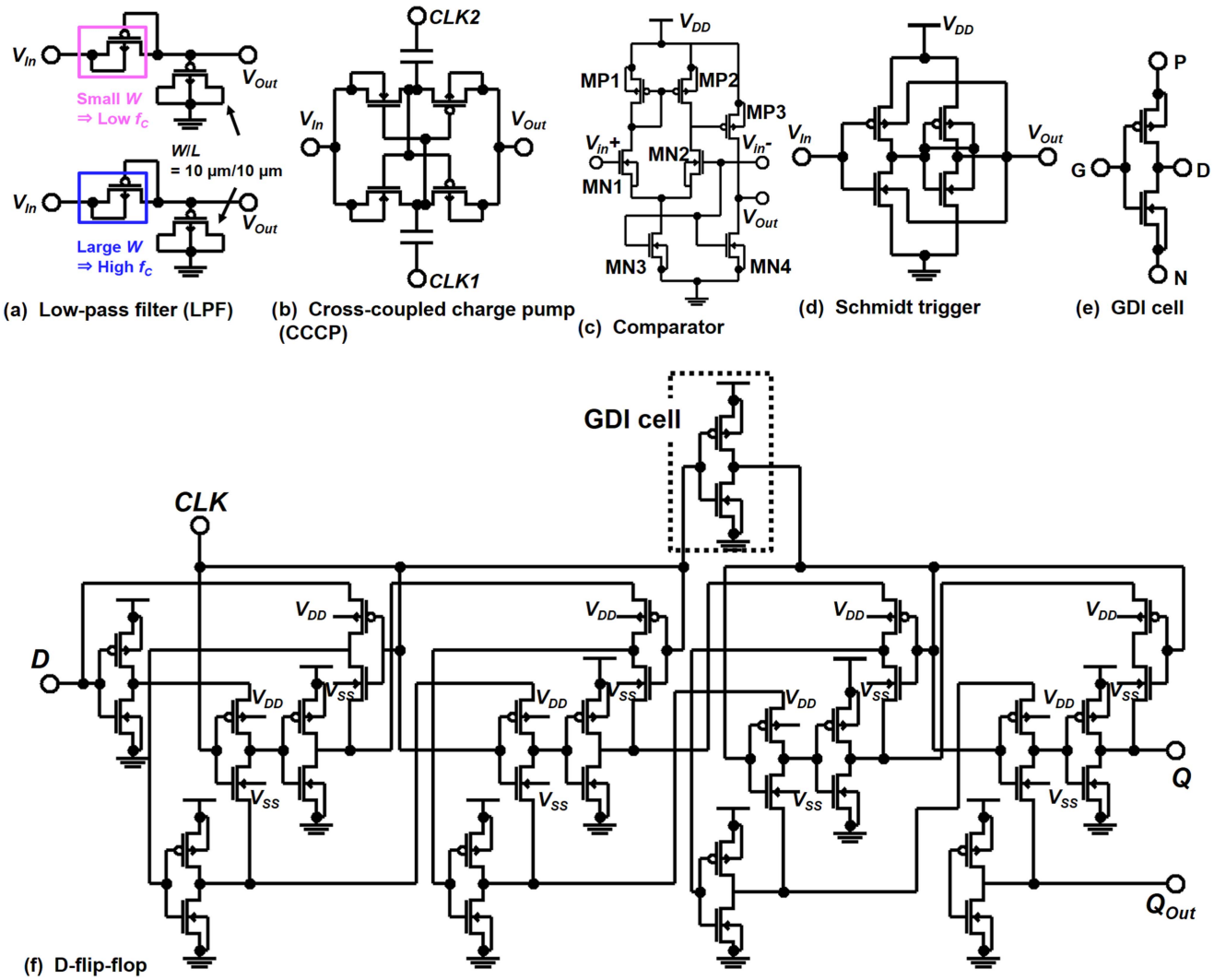

Fig. 2. Circuit blocks that compose the system; (a) low-pass filter (LPF), (b) cross-coupled charge pump (CCCP), (c) comparator, (d) Schmidt trigger, (e) GDI cell, (f) D-flip-flop (DFF).

light receiver (a smaller area is allowed). The output of the light receiver is input to two low-pass filters with different cut-off frequencies. High f_C LPF and low f_C outputs are used as the clock generation (100 Hz) and the reference voltage generation (almost DC), respectively. The DC-DC converter boosts the comparator's output to approximately 1 V, considering the silicon-based photovoltaic cell outputs approximately 500 mV under general illumination, which is too small to process on transistors. The boosted voltage is used to every circuit block to operate transistors (the red lines). When the flicker is included from the illumination, the comparator outputs impulse each time the inverse of flicker frequency. The Schmidt trigger is used to generate the square wave with the flicker frequency. To generate the square wave, a single D-flip-flop is connected, wherein the D-flip-flop comprises a gate diffusion input (GDI) cell [9]. The output of the D-flip-flop; the square wave with the flicker frequency is used.

The system keeps the output signals from the D-flip-flop as long as the light is illuminated and enables real-time flicker detection by FFT (fast Fourier transformation) processing to the signal. Because the image processing will be conducted at a much higher frequency, the detection of the flicker is less likely to inhibit the operation.

Fig. 2 shows the circuit block comprising the detection system. a) low-pass filter (LPF), b) cross-coupled charge pump (CCCP), c) comparator d) Schmidt trigger, e) GDI cell, and f) D-flip-flop (DFF). LPF comprises a diode-connected PMOS as a pseudo-resistor, a MOS-capacitor to avoid using the passive elements of the resistor, and a MIM-capacitor that occupies a large area and is bad for integrations. The cut-off frequency f_C is determined by the resistance R and the capacitance C of the circuit, expressed as

$$f_C = \frac{1}{2\pi RC}. \tag{1}$$

By varying the transistor size of L and W, the R and C values can be adjusted, and then f_C. Here, the MOS capacitor's size is fixed to W/L =10 μm/10 μm.

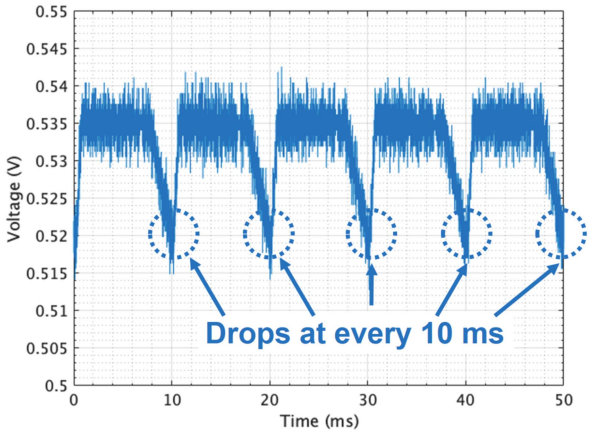

Fig. 3. Measured output of photovoltaic cell under the LED illumination.

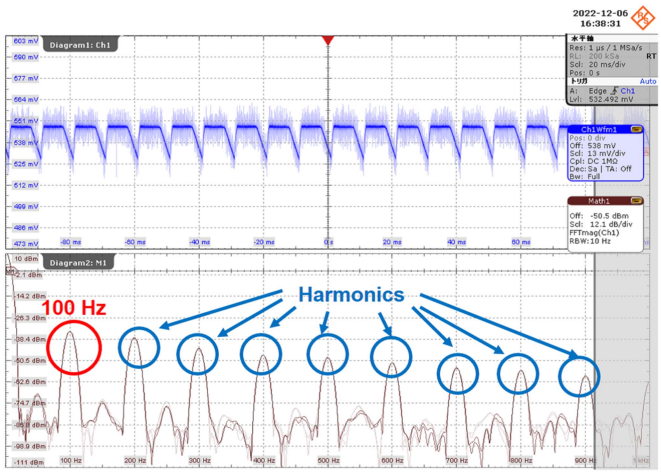

Fig. 4. DFT result of measured photovoltaic cell's output.

CCCP is used to operate the comparator by increasing the output voltage of the photovoltaic cell (as the power source) from 500 mV to 1 V. By inputting the power supply from a photovoltaic cell V_{In} and clock source V_{CLK}, about 1 V voltage generation is estimated. The output voltage of CCCP is ideally expressed from the clock voltage V_{CLK} as

$$V_{Out} = V_{In} + V_{CLK}. \tag{2}$$

In this design, only one-stage CCCP is necessary to supply the power to the transistors. The output of the comparator becomes the impulse at each time of the inverse of the flicker under the LED illumination. The Schmidt trigger shapes the wave to input the D-flip-flop, and the output is the square wave with half of the flicker frequency, which can be used as the digital clock. Adding the D-flip-flop to divide the signal enables to regulate the output clock to $1/n$ frequency. In summary, the proposed system works as the ADC specialized in LED flicker.

III. Validations

Fig. 3 shows the output voltage of the measured photovoltaic cell under the LED illumination powered by the commercial power source. It was observed that the flicker effect appeared at every 10 ms. As LED illumination has large illuminance, about 500 mV or more output voltage can be obtained [10]. Fig. 4 shows the DFT analysis result of the output of the photovoltaic cell, demonstrating that the 100 Hz and harmonic frequencies were included in the LED illumination.

The proposed system circuits were designed on a 0.18 μm standard CMOS process fabricated by Rohm Co. Ltd. Both simulation and experiments were conducted for validation.

A. Simulation

Furthermore, we verify the signal processing of each unit to generate the square wave for digital clock from the photovoltaic cell output. The input power supply voltages to Schmidt trigger and D-flip-flop have been set to 550 mV (the estimated input from a photovoltaic cell).

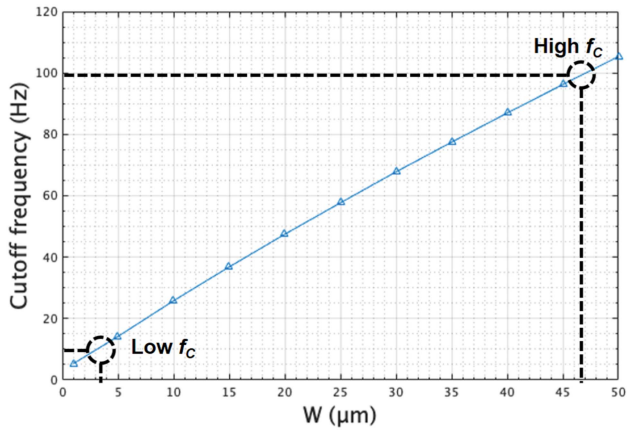

Fig. 5. Cut-off frequency simulation of LPF as the function of the width of the pseudo-resistive transistor.

TABLE I
Element Values of the Devices Used for CCCP

Element	Value
NMOS	W/L = 5 μm/0.18 μm
PMOS	W/L = 5 μm/0.18 μm
Capacitors	C = 15 pF

1) LPF: The cut-off frequency of LPF can be modified by changing the design of the transistor used as the pseudo-resistance. Fig. 5 shows the simulation result of the cut-off frequency of LPF as the function of the transistor's W. As W increases, the current increases; that is, as W increases, the lower resistance and cut-off frequency also increase. Furthermore, the result shows that the cut-off frequency is almost proportional to the transistor's W. Considering our proposed system integrates two LPFs with different cut-off frequencies of 10 and 100 Hz, W of 3 μm (for 10 Hz) and 50 μm (for 100 Hz) were chosen.

2) CCCP: The element values inside CCCP are set as shown in Table I. Fig. 6 shows the transient output of CCCP when the input voltage is 500 mV (photovoltaic cell). It was observed that the voltage increased by two times owing to the CCCP

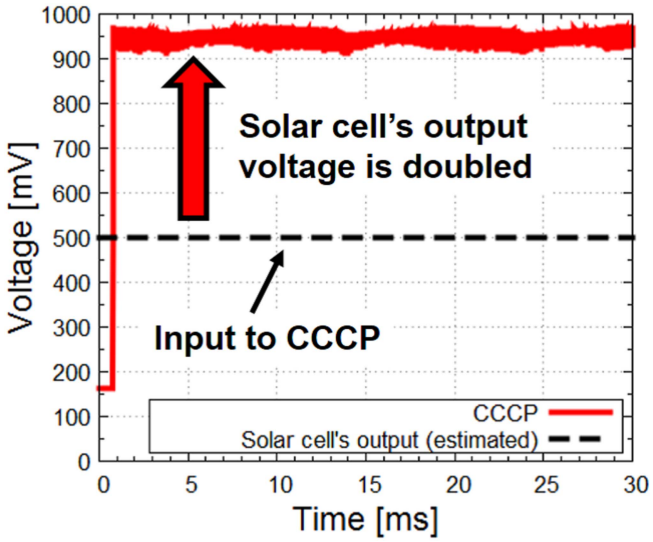

Fig. 6. Transient simulation output of CCCP when the input voltage is 500 mV.

TABLE II
ELEMENT VALUES OF THE DEVICES USED FOR COMPARATOR

Element	Value
MP1	W/L = 5 μm/1 μm
MP2	W/L = 5 μm/1 μm
MP3	W/L = 13 μm/1 μm
MN1	W/L = 20 μm/1 μm
MN2	W/L = 20 μm/1 μm
MN3	W/L = 2 μm/1 μm
MN4	W/L = 2 μm/1 μm

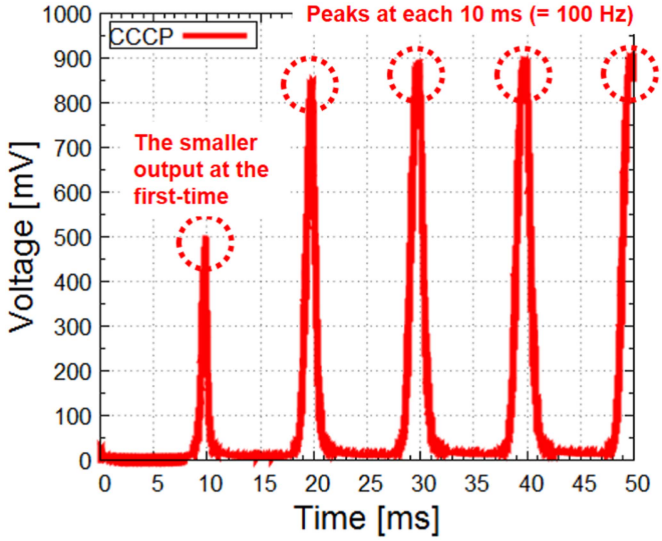

Fig. 7. Transient simulation output of comparator with the V_{DD} of Fig. 5 and two inputs from the output voltages of two LPFs.

with approximately 1 ms, which is significantly shorter than the flicker frequency from LED.

3) Comparator: The element values inside comparator are set as shown in Table II. Fig. 7 shows the comparator's transient output with V_{DD} of Fig. 5, and two inputs of the output voltages

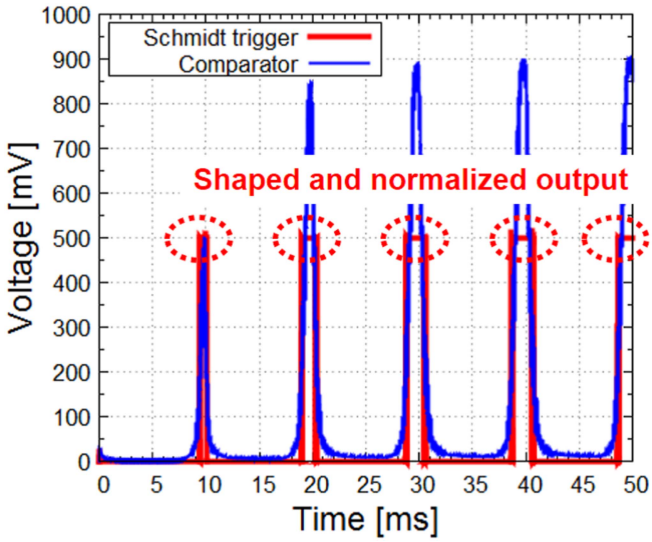

Fig. 8. Transient simulation output of the Schmidt trigger as the input of the comparator's output of Fig. 7.

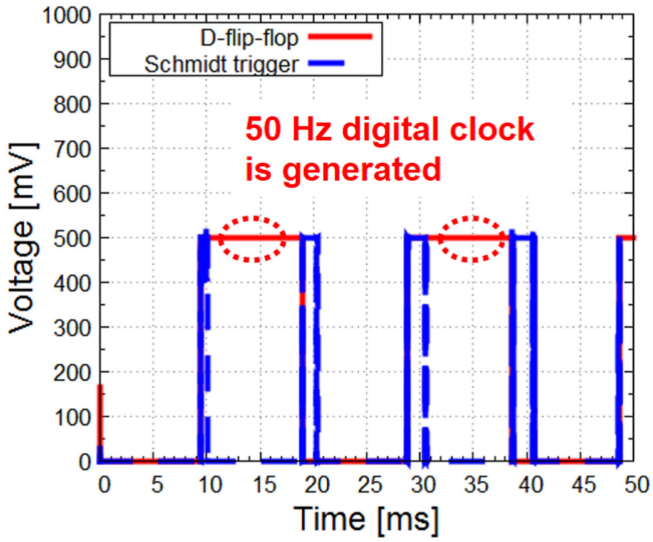

Fig. 9. Transient simulation output of the D-flip-flop as the input of the Schmidt trigger's output (after eliminating the chattering).

from the two LPFs. It was observed that the impulse appeared at every 10 ms (100 Hz), thereby detecting the flicker.

4) Schmidt Trigger: Fig. 8 shows the output of the Schmidt triggers with the input of the comparator's output in Fig. 7. It was observed that wave shaping was done.

5) D-Flip-Flop: Fig. 9 shows the D-flip-flop output when the input is the Schmidt trigger's output (here, we eliminate the chattering of the Schmidt trigger caused by the latency of the comparator's output). It was observed that the square wave with half of the flicker frequency was successfully obtained.

B. Experiment

The above simulation results verified the proposed concept. An experiment was then conducted at the component-level to

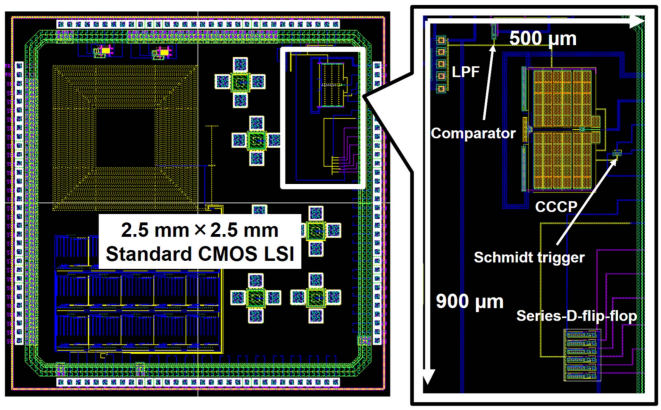

Fig. 10. Layout of the entire system (the D-flip-flop part is shared to another circuit and the first output of the D-flip-flop is used).

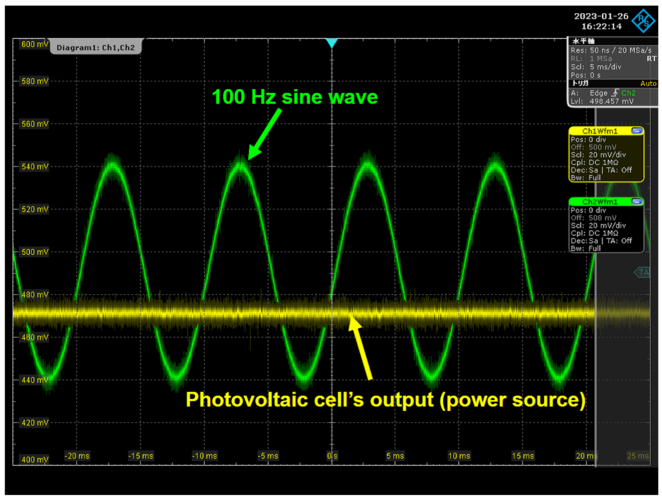

Fig. 11. Input signal to the comparator and CCCP that emulate the output of LPF (100 Hz sine wave) and the photovoltaic cell (500 mV DC).

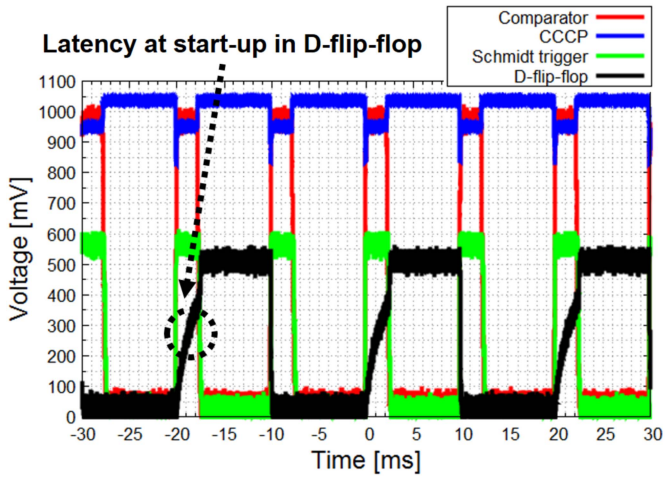

Fig. 12. Measured output voltages of each component from the inputs in Fig. 11.

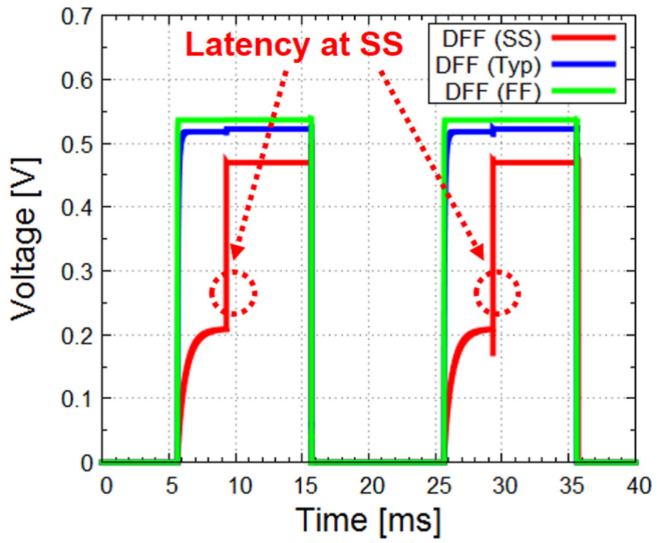

Fig. 13. Transient responses of the D-flip-flop with different corner conditions.

verify that the realistic operation can also process the signals successfully. Fig. 10 shows the layout of the system; the area was 500 μm $\times$ 900 μm (as this layout is aimed to measure each component and connected to several output terminals, the implementation is not optimized). Here, the D-flip-flop part was shared with another circuit; in this study, only the first-block of the series-D-flip-flop was used as the output. The system was integrated from the LPF to the D-flip-flop block, thereby enabling measurement of the response.

Fig. 11 shows the input signal that emulated the output of the LPF block with a 100 Hz sine wave (the green line), and the photovoltaic cell's output as the power source (denoted by the yellow line). The sine wave and DC-signal were input to the comparator and CCCP for voltage boost verification, respectively.

Fig. 12 shows the measured output voltages of each component: the comparator, CCCP, Schmidt trigger, and D-flip-flop. The measurement starts by inputting the emulated LPF output (Fig. 11) to comparator, then Schmidt trigger, and D-flip-flop (CCCP's output can be obtained from the emulated photovoltaic cell's output in Fig. 11). The results showed that the proposed system successfully generated the 50 Hz digital clock with the emulated photovoltaic cell's output signal. The comparator generated the 1 V impulse at 10 ms from the CCCP's output of 1 V boosted voltage, and the Schmidt trigger then generated a 500 mV impulse with the input from the comparator's output. Finally, the D-flip-flop generated a 50 Hz square wave with the input from the Schmidt trigger's output.

Here, the D-flip-flop showed the latency at the start-up, which can be attributed to two reasons. First, because the D-flip-flop was series-connected and shared with another circuit (not used in this system) it increased the load resistance of the output, causing latency. Therefore, using only one D-flip-flop to output could improve the start-up speed. The second reason is the process corner of CMOS fabrications. Fig. 13 shows the transient responses of the D-flip-flop with different process corner conditions. When the process corner is SS (denoted by the red

line), the performance of the transistors degraded the start-up and caused a delay. We also estimated that the two issues could work to switching latency in the D-flip-flop (increased load resistance and worse transistor performances). Our previous work suggested SS-like process variation in the CMOS process [11]. Also, our implementation was not optimized as like Fig. 10, and layout optimization is predicted to be effective to ease the latency. These issues can be avoided by removing the series-D-flip-flop and changing to shrunk CMOS process for enhanced switching speeds.

Except for the latency in the output of the D-flip-flop, the experimental results demonstrated the sequenced processing of the signals to generate the 50 Hz square wave.

IV. Conclusion

This study proposed an sub-kHz digital clock generation by the LED flicker extraction system. The proposed system was aimed for standalone operation, with two on-chip photovoltaic cells of power source and light receiver, and multiple signal processing for generating the digital clock with the flicker frequency. Validation of the proposed method was achieved from both simulation and experiments, which successfully output the signal as the digital clock. Integrating this system can help digital signal regulation under room illuminations.

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