Overcoming Silicon Limitations in Nanophotonic Devices by Geometrical Innovation: Review

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(Invited Article)

Abstract—**In order to continue to fulfill the ever-increasing demands on ultra-fast microprocessors, a revolution in silicon photonics communication is necessary. Traditional CMOS, FinFET, and GAAFET downsizing techniques have started to near the physical limits of available materials. Although on-chip optical communication presents a promising direction for circumventing the scaling bottleneck, silicon-based solutions are constrained by several factors, such as the element's indirect energy band gap, limited absorption spectrum, native oxide, and more. However, the employment of recent innovative design geometries has enabled the development of a series of silicon nanophotonics and nanoelectronics devices that both overcome these limitations as well as improve on existing physical phenomena. Presented in this comprehensive review is a new, methodical approach showcasing examples of these Si nano-devices, which are part of a larger family of components being developed for optical communication and advanced sensing applications. After presenting stand-alone devices, we discuss concerns, considerations, trends and forecasts regarding their possible integration into nanophotonics modules and platforms.**

Index Terms—**Comsol Multi-Physics simulations, geometry workaround, indirect band gap overcoming, inter-sub-band transitions (ISBT), nanophotonics and nanoelectronics silicon devices, photonic integrated circuits (PIC).**

I. Introduction

FOR the last five decades, complementary metal-oxide-semiconductor (CMOS) technology has formed the backbone of the semiconductor industry as a whole and the microprocessor industry in particular. Since 2005, traditional CMOS scaling techniques have begun to reach the physical limits [1], [2], [3], [4] of available materials. Additional technologies have appeared over the years, such as the fin field-effect transistor (FinFET) and the Gate-All-Around field-effect transistor (GAAFET) designs. As MOSFET dimensions approach the 3-nanometer scale, a number of problems begin to plague the device. Second order phenomena such as electron migration, quantum tunneling and parasitic capacitances become significant contributing factors to interconnect delay, slowing the communication between on-chip components and decreasing computational power. Additionally, potentials inherent to the material such as thermal voltage do not scale, meaning that the heat dissipated increases exponentially with the on-chip density of MOSFET transistors. Eventually, cooling requirements make the device impractical or untenable.

A number of international groups and research teams have designated on-chip optical communication and interconnects [5], [6], [7] as a promising solution for circumventing the CMOS scaling bottleneck. Optical communication would bring major disruptive solutions for the problems currently faced by CMOS technology, as it would allow for significant reduction in the use of the metal interconnects currently employed as communication lines between on-chip components. This would solve the aforementioned problem of second order phenomena and free up space on the chip surface for the integration of more transistors.

Indeed, optical communication can be scaled down, and enable space free up by replacing complex and sizeable electronic metal interconnects. In addition to size and complexity, optical interconnects can address several other existing issues caused by the metal lines. Among others, one can identify cross-talk, interferences, proximity and density limitations, overheating failure mechanisms, quality and reliability rules constraints, and full integration needs. We now explore some of the above improvements that optical communication can bring in regard to microelectronics architecture.

Efficient scaling is a paramount concern in microelectronics. Metal electronic interconnects such as copper wires require minimal space to be set aside not only for their own dimensions but also for insulation in the vertical and horizontal gaps between them. In contrast, on-chip optical interconnects can be implemented using waveguides, which are much smaller in size. These waveguides are usually several hundred nanometers wide and require some place in between them, as do traditional lines; however, this still more efficient spatial usage than metal lines. Waveguides can be stacked in a more compact way than metal lines. Typically made from materials such as silicon oxide or polymers, the waveguides can be fabricated directly on the chip substrate, where they direct the optical signals and allow for compact routing of data within the chip.

Metal electronic interconnects require the splitting of lines to reduce currents and prevent overheating failure mechanisms such as self-heating and electro-migration. In addition, quality

Manuscript received 15 May 2023; revised 22 June 2023; accepted 10 July 2023. Date of publication 13 July 2023; date of current version 15 August 2023. The development of the AFM-NSOM dual-mode tip photodetector (Figures 13 to 17) was supported by the Israel Innovation Authority (IIA) under Grant 74788 (JCT) and Grant 74761 (BIU), and is under Patent number US 11,169,176 B2.

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Digital Object Identifier 10.1109/JPHOT.2023.3295077

and reliability rules may also require further enlargement of the lines even after splitting. Crucially, this complexity increases as the number of interconnections and data paths grow. On the other hand, optical communication can easily deliver multiple data streams through a single waveguide, eliminating the need for different layers of wiring and simplifying the routing process.

Another concern addressed by optical communication is the proximity and sometimes high density of metal interconnects causing non-desirable interferences and crosstalk due to electromagnetic coupling. This tendency is mitigated in optical communication since the light signals do not interact with each other in the same way (different wavelengths, polarization modes, etc …). Consequently, optical interconnects can be packed more closely together, enabling higher data transfer density within a given area on the chip.

Eventually, the coexistence of electronic and optical components on the same wafer can simplify and improve the chip performance. For example, lasers, modulators, and photodetectors can be directly integrated on a silicon substrate beside electronic components. By integrating these optical components with other chip elements, space can be saved as there is no need for separate, external optical devices [7].

Although technological advancement has already pushed silicon based computing to its physical speed and size limits [4], further innovations are still expected to be based on this cheap, widely available material, which makes up almost 28% of the Earth's crust [8], [9], [10]. Pushing silicon beyond its current boundaries will require replacing electronic systems with photonic ones [11], [12], [13], [14], and advancements in the field of silicon photonics integrated circuits (PICs) [6], [7] in order to combine optical signals with electronic data processing. As expected, development of these devices for use in the next generation of ultrafast computers is proceeding in concert with more general efforts to develop the next generation of optoelectronic communication systems. Recently published roadmaps outlining silicon photonics' future [5], [12], [15], [16] discussed the various innovations and benefits expected to result from further development.

Silicon has long been the material of choice for nanophotonic devices due to its well-established fabrication technology, high refractive index, and compatibility with CMOS electronics. The field of silicon photonics has made great strides since its inception in the 1980s [12], and at the beginning of the 21th century [17] more and more start-ups are working in the area. However, silicon has some limitations in terms of its light-emitting and light-absorbing capabilities, as it is a priori limited by its indirect band gap. One may classify the effects of silicon's limitations according to their impacts on three types of devices which are the building blocks of the optical communication chain: light emitting devices, light guiding devices (waveguides) and light receiving devices (sensors):

- *Light emitting devices* – Regarding light emitting devices, their main constraint is the fact that silicon possesses an indirect band gap between the conduction and valence bands, preventing radiative recombination. For this reason, it is difficult to obtain light emission in standard monocrystalline silicon.
- *Light guiding devices* – In the context of light guiding devices (waveguides), silicon's well-known low absorption range, usually thought of as a constraint, can be considered a benefit for several reasons. In the near-infrared wavelength range used in silicon photonics such low absorption allows for better efficiency of the signal propagation through the waveguide. Because of this low absorption, the light experiences minimal loss as it propagates, leading to longer transmission distances without significant degradation. This is crucial for maintaining signal integrity, reducing crosstalk between neighboring waveguides, enabling high-performance optical communication and energy efficiency without additional amplification, and proper integration with other photonic components.
- *Light receiving devices* – Lastly, in contrast to passive waveguides (for which a low absorption is generally preferred as it enables reliable and efficient signal transmission, as outlined above), in the case of light receiving devices a high light absorption is desired. This holds particularly for photodetectors or modulators, where it is necessary for efficient device operation.

While some researchers have been looking for alternative III-V compound semiconductors (like GaAs, and InP) in addition to silicon components [18], [19], others tried to produce CMOS compatible silicon photonic devices using specially adapted materials and configurations. However, these efforts did not always meet with the greatest of success and had serious replicability issues. Three decades ago, a material in the form of porous silicon [20], [21], [22], which would enable limited controlled luminescence in the visible range at room temperature, was developed [23]. Other studies were conducted on electroluminescence effects while using hot electrons to impact the pinch-off configuration in MOS devices [24], [25]. Yet another hot electron-based attempt was to track the radiative intra-conduction relaxation [26] and the impact ionization [27] mechanisms, which led to radiative recombination of electron-hole pairs. In addition to electroluminescence [28], photoluminescence was also studied, using silicon quantum well structures [29], [30], [31], [32].

Over the years, many important books [33] (including recent ones [34], [35]), extensive reviews [14], [36], [37], Moore's law forecasts [1], [2], [3], [4], perspective analyses [38], and roadmaps [5], [12], [15], [16] covering the domain of silicon photonics [39], [40] have been published and presented to the Scientific Community. Of course, hundreds of articles were published as well, and it is not realistic to address all of them. Indeed, as part of our review, we will survey the four existing trends for overcoming silicon's limitations, as well as an innovative fifth strategic direction in Si nano-photonics. In the past, similar reviews focused on specific items like coupling, switching and modulation challenges [41]. Here we extend the approach to cover most of silicon photonics' needs. For convenience, Fig. 1 shows the presented review structure, which is further detailed in the paragraphs below. Taking into account the progress made over the last few decades, the strategies available today can be categorized into four complementary areas, with a fifth one suggested on our part:

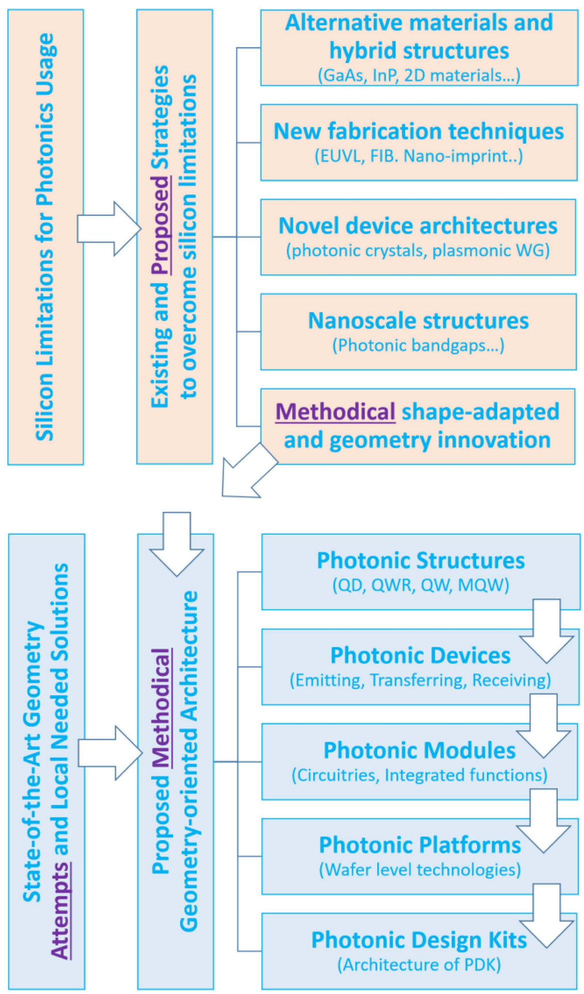

Fig. 1. Schematic chart presenting the reviewing structure of the article. Starting from a mapping of silicon's limitations for photonics usage, and going through existing tried solutions (upper orange background part), the article will propose a methodical approach of 5-levels architecture (lower blue background part), all using special shapes and geometry to overcome silicon photonics limitations.

1) Alternative materials and low dimensional structures: As mentioned above, silicon is a commonly used material in photonics devices, but it has limitations in terms of its light-emitting and light-absorbing capabilities. One solution is to employ complementary materials which have better optical properties such as III-V semiconductors, like gallium arsenide (GaAs) [36], [42], [43], [44] and indium phosphide (InP) [45], [46]. 2D materials [47] such as graphene [48], [49] and transition metal dichalcogenides (TMDCs) [50] are also candidates, and gallium nitride (GaN) [51] has also been investigated. The integration of these materials into silicon-based devices enables the creation of hybrid structures that offer superior performance. Some attempts have used modified silicon structures such as porous silicon [20], [21], [22], amorphous silicon [52] and combined silicon-germanium [53], [54], [55]. Older alternative materials included solutions such as polymers [56], organic light-emitting diode (OLED) [57], [58], and carbon nanotubes (CNT) [59] as replacements for transistors. Recently, researchers from Massachusetts Institute of Technology (MIT) presented a

TABLE I
MAIN ALTERNATIVE CANDIDATES FOR SILICON PHOTONICS

Type	Alternative Candidate	Status and Main Applications
Silicon-modified structures	**Amorphous Silicon** [52]	Amorphous silicon structure. Low-loss passive devices: Waveguides (WG), power-splitters, tapers, ring resonators, micro-cavity resonator, and Mach–Zehnder interferometers
	Porous Silicon [20] [21] [22]	Porous silicon structure. Effect of Electroluminescence. Not always repeatable. Micro-cavity resonators.
	Silicon Germanium (SiGe) [53] [54] [55]	Modulators for Telecom. Lasers for Datacom. Photovoltaic. Extension to Near-to Mid-Infra-Red (NIR to MIR).
III-V Compound Semiconductors	**Gallium Arsenide** (GaAs) [36] [42] [43] [44]	Expensive and brittle. Insulation layers are complex. Used where Si is not sufficient. Detectors, Lasers, Quantum-cascade lasers (QCLs) for Defense
	Indium Phosphide (InP) [45] [46]	Microwave (MW) photonics, free space laser communications, light detection & ranging (Lidar).
	Gallium Nitride (GaN) [51]	RF photonics for Defense. Advanced LEDs for Energy.
	Cubic Boron Arsenide (CBA) [60]	New attempt. Overcoming electron-hole limitations and overheating. Heterojunctions, photovoltaic devices, NIR light detection.
Low Dimensionality Materials	**Graphene** [48] [49]	Si-graphene hybrid photonics. Modulators and photodetectors. Plasmonic nano-cavities, silicon nano-wires solar cells, quantum well lasers. Meta-material structures
	Transition Metal Dichalcogenides (TMDCs) [50]	Photo-response mechanisms: photodetectors, photovoltaics and light emitting devices
	Carbon Nanotube (CNT) [59]	CNT-based photodetectors. Sub-10 nm channel length transistors.
Organic Materials	**Polymers:** Si-organic-hybrid (SOH), plasmonic-organic-hybrid (POH) [56], OLED [57], biodegradable photonics [67]	Optical modulators

new material called cubic boron arsenide (CBA) [60] to overcome the holes limitation. However, the material was fabricated and tested in very small laboratory batches. Table I summarizes the main material alternative options.

2) New fabrication techniques: Traditional microfabrication techniques such as photolithography and electron beam lithography are limited in terms of the resolution and complexity of the structures which can be created through them. In cases where resolution accuracy is a limiting factor, a number of emerging techniques offer higher resolution, complexity and greater control over the dimensions and shapes of nanoscale structures. Examples include nanoimprint lithography [61], [62], focused ion beam (FIB) milling [63], direct laser writing, and extreme ultra-violet lithography (EUVL) [64], [65], [66].

3) Novel device architectures: New device architecture offers another work-around for some of the limitations of silicon-based devices [68]. For example, instead of using traditional optical waveguides, one can employ photonic crystal [69] or plasmonic waveguides [70], which can offer greater confinement and lower losses. Similarly, conventional light emitters such as LEDs or laser diodes can be replaced by light sources such as quantum dots or nanowire LEDs [71], [72], which can offer higher efficiency and lower power consumption. There are several photonic device architectures. Each one of them usually uses different electro-optic effects and mechanisms to manipulate optical signals for sensing, receiving, modulating, switching, and/or other functions. The specific architecture chosen will depend on the desired application, performance requirements, and compatibility with the materials and technologies employed. Among others, one can identify the following communication and sensing system architectures. In optical sensing applications, various electro-optic device architectures are employed such as Fabry-Perot interferometers [73] and fiber Bragg gratings [74]. Interferometric sensors are used to detect physical quantities such as strain, temperature, or pressure. Such sensors rely on the interaction of light with the electro-optic properties of the sensing elements to provide accurate measurements. For control of optical signals routing, various architectures can be employed for optical switches, including microelectromechanical systems (MEMS) [75], liquid crystal-based switches [76], and semiconductor optical amplifiers (SOA) [77]. Usually, such switches use electrical control signals to manipulate the optical path of signals, allowing for efficient switching between different optical channels or paths.

4) Nanoscale structures: Structures with dimensions on the nanoscale are capable of manipulating light in ways beyond the reach of conventional optics. For example, photonic crystals can be used to create photonic bandgaps that prohibit certain wavelengths of light from propagating through the material [78], [79], [80]. Similarly, plasmonic structures can be used to confine and enhance the electromagnetic fields in very small volumes. However, such structures are only part of a full solution-flow we propose in the next paragraph.

Overall, it appears that the key to overcoming the limitations of silicon in nanophotonic devices is to use a combination of these four strategies in a creative and methodical way, taking advantage of the latest advances in materials science, nanofabrication, and device engineering. A fifth alternative, methodical, and strategic direction is now proposed as an added value of the review:

5) Methodical geometry innovation: Smart engineering of a silicon device geometry can enable it to mimic certain physical properties usually obtained with alternative materials. Manipulation of the light can also be done by changing the geometry and the dimensions of a structure or of a device. For example, silicon waveguides are usually rectangular shaped in order to limit the number of optical modes capable of propagating inside. Changing the shape of the waveguide will enable the manipulation of light polarization and dispersion. Another example of light confinement is the use of specially shaped nano-structures such as nano-wires, nano-tubes, and nano-disks. Then one can confine the light in extremely small volumes. Extending the idea, such methodical exploitation of the geometric properties of special structures and adapted shapes may constitute a new approach. We will present several specific geometries which completely alter the behavior and the applications of nano-devices, transforming them from regular nano-electronic devices into nano-photonic ones. Then, we will expand our discussion into the area of methodology, outlining five phases of development in a bottom to top approach: 1) quantum-based or nanoscale structure, 2) photonic device, 3) photonic module, 4) photonic platform and 5) photonic products designed kits (PDKs). This review presents several representative examples, out of more than forty components currently developed by our team, of nanoscale silicon-based devices whose special geometrical structure enables them to overcome silicon's limitations as well as to reinforce physical phenomena (absorption and emission spectra). These devices were all initially simulated using Comsol [81], following which they were fabricated and tested.

II. Tailored Geometrical Shapes in Nano-Devices

When compared to replacing silicon with alternative materials (Table I), implementing adapted geometries in relevant nano-devices can serve as a simpler workaround of silicon's limitations. Out-of-the-box thinking is critical in the design process, as will be seen in the following examples of creatively shaped, high-performance devices. Such devices, based on smart independent structures, and connected to form modules, will enable future integration into existing platforms.

A. State-of-the-Art Geometry Attempts and Tailored Solutions

As presented below in the sub-classification, over the last three decades, researchers have tailored many smart devices using various special adapted shapes and/or geometry. Since many of these research teams worked in parallel, and specialized in different types of devices (waveguides, sensors, lasers etc ...), these state-of-the-art devices usually appeared as a local solution to an existing concern or need. Surveying the literature, it is difficult to identify a fully-fledged vision of developing a complete family of devices based on geometric architecture. However, as mentioned in the introduction, one does point out some major application domains for which geometry is of crucial consideration in photonic device design: 1) Light-emitting components of quantum-based structures, in which the control of the layer thickness and distance between wells are important; 2) Photonic waveguides and fibers in which core geometry, angles and refractive indexes are primordial to prevent losses (i.e., optical interconnects); 3) Light sensors, modulators and more; and lastly one can find 4) Sensing scanning tips for surface super-resolution.

1) Light-Emitting Devices of Quantum-Based Structures: Quantum-based structures served as the basis for light-emitting devices. Quantum wells, quantum wires and quantum dots, mainly in GaAs [82] but also in Si [83], [84], [85], were unsurprisingly at the center of geometry-related research. The layers thickness in nanoscale range is critical for enabling quantum effects. In addition to the thickness, additional parameters like dopants influence were checked with time [86]. Several research teams (like Prof. Krishna Saraswat's at Stanford University) focused on the integration of quantum wells in MOSFET [87] for light emission purpose, employing a high-k dielectric material [88].

2) Waveguides and Fibers as Photonics Interconnects: Photonics interconnects are the best candidates to replace the metal interconnects ubiquitous in the microelectronics industry. This is why massive efforts have been invested over the years in the development of viable solutions for "wiring" through waveguides, in particular in the Mid-Infra-Red (MIR) domain [89]. Studies have been performed not only on the wavelength range, but also on the waveguide shape: recently, triangular cross-section waveguides (as opposed to the standard circular ones) were studied [90].

3) Sensing Components as Light-Receiving Devices: The third main category of silicon photonics components is that of silicon light-receiving devices and sensors [91], or integrated silicon light sensors [92], [93]. With devices from these three topics, we can close the basic loop of emitter-medium-receiver purely through silicon photonics components: light emitters, waveguides, and light detectors.

4) Surface Scanning Components for Super-Resolution: The sensing domain for surface scanning has become more important with time [94]. Other sensing components have been developed for near field super-resolution as opposed to standard optical communication. For example, two decades ago, a pyramid-shaped silicon photodetector with a subwavelength aperture was developed in for Near Field Scanning Optical Microscopy (NSOM) sensing [95]. The photodetector, realized with conventional microelectronics technology, is located on top of a high pyramid, enabling detection of reflected as well as transmitted light. The device is an example of a very cleverly shaped component designed with out-of-the-box thinking.

In super-resolution sensing, the photo-induced force microscopy is a very accurate optical force sensing technology, capable to achieve very accurate nearfield sensing [96]. Also, Si photonics have been widely applied to artificial intelligence [97], [98], optical calculation (optical deep learning network) [99], [100], Light Detection and Ranging (LiDAR) [101], [102], and more and which are all important applications of Si photonics. Since the domain of Si photonics is continuously evolving, there could also be many important sub-fields of Si photonics which were unintentionally forgotten.

In addition to above State-of-the-Art geometry tailored solutions for photonic devices, additional emerging Si photonic domains appeared such as topological optics [103], exceptional point [104], Mie-optics [105] and more, and which enabled also the development of innovative photonic devices. Topological optics, which was identified as a rapidly growing field, explores unique light propagation phenomena and devices, and based on the topological properties of materials. While silicon is not an inherently topologically non-trivial material, it can be combined with other materials or structures to realize topological photonic devices.

Among silicon photonics devices based on topological optics, one can find the topological insulator-based waveguides [106], lasers, photonic crystals and Metamaterials. Realization of silicon photonics devices based on topological properties is an evolving research area, in which the development and integration of topological optics in silicon photonics are ongoing and subject to further advancements and discoveries. Silicon can be utilized as a component or substrate material in the fabrication of metamaterial structures [107], in spite the fact it is not typically considered a metamaterial since sharing inherent properties to manipulate electromagnetic waves in the same way as engineered metamaterials.

Metamaterials are typically constructed by arranging subwavelength structures (nanostructures) in a specific pattern to achieve the desired electromagnetic properties. While silicon is not inherently a metamaterial, it can be used as a building block or host material for creating metamaterial structures. For example, silicon can be used as a substrate or platform material to support the arrangement of metallic or dielectric nanostructures that give rise to the desired electromagnetic properties. By incorporating silicon into the fabrication process, researchers can leverage its well-established fabrication techniques and compatibility with complementary metal-oxide-semiconductor (CMOS) processes to create metamaterial structures. Silicon-based metamaterials have been explored in various applications, such as terahertz devices [108], photonic circuits [109], [110], plasmonics [111], and sensing [112]. These applications often involve integrating silicon with other materials or nanostructures to create the desired metamaterial properties. So, while silicon itself is not a metamaterial, it can play a crucial role in enabling the fabrication and integration of metamaterial structures to achieve the desired electromagnetic functionalities.

Silicon metasurfaces were proven perfectly compatible with CMOS technology and Si photonics [113], which already widely serve as optical waveguide [114], imaging lens [115], and holography [116]. For alternative materials, Si photonics is also perfectly compatible to thin film of Lithium niobite [117], which can achieve much faster modulation speed.

B. Challenging Examples of Shape Adapted Devices

Our team [118] has taken up the challenge of developing a series of devices methodically based on shape-adapted solutions. Whenever the team starts a new project, it identifies the needs and expected performances based on specifications or requests, while translating the identified "challenges" into possible options of adapted geometries. This work is not straightforward; however, with patience and creative thinking, one can develop tailored adapted solutions. Sometimes, an existing well-known electronic device is customized in order to impart photonic properties to it. The team is specialized in developing new nano-electronic and nano-photonic devices, primarily using numerical platforms and scripts, with analytical models added to complement the investigation. Comsol Multiphysics [81] is an advanced simulation program which provides the tools to model structures and solve complex physics and engineering problems. The program is based on the Finite Element Method (FEM) [119], which is a method of numerically solving differential equations describing field problems [120], [121], [122]. In practice, Comsol constitutes a basic platform that includes primary functions of model designing and geometrical definition via the program [123]. Throughout the research, modules like "Semiconductor" and/or "Wave Optics" are used. To fully set up a device for testing, one must complete a few steps prior to the simulation itself. A few examples are presented below:

1) Gate-Recessed Channel as light emitting transistor: As noted above, silicon photonics research is a key effort in the race to realize ultra-high-speed processors [124]. We developed a new concept of MOSFET transistor, called MOSFET Quantum Well (MOSQWELL) [125], which overcomes the silicon indirect band-gap with special geometry. The device is based on a silicon quantum well structure (Fig. 2a) which enables control of light emission by through varying the thickness of the silicon layer. This quantum well consists of a recessed ultra-thin silicon layer, obtained by Gate-Recessed Channel (GRC) geometry, which is located between two oxide layers (Fig. 2b). Regular band-to-band (BTB) transitions between conduction and valence bands do not allow for radiative recombination. However, hot electrons enable easier photonic inter-sub-band transitions (ISBT) in the conduction band. Located along the transistor channel, the quantum well structure forces the generation of hot electrons and photonic inter-sub-band transitions (ISBT), as shown in Fig. 3.

The device's coupled optical and electrical properties have been simulated for channel thicknesses varying from 2 to 9 nm (Fig. 4) [126]. The simulation results show that this device can emit NIR radiation in the 1-2 µm range (Fig. 4), compatible with the optical networking spectrum. The emitted light intensity can be electrically controlled by the drain voltage V_{ds} while the peak emission wavelength depends primarily on the channel thickness, with a slight influence of V_{ds}. Moreover, the location of the radiative recombination source inside the channel, responsible for the light emission, is also controllable through the applied voltages.

A dual-mode form of operation (i.e., both electrical and optical) is feasible, in which some of the transistors can be set to work as regular nanoelectronics switches and others as photonic transmitter or modulator devices. This raises the prospect of future architecture enabling two types of parallel communications (Fig. 4).

2) Y-Junction in Silicon Waveguides: Although Y-junctions in waveguides (WG) are not a new concept [127], they remain a necessary and required intersection in the interconnect world of optical data communication. Both symmetric [128] and asymmetric [129] Y-junctions were developed in the past for local needs. Moreover, not only standard separation branching was developed, but also nice are-shaped branching waveguide Y-junctions were fabricated [130].

The PAINT (Phase And INtensity Trace) device is a silicon-based Y-junction waveguide for the Near Infra-Red (NIR) [131]. As opposed to a regular waveguide, which simply transmits light in a given direction while minimizing power loss, a Y-junction

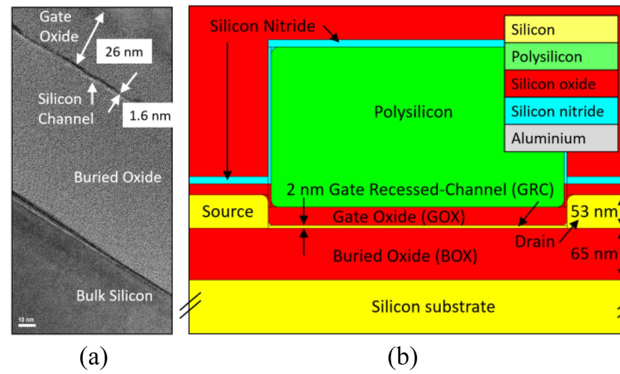

Fig. 2. MOSQWELL device structure: (a) HRTEM image of the real device showing Gate Recessed Channel (GRC) under the gate region; (b) Comsol simulation of the device, showing the quantum well embedded structure and the different layers.

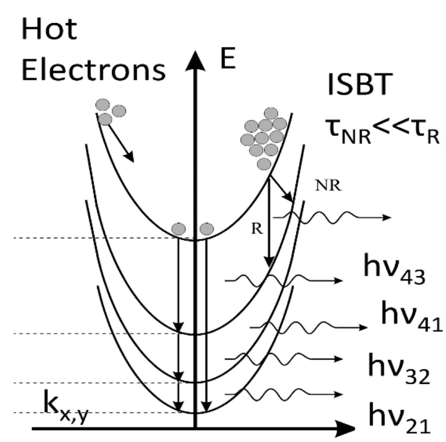

Fig. 3. Photonic inter-sub-band transitions (ISBT) of hot electrons in the conduction band of the MOSQWELL channel.

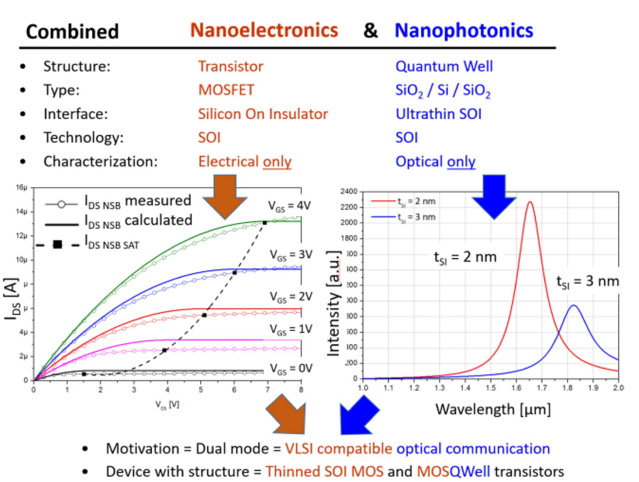

Fig. 4. MOSQWELL device dual-mode concept with light emission spectra for channel thickness of 2 and 3 nm.

separates or combines signals according to a desired ratio. As shown in Fig. 5, a Y-junction is comprised of three sections: branching, tapered and straight-guide. Its working principle is described in terms of simple modes: there are two types of local normal modes, odd and even. In the branching section, the two

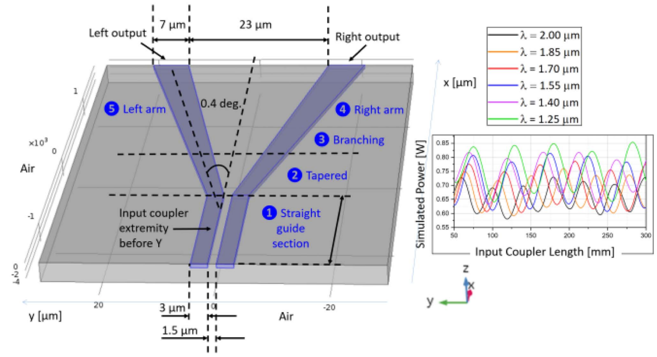

Fig. 5. PAINT device 3D Comsol schematics.

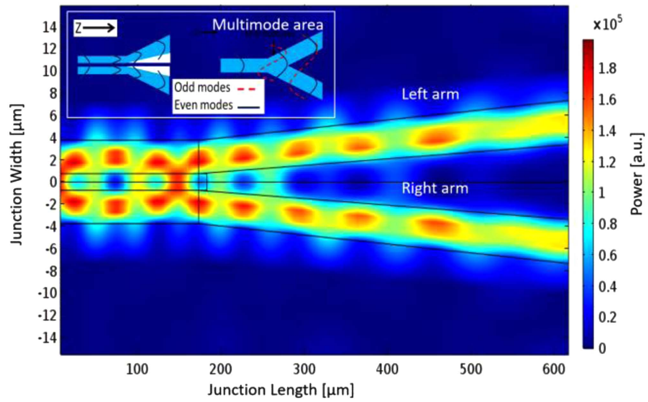

Fig. 6. PAINT device Comsol-simulated EM wave power distribution in the Y junction area. The coupling continues even after the junction split-up.

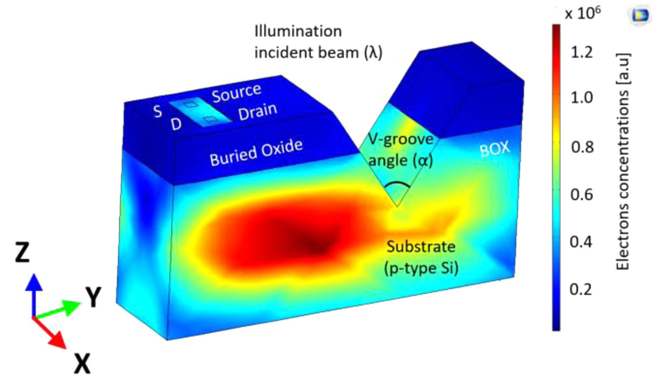

Fig. 7. SOIPAM device showing the V-groove geometry using Comsol schematics.

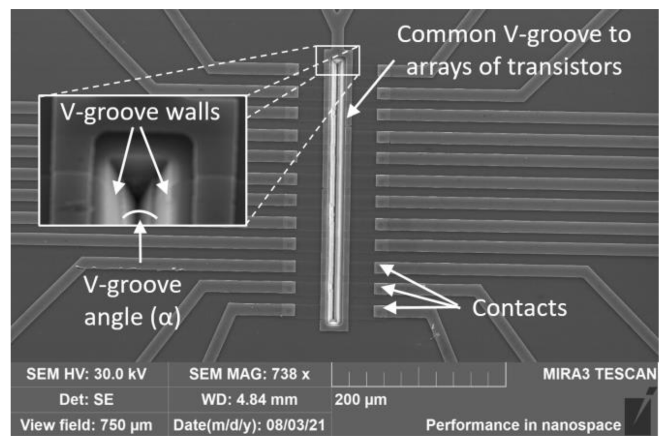

Fig. 8. Common V-groove for multiple transistors.

modes propagate; however, when they reach the straight guide section, only the fundamental mode survives, while the odd mode transforms into higher order modes and dissipates into the substrate [132]. A Y-junction with a low-difference refractive index (RI) and coupler as its input was designed and simulated. The simulation uses the Comsol Multi-Physics software package [81], allowing us to vary crucial parameters as shown in Fig. 5.

Optimization analysis was for single mode design in order to achieve a maximum input area error while preserving a good 50-50 splitting ratio. Combined design and simulations of Y-junctions can benefit and predict advanced optical communication. The coupling continues even after the junction split-up (Fig. 6).

3) V-groove Aperture in Photonic Modulators: The V-groove shape was first used in the past for the purpose of fabricating waveguides with Bragg grating filters [62] using nanoimprint lithography. When compared to the original attempts of light confinement, the idea of V-groove aperture usage was later re-applied in the domain of light absorption. The Silicon-On-Insulator Photo-Activated Modulator device (SOIPAM) [133] is a silicon photonic modulator, which acts as well as a light detector. The signal passing through is an electric current, which is controlled by illumination (Fig. 7) [134]. The current is transmitted only when the device is unilluminated (i.e., normally ON), and is blocked when there is enough incident illumination (OFF). It is composed of a p-type silicon substrate, a Buried Oxide (BOX) insulator layer above, and an n-type silicon channel at the top. A positive drain voltage is applied above the channel, while a negative gate voltage is applied to the substrate. Without illumination, minority electrons accumulate under the BOX near the channel, and the electrostatic forces turn the channel into a partial depletion region but allows the channel current to flow.

When illuminated, excess charge carriers are created, which causes more electrons to accumulate under the BOX and thereby increase the channel shortage layer, closing the channel. To optimize the number of absorbed photons, the illuminated area in the device is shaped as a V-groove (Figs. 7 and 8), so that more charge carriers will be generated for a given illumination power. The geometrical parameters of this device are optimized for the specific illumination wavelength. The interest in photo-activated silicon-based devices is constantly growing, and a presentation of alternative MOS devices was recently published, along with a description of the coupling of electronic and optical properties. [133], [135].

4) V-groove Aperture in Polarization Modulators: A further derivative of the above concept is a device which includes a polarization trigger. The V-groove embedded in the device enhances sensitivity to the polarization of the photonic control

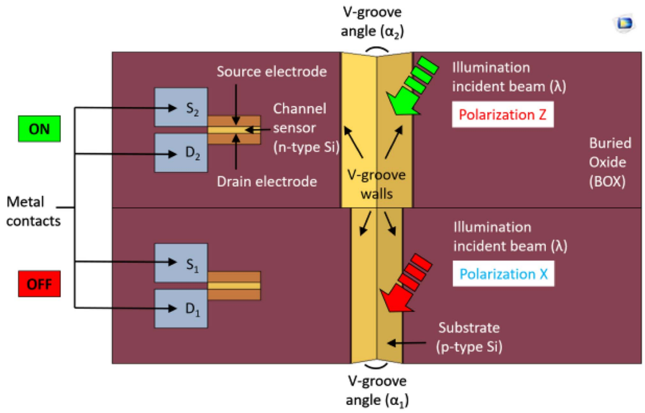

Fig. 9. Two adjacent SOIPAM for polarization trigger mode.

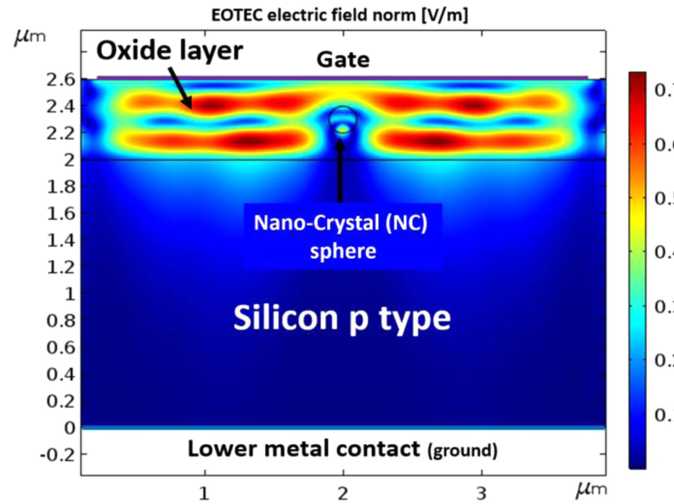

Fig. 10. EOTEC device presenting the electric component distribution of the incident light for specific wavelength.

signal, and thus works as a polarization sensitive modulator [136]. Put differently, this device acts as a polarizing transistor. The data in this device is electronic while the modulation control is optical. It can be used as a building block for the development of optical data processing by silicon-based processors based on typical microelectronics manufacturing process. When several V-groove based devices, each possessing different aperture angles, are placed adjacent to each other, we can implement a polarization selection (Fig. 9).

Through combining several adjacent structures (Fig. 9), one can obtain an Optical Polarization Sensitive Ultra-Fast Switching and Photo-Electrical Device [137]. A possible application of this device is for encryption/decryption, as the strongest electrical responsivity is obtained only for a specific polarization of the illuminating beam: when the V-groove is sufficiently narrow, the device mainly responds to one polarization state exclusively, causing electrons to be generated only for incident light of that state. While the nature of the data remains electronic, the modulation control is optic, creating a photo-induced current depending on the polarization direction. This coupled device acts as a polarization modulator as well as an intensity modulator. The device can be implemented in different circuitry configurations, such as dual, triple, and multi-element.

5) Embedded nano-crystals in excited MOS Capacitors: The expected performance of an Enhanced Optical Tunable Excited Capacitor (EOTEC) [138], [139] has been studied as part of the larger effort to develop optoelectronic high-speed devices for optical communication. The influence of semiconductor nano/micro-crystal dots, embedded in a thick SiO_2 film grown on a silicon substrate, was analyzed as a function of several parameters such as the sweep rate, penetration depth, dot size (Fig. 10), and the various material properties of several elements. In fact, silicon and germanium nano-crystals can act as efficient light emitters since there is a quantum confinement effect. By embedding such NCs inside a MOS structure, it is possible to create efficient light emitting devices, which can be integrated into micro/nanoelectronics circuitry. Moving forward, one can obtain not only enhanced light emission but also enhanced absorption through the NCs, and in turn enhanced light confinement in waveguides and resonators. In summary, embedding nano-crystals will lead to enhanced optical properties in MOS devices. The specific improvements to performance and effects will depend on the size, shape, distribution, and depth location of the nano-crystals inside the insulator layer. The ion implantation process itself is challenging as it requires an excellent control over the energy and dosage, all while varying the above parameters to their desired levels.

We have previously numerically demonstrated the capability for faster optoelectronic responsivity in the future. The series of CV curves obtained enable a good forecast of possible usage and applications, such as in MOSFETs, tunable capacitors, memory units, and Boolean logic elements. In previous publications, the frequency dependence of the capacitance variation between dark and NIR modulated illumination conditions was measured for metal-oxide-semiconductor (MOS) structures with germanium nanocrystals (Ge-NC) embedded in a thick SiO_2 film grown on a Si substrate. The results have shown that the device is expected to be sensitive at high frequencies (up to 111 GHz), making it a good candidate for optoelectronic high speed use and for optical communication applications [139].

As mentioned, the proposed device can be used not only as an optically tunable capacitor or memory unit, but also as part of Boolean logic circuitry incorporating a cascade of several such devices (in serial and in parallel connection depending if one wishes to realize logic AND or logic OR functionality). Such logic circuitry will be a hybrid circuitry in which, for instance, two optical input signals are mixed together through the logic operation to generate an electrical output. The advantage of using a hybrid optical-electronic logic gate is related to faster responsivity of the gate, as no RC time latency (the time constant equals the product of resistance and capacitance of the structure) is anticipated in the case of an optical input control signal, as has been demonstrated. The next step under research is to implement silicon nano-crystals (Fig. 11), as opposed to the germanium ones used in the prototype.

Fig. 11 shows a 3D COMSOL simulation of the EOTEC device with an internal view of the four layers, including 30

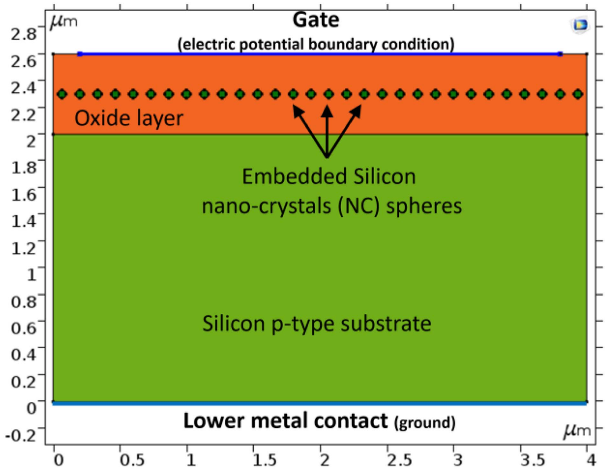

Fig. 11. EOTEC device sharing 30 embedded Si nanocrystals.

implanted micro/nano-crystals (NC) dots (radius = 20 nm) in ~~at~~ the middle of the oxide layer (depth = 500 nm). For better understanding of the layers, the upper metal contact has been reduced to a 1 μm square size in order to show the NC in the oxide layer. The Si-NCs are almost spherical, with diameters ranging from 4 to 10 nm. The diameter is largest in the center of the projection range, where the density of implanted Si atoms is the highest; the spatial distribution of Si-NC is almost symmetric with respect to the projection range position. The thickness of the Si-NC layer is about 110 nm.

6) Drilled Cylinder in dual-mode AFM-NSOM tip: In addition to customized silicon devices, capable of being integrated into CMOS technology, silicon photonics is also a desirable feature in stand-alone devices, particularly in the domain of sensing, scanning and super-resolution in the near-field. Combining the mechanical properties (topography) of an Atomic Force Microscope (AFM) silicon commercial tip with the imaging properties of a Near-Field Scanning Optical Microscope (NSOM) pipette was the next geometry-based step towards dual-mode scanning.

AFM scans a surface with a nanoscale tip in order to create a topographic mapping. When the tip, fabricated from n-doped crystalline silicon, is located at a nanometric distance from the surface, Van der Waals, Casimir, capillary, and electric and magnetic forces all act on it, causing the tip to be displaced from its regular position. The back of the tip is illuminated with a laser beam, and the reflected light picks up a phase change because of its movements, enabling interferometric measurement of the tip displacement and hence a topographical mapping of the surface.

Unlike AFM, NSOM provides an optical image (i.e., not a topographical/geometrical image) of the surface. The surface is illuminated by an external light source, in some cases via a hole bored in the tip itself. The tip extremity is significantly smaller than the optical wavelength, and it records the evanescent waves reflected from the surface by tiny spatial structures. These optical signals are conducted to the tip base using fiber optics, where they can then be transmitted to an optical detector, which results in an electrical signal proportional to the intensity of the light impinging on the tip. As the tip is moved over the surface,

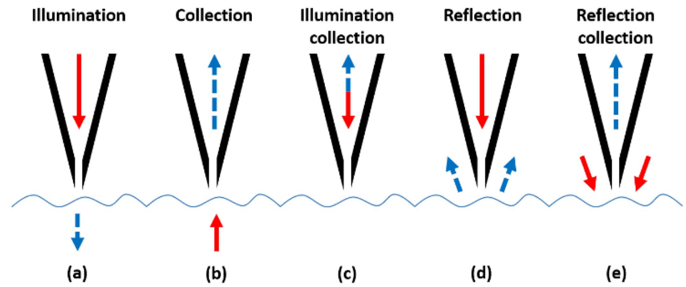

Fig. 12. Five main modes of NSOM operation: (a) illumination; (b) collection; (c) illumination-collection; (d) reflection; (e) reflection-collection.

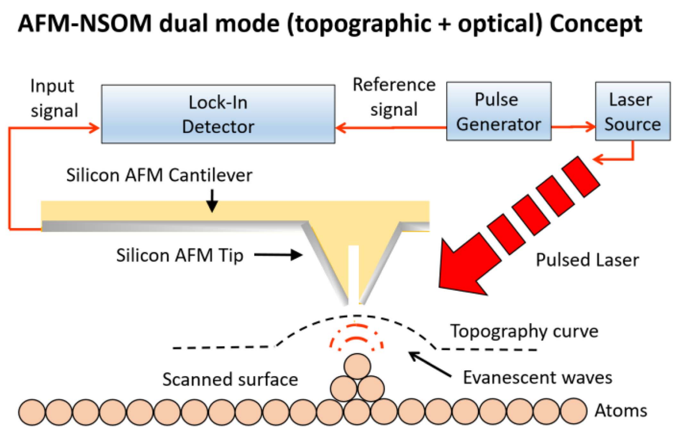

Fig. 13. AFM-NSOM combined device-sensing concept.

the optical reflectivity of the various features is measured at each point, which when combined form a complete image of the surface. NSOM measurements can be conducted in several modes, as presented in Fig. 12.

As noted, both types of microscopes provide nanometric information on the scanned sample, so both of them are widely employed in nanoscale measurements. However, it is very difficult to synchronize/coordinate between them, as they provide two different types of information due to the different imaging methods. An additional problem shared by both methods is that they must be insulated from external vibrations due to their principle of action. Moreover, NSOM has a low optical efficiency since the coupling of the evanescent waves to the extremity of the tip and the light transmission is a non-efficient energy process.

The unified AFM-NSOM tip project (Fig. 13) aims to address all of the above-mentioned problems [140], [141]. By combining the two tips into one and integrating the two microscopes into a single system, we can obtain both types of mappings simultaneously without having to worry about coordination - we can simultaneously obtain two different and complementary readings from each scanned point. The integration into one instrument significantly reduces the complexity of dealing with external vibrations, as we only have to worry about compensating for the one tip. In addition, we propose placing a nanoscale Schottky photodiode at the extremity of the scanning tip (Fig. 14), which will immediately convert the waves picked up there into electrical signals. This will result in much greater efficiency than in a

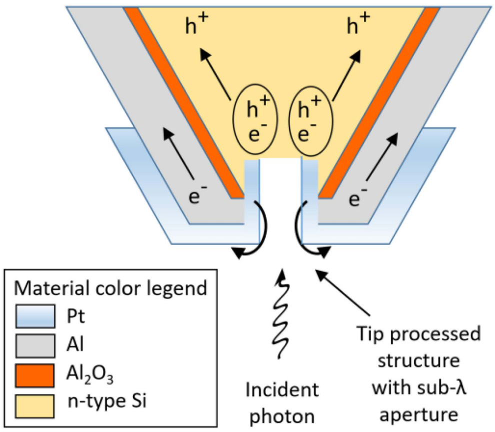

Fig. 14. AFM-NSOM combined device physical mechanisms: absorbed photons enter the tip aperture and create pairs electron-hole pairs, which are separated into two distinct currents.

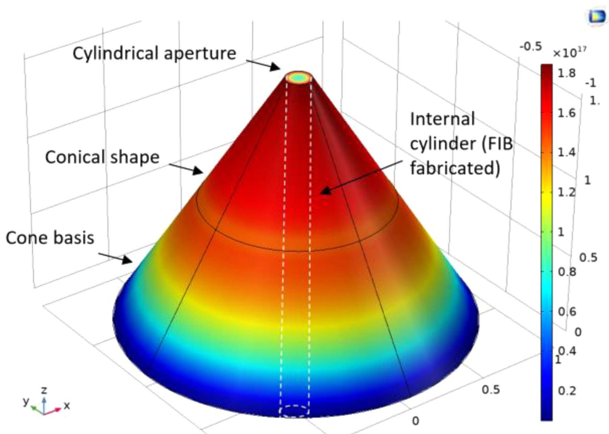

Fig. 15. Comsol simulation of the electrons concentration over the drilled-out cone of the combined AFM-NSOM device.

system using a regular NSOM tip, as we eliminate the need for the coupling of evanescent waves and their transmission via a fiber optic.

A large series of simulations (Fig. 15) were performed before the fabrication of the dual-mode tips using commercial AFM tips (Fig. 16).

Another point worth noting is the advantages of this method compared to apertureless NSOM (also called s-SNOM). It has been shown that this technique can also realize both topographical and optical measurement with a high resolution [142]. However, apertureless s-SNOM has a few drawbacks that make it difficult to work with. The primary one is that the signal has to be extracted from large background noise [143] using very precise methods, including a lock-in amplifier filter, non-linear and linear background suppression [144], focusing of the illumination in a very tiny area around the tip to reduce the background effect, and more. Precisely adjusting these features usually takes several hours at the least. However, in the AFM-NSOM concept, the tip itself is used as a detector, and there is with no need for drastic adjustment of the optical illumination as there is no background signal. Moreover, one of the reasons that s-SNOM is preferred

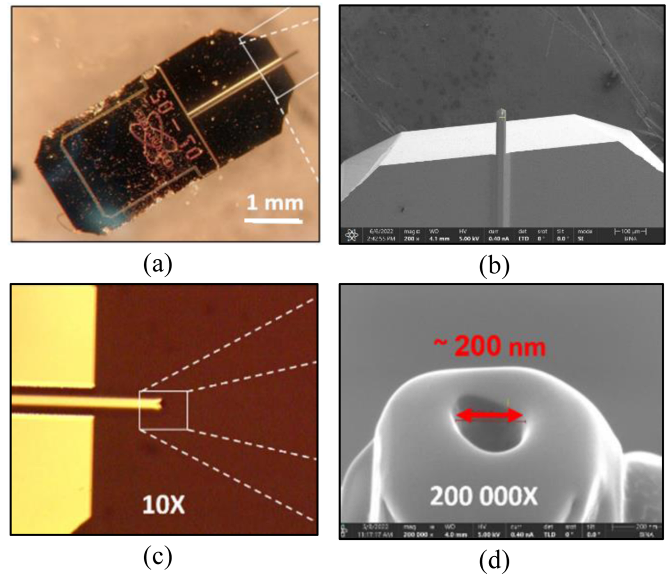

Fig. 16. AFM-NSOM combined device. (a) Commercial silicon-based chip; (b) SEM bird's eye view of the cantilever part; (c) Zoom-in of the cantilever part; (d) SEM high magnification bird's eye view of the drilled tip after FIB processing.

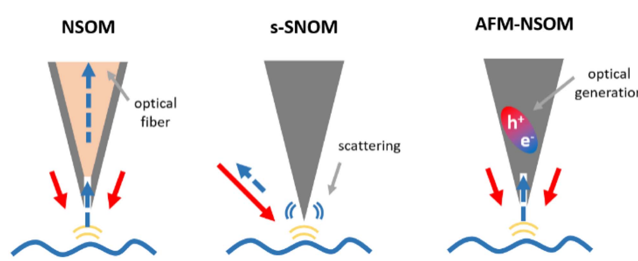

Fig. 17. Schematic representation of the operation principle for the three main near-field optical methods.

TABLE II
THREE MAIN NEAR-FIELD OPTICAL METHODS COMPARISON

	Backgrou nd signal	**Wavelength limitation**	**Optical adjustment**	**Dual mode**
NSOM	Low	High	Easy	No
s-SNOM	High	Low	Hard	Yes
AFM-NSOM	Low	Medium	Easy	Yes

to common NSOM methods is that the usable wavelengths are limited by the properties of the fiber optics used to transmit the collected signal from the tip. As the AFM-NSOM device transmits said signal without the use of an optical fiber, this issue does not exist, and any wavelength can theoretically be measured, depending on the Schottky barrier. Fig. 17 and Table II compare some of the main features of the different NSOM methods.

7) Plasmonic devices in near-field super-resolution: Plasmonic devices are part of the broader effort to develop exclusively silicon photonic devices. In this case, the main domain of applications will be surface sensing and scanning activities in the near-field range. New types of scanning tips [145] and of imaging modes [146] may aid in the advancement of super-resolution techniques for viewing nanoscale features on surfaces. Some techniques employ Localized Surface Plasmon (LSP) generated at the top of the tip. These Tip-Enhanced Fluorescence (TEF) techniques rely on the coupling between the absorption band of fluorophore and localized surface Plasmon resonance of the tip-substrate system [147], [148], [149]. Recently several new types of silicon tips based on Plasmon resonance energy transfer were developed [150].

8) Extended Family of Shape-Adapted Nano-Devices: The case studies presented above represent only a few out of dozens of devices developed by our team whose special shapes and geometries enable the usage of silicon despite its inherent limitations. As discussed above, there is a need to create a full family of new silicon nanoscale photonic components which can be smoothly integrated into the microelectronics industry. Several research teams around the world have developed stand-alone devices to address particular needs, and our team is specialized in the modelling and the simulations of such components [118]. Over the years, our team has simulated and developed a series of such devices, coupling both electrical and optical properties: light-emitting transistors [151], nano-amplifiers [152], capacitors with embedded nano-crystals [138], [139] photo-activated [133] and thermo-activated [153] modulators, polarized-photo-activated modulators [136], [137], nano-polarimeters [154], Y-junction waveguides [131], and more. The beneficial effects of these devices will be felt in many fields: optical communication, space and airborne sensors, and smart autonomous vehicle (SAV) sensors. Table III presents a list of the top devices, some of which have been developed in collaboration with other institutes worldwide. These nanoscale devices are classified per their initial nature. For example, one can identify light emitting devices, light absorbing devices, waveguides, sensors, modulators, super-resolution and near-field scanning devices, arrays, detectors, and nanoelectronics stand-alone components. Only a few of the silicon-based ones were presented in the above sections, since each one of them shares a special adapted shape and geometry.

TABLE III
NANOPHOTONICS DEVICES SHARING ADAPTED SHAPES

	#	Device acronym	Device definition	Device function
Light Emission	01	**MOSQWELL** [125] [151]	Metal-Oxide Semiconductor Quantum Well	Light Emitting Transistor
	02	**LENS**	Light Emitting Nano-pixels Structure	High-Resolution Display pixel
	03	**LENA** [modelling]	Light Emitting Nano-pixels Array	High-Resolution Display array
Nanoelectronics	04	**HAND** [152]	Hall Amplifier Nanoscale Device	Nano-amplifier working at THz
	05	**MOSEXCAP** [155]	MOS Excited Capacitor sharing regular layers	Fast response Capacitor
	06	**EOTEC** [138] [139]	Enhanced Optical Tunable Excited Capacitor sharing embedded nano-crystals (NC)	Ultra-fast response Capacitor
Super-resolution Sensing	07	**NSOM**	Near-field Scanning Optical Microscope	Pyramid-shape photodetector tip
	08	**NSOM-AFM** [140] [141]	Combined NSOM & AFM Photodetector	Dual-mode NSOM-AFM Sensor
	09	**NANOPOL** [154]	Nanoscale Polarimeter	Filtering Near-Field Polarization
	10	**NAP**	Combined NSOM, AFM and Polarimeter Nano-Detector	Triple-mode NSOM-AFM-Polarization Sensor
Trigger Activated Modulators	11	**SOIPAM** [133]	SOI Photo-Activated Modulator	Light Modulator
	12	**SOITAM** [153]	SOI Thermo-Activated Modulator	Thermal Modulator
	13	**SOIP^{2}AM** [136] [137]	SOI Photo-Polarized-Activated Modulator	Polarization Modulator
	14	**N-SOIXAM**	Multiple (N) connected SOI Triggered (X) Activated Modulators	Combined V-groove Modulators in active Circuitry
Raman	15	**SERS** [156] [157]	Surface Enhanced Raman Scanning	Nano sensor array for Raman pH Imager
	16	**TERS** [157]	Tip-Enhanced Raman Spectroscopy	Raman Surface Scanner
Guides	17	**PAINT** [131]	Phase And Intensity Trace	Y-Junction Waveguide
	18	**OPTICON** [modelling]	Optical Interconnects	Optical routing in silicon
Detectors	19	**NA^{2}OD** [modelling]	Nano-Antenna Acousto-Optic Detector	Acousto-Optic Detector
	20	**NRSD** [modelling]	Nano-Rod Sensing Device	Resonance Detector

III. FROM SINGLE DEVICES TO MODULES AND PLATFORMS

A. *Nomenclature*

Along the review, in order to develop our approach to overcome silicon photonics limitations, we used several similar expressions such as “architecture,“ ”structure,“ ”shape,“ and ”geometry", which appear to be related terms. In fact, they have distinct meanings. To clarify the meaning of each word, we summarize hereby the spirit of each expression, and the differences between them:

Architecture is a well-known term, coming from the microelectronics industry world, and which refers to a whole package of design rules and dimensions defining a new technology used for a new microprocessor or other product [158]. The architecture is designed to meet the challenging requirements of the customers for specific applications [159]. For example, the term Intel Architecture refers to a combination of microprocessors and complementary hardware, which creates the building blocks for a variety of computing systems [160]. It may consider factors such as functionality, performance, efficiency, and more. Moreover, a new model, entitled “tick-tock” and started by Intel Corporation in 2007, defined that every microarchitecture change (“tock”) will be followed by a shrink of the process technology (“tick”). In such a way, there is a continuous improvement of the design rules and dimensions to obtain faster microprocessors. When we use the term “architecture” in this review, we intend to define a set of rules and approach to be used towards the

TABLE IV
DEVELOPMENT FLOW OF THE PROPOSED SHAPE-ADAPTED AND GEOMETRY-BASED STRATEGY

Innovation levels	Applications or examples
Geometric Based Structures	• Quantum Well (QW) • Quantum Wire (QWR) • Quantum Dot (QD) or Nano-Crystal (NC) • V-groove Aperture (VGA) • Embedded Drilled Cylinder (EDC) • …
Photonics Stand-alone Devices	• Embedded QW in lighting transistor (MOSQWELL) • Embedded NC in MOS capacitor (EOTEC) • Embedded VGA in modulator (SOIPAM) • Embedded drilled cylinder in sensor (AFM-NSOM) • Quantum-cascade lasers (QCLs) • …
Photonics Modules	• Transceiver photonic module • Multi-spectral sensing module • Optical buffers • Optical amplifier module • Optical switching module • Optical sensor module • Quantum computing module • Boolean Gates • …
Photonics Platforms	• Silicon-On-Insulator (SOI, SiO_2) • Silicon-Nitride (Si_3N_4) • Indium Phosphide (InP) • Germanium-on-Silicon (Ge-on-Si) • Hybrid Integration
Photonics Integration Mode	• Commercial wafers with separated areas (MPW) • Heterogeneous integration • Monolithic integration • Product Design Kit (PDK)

geometry-oriented design and realization of series of new silicon photonic devices and modules.

The term "structure" represents here the "basic cell" to be embedded into the designed silicon photonic device. In our approach, we define five levels of silicon photonic design, as presented in Fig. 1(b), and the structure is the lowest one. The structure is usually the game-changer of the device. Many of the structures are quantum-based elements, such as quantum dots (QD), quantum wires (QWR), quantum well (QW). An example of such a structure is the SiO_2/Si/SiO_2 QW embedded in the channel of the MOSQWELL transistor presented later [151]. Its presence in the path of the channel, between the source and the drain connections, will allow hot electrons to reach discrete levels of energy inside the conduction band, and as consequence will enable permitted intra-sub-band transitions (ISBT) with radiative recombination. Sometimes, the structure will consist in a special contour of polygon, like the V-groove shape in SOIPAM device [136], or the Gate-Recessed-Channel (GRC) silhouette in the MOSQWELL one [126]. The structure term is outlined further described in Table IV, which shows the definitions of the five levels of components.

At the end, the term "geometry" represents the essence of this review article. Geometry includes the shape design (circular, rectangular, other polygon etc.) of the basic structure (i.e., a V-groove silhouette for an aperture in modulators, a step function profile for Gate-Recessed-Channel in quantum photonic transistor, etc.) the dimensions, the layers thickness and the embedded shapes of a device. Since the term originates in mathematics, it deals with the properties and relationships of points, lines, curves, shapes, and spaces. In our context, it refers to the mathematical description of devices' spatial properties, such as dimensions, angles, curves, and surfaces. It is the term used in numerical work of simulations.

B. Photonics Modules As Building Blocks

Moving ahead, one can conceive of several modules, based on the above proposed set of devices and applications. Each module is a building block, which groups several functions into one full circuitry (Table IV). This emphasizes the capability of these components to act not only as separate unique photonic devices, with desirable properties applicable to the field of photonic processing, but also to be integrated into "low hanging fruit" prototypes for realistic photonic processing applications. The issue of integrating different devices into a module is not a trivial task since different players can fabricate the devices separately, even on different wafers, so they need to be assembled into a unified and functional module in order to be tested and characterized. In order to allow such module-based integration flexibility, the intention is to use a heterogeneous rather than monolithic approach to the fabrication [161] process; however, hybrid integration approaches can be evaluated too – such as silicon Nitride (SiN) photonic technology based on Silicon-On-Insulator (SOI) substrates. In this approach, one can also fabricate each device on a separate photonic chip, and each such chip will also include optical waveguides and couplings to optical fibers. The fibers will in turn be connected to optical connectors, and through those fibers, we intend to facilitate the required optical coupling interface between the different chips and to connect them into a single functional module. In such a case, the focus will be on Smart Vision – i.e., optical acquisition – and not data processing.

Many of the above presented devices can be integrated as a "module" (full function), as presented in Table IV and Fig. 18, before integration into Photonics Integrated Circuits (PICs). There are many examples of photonics modules (i.e., modules in which photonic devices are embedded), which are commonly used in optical communication and sensing systems. Among others, one can find transceiver photonic modules (both transmitter and receiver components in a single package), multi-spectral sensing modules (circuitry containing an array of various detectors capable of sensing many wavelengths), electro-optic modulators, optical buffers (optical memory buffer), optical amplifier modules, optical switching modules, optical sensor modules, quantum computing modules (on-chip time bin entangled photons in miniature photonic structures [162], and many more.

Each one of these proposed modules is based on the connection of photonic devices and additional components to form

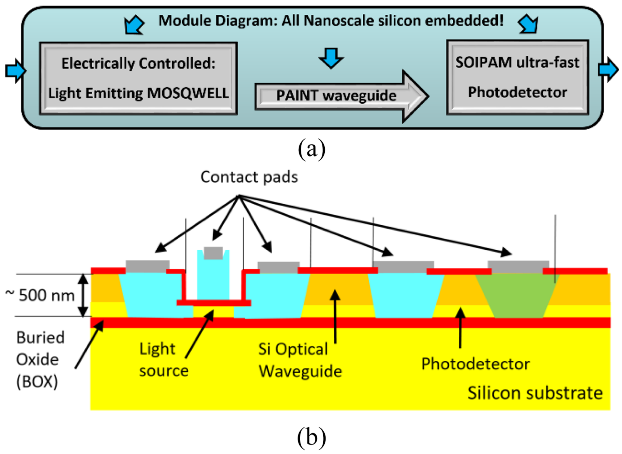

Fig. 18. Module block diagram including several only silicon devices: Waveguide (PAINT) between MOSQWELL Inter Sub Band Transition Light emitter and SOIPAM modulator. (a) Concept; (b) Planar fabrication process (cross section view).

a unified circuitry. Of course, the above examples are just a few examples of the functionalities that can be created, and the specific components and functionalities to be integrated into a module will depend on the intended application and system requirements. The modules provide a convenient way to package and interface photonic devices, making them easier to integrate into optical systems and facilitating their use in practical applications.

C. Full Technology Flow

However, the design, development and fabrication of photonic modules remains a difficult challenge due to the many concurrent limitations and requirements that must be fulfilled in order to group multiple devices into one compact circuitry. For example, concerns and considerations may arise in regards to integration and packaging (into a compact module), alignment and assembly accuracy (of waveguides and other components), thermal management, proper compatible connectivity, process steps (accurate photolithography and layers deposition), survival in challenging environments (military, space, defense), electrical interfaces to other components, quality and reliability parameters (lifetime, stress conditions, humidity, temperature and pressure, degradation), and of course cost (strong yield and reliability), as well as time constraints. In addition, since fabrication involves hybrid integration, these modules also require highly qualified personnel with experience in multiple disciplines, such as electronics, photonics, quality and reliability, packaging, and more.

As mentioned above, with our approach, we strongly recommend developing a full technology flow, which will include the five main relevant steps: 1) structure, 2) device, 3) module, 4) platform, and 5) Multi-Project Wafer (MPW) [163].

D. Compatible Platforms

The next challenge after fabricating the structures, devices and modules is the proper choice of platform. Not all existing platforms and foundries enable smooth integration of developed devices [164], [165], and there are many parameters which need to be considered. Today, the domain of photonics platforms is well developed; for example, the Scientific Community has access to a series of industrial photonics platforms [166]. These have been developed by leading research institutions and private companies worldwide through Multi-Project Wafer (MPW) schemes [163], like those offered by the Europractice IC service, which offer a broad set of Si-photonic technologies which can be used for the smooth integration of devices and modules. The win-win situation of combining and integrating some of the newly-designed building blocks into standard platforms can open new markets for these institutions and bring additional synergies into the industrial and academic worlds. Worldwide silicon photonics foundries enable available silicon photonics platforms that should be considered for a future integration of products. Since silicon photonics is a technology that uses silicon as a platform for the integration of optical devices and electronics on a single chip, there are several silicon photonics platforms that are currently being used or have been proposed for future integration of products, some specialized for Mid-Infra-Red (MIR) applications [89], [167] and devices [168]. Some of the most important existing platforms today are:

1) *Silicon-on-Insulator (SOI) platform* – This platform uses a silicon wafer with a layer of buried oxide (BOX) that serves as an insulator. The silicon layer is used for the optical devices, while the BOX layer isolates the optical devices from the electronic devices. Among the existing SOI platforms, some offer the best performance for Si passive and high-speed active devices, among others [169]. As an example, one can cite the silicon electro-optic Mach-Zehnder modulators (MZMs) and germanium photo-detectors, complemented with additional modules for thermal tuning capability trough metal heaters, Complementary Metal-Oxide-Semiconductor (CMOS) metallization levels for optimal routing compatible with back-end treatments as Under Bump Metallization (for hybrid integration with CMOS logic through flip-chip mounting), or micromachining of handle wafers for passive fiber edge-coupling. Other SOI platforms exist with similar photonic capabilities, but also provide a monolithic integration of CMOS logic to allow the co-integration of electronic and photonic components. This is the case of IHP using a Silicon-Germanium (SiGe), Bipolar CMOS (BiCMOS) process and Global Foundry (GF) using a 90 nm SOI CMOS process).
2) *Silicon Nitride (SiN) platform* – This platform uses a silicon nitride layer as the waveguide material, and can support a wide range of applications [170]. The advantage of this platform is that it has a higher nonlinearity compared to silicon, which can be useful for applications such as frequency comb generation. The platform offers

the possibility of two depth levels for SiN etch, allowing for fabrication of components such as strip waveguides, rib waveguides, shallow and fully etched grating couplers etc. These platforms are especially useful in the visible (VIS), Near Infra-Red (NIR) and Mid-Infra-Red (MIR) ranges [165], [171], and allow the selective removal of cladding from waveguides for micro-fluidic channels and sensing zones etc. They also offer several metal layers for functions such as thermo-optic tuning, electrical inter-connects etc., and can integrate trench etch for devices such as edge couplers.

3) *Indium Phosphide (InP) platform* [46] – This platform uses a semiconductor material that has a higher index of refraction than silicon. It is commonly used for the fabrication of lasers, polarization beam splitters (PBS) [172], photodetectors, and high power Photonics Integrated Circuits (PICs) [173], [174]. Moreover, a dedicated platform already exists for the manufacturing of such devices [175].
4) *Germanium-on-Silicon (Ge-on-Si) platform* – This platform uses germanium as the waveguide material on a silicon substrate. The advantage of this platform is that it has a high refractive index, which can be useful for applications such as waveguides [176] and wavelength division multiplexing (WDM) [55].
5) *Hybrid Integration platform* – This approach toward silicon photonics combines different materials and platforms. Among others, one can find the association of silicon and InP, integration of III-V compounds [177], and organic parts to take advantage of their respective properties [178]. This approach can be useful for applications such as high-speed modulators and detectors.

Ultimately, the choice of platform will depend on the specific requirements of the application and the trade-offs between performance, cost, and ease of fabrication.

E. Technology Readiness Level (TRL)

Photonics has been offering significant advantages, which are associated with its much larger bandwidth of information (leading to higher data processing rates), its reduced power dissipation, and its smaller crosstalk occurring between close channels of optical data transmission, in respect to what is obtainable with conventional microelectronics processing circuits. This is why photonics could and should be a game changing factor, a significant tool that can complement electronic processing circuitry and solve bottlenecks that electronic processors are struggling to cope with. Such a dream has motivated large number of scientists and engineers around the world in the last decades to try and establish monolithic photonic processing circuitry. However, those attempts have not yet matured to sufficiently high-level technological maturity. This is why it is also crucial to develop guidelines for ~~to~~ moving from devices to systems in the industry. Such a well-established bridge between science and engineering will enable new technologies to develop in a smooth, cohesive way. One of the metrics for qualifying success in the long path towards the development of nanophotonic stand-alone devices, modules and platforms is the technology readiness level (TRL) of each component towards its possible integration into a higher level of circuitry. Table V presents the TRL standard scale.

TABLE V
TECHNOLOGY READINESS LEVELS (TRL) STANDARD SCALE

TRL ID	TRL simplified definition
TRL 1	Basic research
TRL 2	Technology formulation
TRL 3	Proof-of-concept
TRL 4	Small-scale prototype (validation in lab)
TRL 5	Large-scale prototype (validation in relevant environment)
TRL 6	Prototype system (demo in relevant environment)
TRL 7	Demonstration system (operational environment)
TRL 8	System completed and qualified
TRL 9	Full commercial application

TABLE VI
QUALITATIVE CRITERIA COMPARISON BETWEEN ELECTRONIC AND PHOTONIC DEVICES

Criteria	Electronics Devices	Silicon Photonics Devices
Speed	• Switching speed • Clock speed • Intra-chip communication	• Modulation speed • Transfer data rate • Intra-chip communication
Space	Regularly larger dies	Smaller dies, less metal
Cost	Higher cost	Lower cost (since less area, less metal lines, etc…)
Size	Per technology	Nanoscale
Power	Higher consumption	Lower consumption
Failure Mechanisms	Metal Interconnect crash: • Electro-Migration (EM) • Self-Heating SH)	No metal interconnect failures. Silicon/dielectric waveguides (WG)
Integration and compatibility	• CMOS Technology • Fully VLSI	• CMOS Technology • Fully VLSI • Starting material based on SOI/SiN technology • Multiple platforms option
Main added values	• Less complex to design • Less limited functionality • Traditional electronic devices are usually less expensive in low volume production runs • Less sensitive to environmental factors such as temperature and vibration which can affect the performances of the photonics devices	• Area reduction • Multi-mode device (electrical + optical) • Optical interconnect between/inside blocks • Low time delay by limiting metal lines number • Free area increase / chip • Clock frequency rate Increase • Modulated channel mobility due to QW structure • Electrically controlled light emission • Translatable to industrial architecture

IV. DISCUSSION

A. Criteria for Industrial Integration of Silicon Photonic Devices

The silicon photonics domain enables many advantages when compared to the regular microelectronics world, as presented in Table VI. Of course, not all the shaped adapted devices are viable candidates for integration into modules and/or platforms. Many research teams developed a stand-alone solution for a particular application, without necessarily considering the long-term need for circuitry integration. One can find unusual shapes developed over the years by several research teams in order to deal with highly specific constraints. However, large integration of vertical components into an array or an additional circuitry can include some fabrication risks and a low-yield of success. The same caveat applies to the AFM-NSOM combined dual-mode devices discussed above. From a quality and reliability (Q&R) point of view, it is usually more conventional to build horizontal planar arrays and circuits than vertical-made shapes.

In terms of the power consumption metric, silicon photonics devices have the potential, depending on the type of application, to use less power than electronic devices. Since silicon photonics devices use light (photons), it enables faster data transport and communication while consuming less power than electronic devices' usage of electrons. For instance, it can be utilized in data center applications to convey high-speed data between servers and other computing components. In this case, they may use less power than conventional electronic copper-based interconnects, which have the potential to suffer from signal loss and need more power to operate at greater speeds. Of course, device's power usage will depend on on many factors, such as the specific technology used, the operating frequency, and the application.

Regarding the possible applications, silicon photonics can definitely bring opportunities that microelectronics will not be capable of competing with. Among others, one can identify optical coding, which is more difficult to break and more desirable for defence and space purposes than electronics' coding. Mixed signal (optical and electronics in parallel) is also an option. One can find additional options such as the skew clock, parallel calculations, high-speed applications, I/Os, buses, low power, and of course area reduction. Regarding the optical interconnect, there are multiple ways to do so: between device to device, block to block and integrated circuit to another one (IC to IC). Silicon photonic devices (SPD) share several advantages, such as:

- *Dimensions:* Their small size makes them suitable in situations with limited space because they are typically based on nanoscale form dimensions or quantum structures.
- *Compatibility:* Devices can be manufactured with similar processes used in microelectronics. This makes them easier to integrate into hybrid chips.
- *High-speed:* Data transfer at very high speeds is a key parameter, which makes them suitable for use in applications requiring fast data transfer rates such as optical communication.
- *Low power:* When compared to traditional electronic devices, SPD can also consume less power than, particularly over long distances. Indeed, light signals experience less attenuation than electrical signals, meaning they can travel further without requiring additional power.

However, some constraints reflect disadvantages in these silicon photonic devices:

- *Complexity:* Since SPDs can be more complex than electrical ones, especially when it comes to developing and manufacturing the essential components, they can be fairly difficult to build. They are more challenging to develop and produce because to their intricacy.
- *High cost:* Manufacturing SPDs can currently be more expensive than producing typical electronic devices, especially for small quantities.
- *Functionality:* While SPDs can transfer and communicate data, they are not yet ready to process it, which restricts their capability and available uses.
- *Sensitivity:* Finally, one may consider that they can be sensitive to external factors such as temperature and vibration, which can affect their performance. It makes them more challenging to use in severe environments and applications, such as military and space.

If the above comparison to standard microelectronics is important, then comparison to any other well-established technology, such as Micro Electronic Mechanical Systems (MEMS), is also desirable. Due to their tiny dimensions and challenging adapted shapes, it appears that, when compared to MEMS, the nanoelectronics and nanophotonics devices still require more solid and mature technologies as well as long-term planning before they can feasibly achieve large-scale functionality. While MEMS dimensions mainly allow combining both mechanical and electrical components fabricated using semiconductor fabrication techniques, the nanoscale focuses more on photonics properties. In fact, some MEMS developments included photonics aspects as well [179], [180]. Recently, an interesting study emphasized the stretchable properties of silicon photonics [181]. It appears that mechanically stretchable photonics~~,~~ may provide a new geometric degree of freedom for photonic system design without significant degradation processes. Once again, mechanics and photonics properties can live together.

B. Impact Forecast

Assuming a feasible and mature integration process, the main objective remaining is to establish a new sustainable value chain of silicon-based opto-electronic components with industrial value. One can expect a substantial increase in the market for the number of products and services enabled by integrating our innovative components across sectors with state-of-the-art innovative technologies, able to generate growth and new jobs.

While nano-photonics has its road map of evolution, our interface to it involves the capability of developing useful processing modules. These modules share increased integration density, increased operation speed and reduced power consumption per processing operation. This is obtained while reducing the complexity of the fabrication process (e.g., by realizing light emission without requiring III-V materials), matching the proposed Research and Development (R&D) process with industrial partners who are capable of using it and taking it to higher TRL levels, and enhancing the fruitful interface between academia and industry. Moreover, this will bring benefit to real-need processing and connectivity (data exchange) challenges that our world is currently facing. The proposed approach will enhance industry's potential to take advantage of market opportunities and establish leadership in the field, as well as boost business activity. The results will also be available for commercial purposes.

It is anticipated that the Photonics Integrated Circuits (PICs) market will increase from a value of USD 478 million in 2019 to reach USD 2.266 billion by 2026 [182]. Moreover, large research and development (R&D) costs are also incurred by academic institutions, which are not reflected in these numbers. One can obtain silicon-based photonics benefits from several key players: mature CMOS foundries (200 mm/300 mm wafer size), advanced Si patterning capability (nanometer scale accuracy), volume scalability ($>$ 1M units/year) with cost efficiencies of scale, and wafer-scale 3D packaging, assembly and test (TSVs, micro-bumps). These are some of the advantages, in respect to the PIC based on other materials such as Indium Phosphide, or Gallium Arsenide.

Integrating multiple Integrated Circuits (ICs), the System in Package (SiP) [183], supports passive devices in a single package. It powers the semiconductor manufacturing processes and silicon die to create a tightly coupled module. Sharing a dual nature, it is a system from design perspective, and a component from the construction one. On the other hand, the SiP does not allow monolithic integrated optical gain/lasing, which is usually overcome by hybrid or heterogeneous integration with active components based on III-V materials. This represents a major cost increase on integration. Solutions to be pursued are to increase the collimation length of silicon based light sources in order to bypass these limitations. Other SiP characteristics that impair its development relate to limitations on performance of modulators and similar building blocks. Again, amongst the variety of devices pursued, different modulator approaches must be explored.

V. Conclusion

At the nanoscale range, electronics and photonics are forging ahead using advanced technologies and architectures. Structures, devices, modules, platforms and kits are the main milestones in the integration path. While researchers have focused on attempts to replace silicon with alternative materials from the periodic table, we suggest sticking to the irreplaceable element and compensating for its limitations through adapted shapes and special geometries, as the case demands. Of course, even if such solutions are feasible for stand-alone devices, they may require additional adaptations to make them practical for higher levels of modules and platform integration. This review presented some creative thinking applied to light emitting and light receiving silicon based components at the nanoscale.

Acknowledgment

The author would like to express his deep gratitude to his students – ALEO research team members – who developed the devices along the years, as well as to his mentor when he was himself a student, Prof. Joseph Shappir at the *Hebrew University of Jerusalem* (HUJI). Lastly, the author would like to express his deep gratitude to research collaborators for brainstorming fruitful discussions along the years: Dr. Avraham Chelly and Prof. Zeev Zalevsky at the *Bar-Ilan University* (BIU), Dr. Alon Vardi at the *Massachusetts Institute of Technology* (MIT), Prof. Carlos Dominguez at the *Consejo Superior de Investigaciones Científicas, Institute of Microelectronics of Barcelona, Centre Nacional de Microelectronica* (CSIC IMB-CNM).

Disclosure: The author declares that he has no known competing financial interests or personal relationships that could have appeared to influence the work reported in this article.

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