

gave a live presentation and discussed their work with the audience. Based on the technical content, presentation skills and quality, innovation, and results, each of these six finalists was evaluated by a panel of experts who were present during the online competition.

Based on the ratings of the final presentations, the first three winners were selected to receive cash prizes:

- The first-place winner is Amina Whichi from CRNS, in Tunisia, and Leipzig University of Applied Sciences, Leipzig, Germany.

- The second-place winner is Kota Sanjeev Vishal from TU Chemnitz, Germany.
- The third-place winner is Wael Suliman from King Fahd University of Petroleum and Minerals, Saudi Arabia.

—Brahim Mezghani

IEEE SSCS Distinguished Lecturer Makoto Takamiya Gives a Talk at the Switzerland Chapter

The IEEE Solid-State Circuits Society (SSCS) Switzerland Chapter organized its first webinar of 2021, together with Prof. Makoto Takamiya from the University of Tokyo, Japan. Takamiya is a Distinguished Lecturer of the SSCS.

The event was advertised and reported using IEEE vTools, and 27 members enrolled. The slides are available from the same platform [1].

Digital Object Identifier 10.1109/MSSC.2021.3072260
Date of current version: 24 June 2021

The presentation was hosted through the WebEx platform of the IEEE Member and Geographic Activities Committee, and the recording is available on IEEE TV [2].

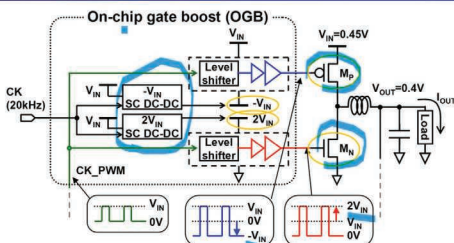
Takamiya started his lecture, “Integrated Power Management Circuits for Energy-Efficient Internet of Things (IoT) Systems,” by introducing a set of techniques published over key SSCS conferences, such as the IEEE International Solid-State Circuits Conference [3], [4], European Solid-State Circuits Conference [5], IEEE Symposium on

VLSI Circuits [6], IEEE Custom ICs Conference [7], and Asian Solid-State Circuits Conference [8]. The presentation took participants through, essentially, four main topics.

The first was an introduction to energy efficiency in IoT systems. This was followed with a discussion of techniques to handle low-voltage distribution with buck converters at low input voltage and large output range. There was an intermezzo on the clocking techniques adopted and, finally, a word on passive integration.

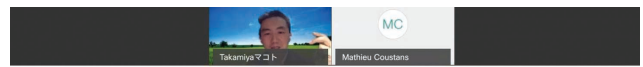


On-chip Gate Boost for Power Transistors

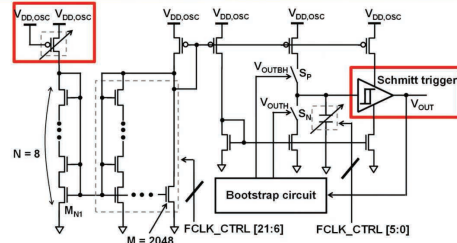


- 2 power rails are generated by on-chip switched-capacitor (SC) DC-DC converters.
- Loss in M_P and M_N is reduced.

Prof. Takamiya describes the on-chip gate boost technique applied in a dc-dc buck converter.



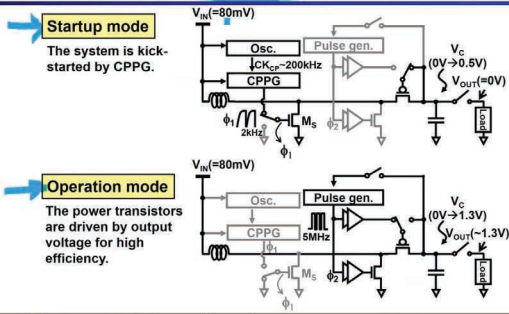
Leakage-Based DCO



- Power: proportional to the oscillating frequency
- No additional voltage reference
- Leakage current is designed as bias

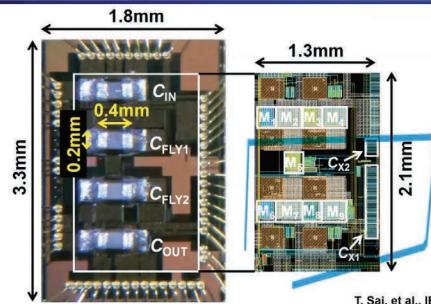
Prof. Takamiya explains the proposed architecture of the leakage-based DCO.

Dual Modes Operation



Prof. Takamiya presents a dual-mode-operation dc-dc converter that has a cold start from 80 mV.

Fabricated SC DC-DC Converter in 180nm



T. Sai, et al., IEEE TCAS II, 2018

Prof. Takamiya shows a switched-capacitor multiratio dc-dc converter leveraging the integration of surface-mounted capacitors.

Outline

- ◆ Energy-efficiency in IoT systems
- ◆ 0.45-V input buck converter
- ◆ Wide I_{OUT} buck converter
- ◆ 80-mV input boost converter
- ◆ Switched capacitor DC-DC converter
 - Integration of MLCCs on die
- ◆ Summary

An outline of Prof. Takamiya's presentation.

Summary

- ◆ Integrated power management circuits for energy-efficient IoT systems
- ◆ Gate boosting for low V_{IN} DC-DC converters
- ◆ Clocked comparator for low I_{OUT} buck converter
- ◆ Integration of MLCCs on die for SC DC-DC converter

Prof. Takamiya's summarizing slide.

While voltage scaling is interesting, it comes with a set of challenges, among which is to drive transistors as switches, with supply voltages close to the threshold of

the available devices. Takamiya explained the of on-chip gate boost.

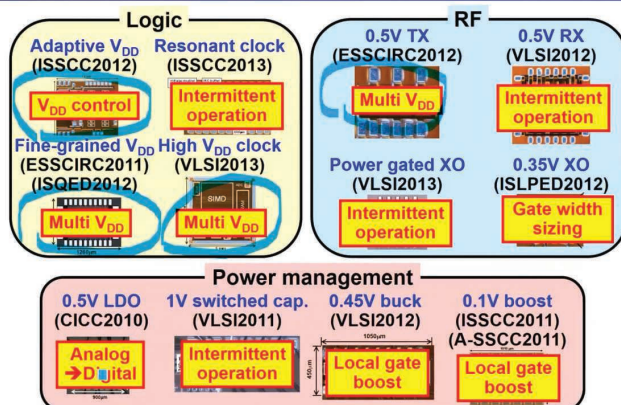
Takamiya also detailed the leakage-based digitally controlled oscillator (DCO) architecture, where a

single digital word enables one to control a precise-enough clock over a large span of operation. This type of oscillator is a key enabler for a wide range of output loads to maintain competitive efficiency, such as 87% over the load range spanning 500 nA–20 mA for a Bluetooth low-energy application.

Switching gears to the reverse operation, we find a key use case in the context of energy harvesting for dc sources, such as solar panels or thermoelectric generators, where the input voltage range is on the order of 100 mV and boost operation is needed. Finally, a couple of slides provided an update on passive integration techniques and the benefits of a surface-mounted capacitor, which brings high energy density within the same package.

The presentation led to a detailed question-and-answer session on oscillator techniques and the observed variability. Participant

Key Techniques for Sub-0.5V Circuits



Prof. Takamiya introduces his lecture and the key published techniques in the SSSC literature.

feedback was very positive, and attendees appreciated the breadth of the topics addressed.

—*Mathieu Coustans, Makoto Takamiya, Michel Bron, Domenico Pepe, and Taekwang Jang*

References

- [1] "IEEE Swiss SSC distinguished lecture (webinar)/integrated power management circuits for energy-efficient IoT systems," IEEE vTools, Jan. 28, 2021. <https://events.vtools.ieee.org/m/254880>
- [2] <https://ieeetv.ieee.org/video/ieee-switzerland-solid-state-circuit-society-webinar-january-2021-makoto-takamiya-integrated-power-management-circuits-for-energy-efficient-iot-system>
- [3] K. Hirairi et al., "13% Power reduction in 16b integer unit in 40nm CMOS by adaptive power supply voltage control with parity-based error prediction and detection (PEPD) and fully integrated digital LDO," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, 2012.
- [4] H. Fuketa M. Nomura, M. Takamiya, and T. Sakurai, "Intermittent resonant clocking enabling power reduction at any clock frequency for 0.37V 980kHz near-threshold logic circuits," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, 2013.
- [5] S. Iguchi Akira Saito, K. Watanabe, T. Sakurai, and M. Takamiya, "2.1 Times increase of drain efficiency by dual supply voltage scheme in 315MHz class-F power amplifier at output power of -20dBm," in *Proc. ESSCIRC (ESSCIRC)*, Bordeaux, France, 2012.
- [6] S. Iguchi A. Saito, Y. Zheng, K. Watanabe, T. Sakurai, and Makoto Takamiya, "93% power reduction by automatic self-power gating (ASPG) and multistage inverter for negative resistance (MINR) in 0.7V, 9.2μW, 39MHz crystal oscillator," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, 2013, pp. C142-C143.
- [7] P.-H. Chen et al., "0.18-V input charge pump with forward body biasing in start-up circuit using 65nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, 2010.
- [8] P. Chen et al., "A 80-mV input, fast startup dual-mode boost converter with charge-pumped pulse generator for energy harvesting," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Jeju, Korea (South), 2011.
- [9] IEEE Solid-State Circuits Society. *Basics of digital low-dropout (LDO) integrated voltage regulators—Presented by Mingo Seok*. (May 11, 2020). [Online Video]. Available: <https://www.youtube.com/watch?v=BwyjvP51UY0>

IEEE SSCS Poland Chapter Activities

The year 2020 enforced many remote-led activities throughout all aspects of our lives. The IEEE Solid-State Circuits Society (SSCS) Poland Chapter organized a series of interesting events with the help of the Distinguished Lecture program and other excellent invited speakers. As usual, the events gathered a substantial number of participants (50+) from science, the growing microelectronics industry in Poland, and students of microelectronics and biomedical engineering fields being taught at the AGH University of Science and Technology, Kraków, Poland.

One of the guest speakers was Dr. Gabriele Manganaro (MediaTek, United States), who discussed aspects of wideband IC design for wireless communications from the system down to the circuit levels, indicating crucial design constraints and key design choices together with their consequences. He pointed out the main analog-to-digital converter

Closed-Loop Neuromodulation

Dejan Marković
UCLA ECE Department
dejan@ucla.edu

CENT
Center for NeuroTechnology

Prof. Markovic explains the details of the biomedical system.

Mixed-signal technologies for ultra-wide band signal processing systems

IEEE SSCS DL 2020
Gabriele Manganaro

28nm 12b/10GSPS ADC: 8x int A/D

Dr. Manganaro, SSCS Distinguished Lecturer, introduces wideband signal processing systems and techniques.