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Through the Looking Glass—2020 Edition

Trends in solid-state circuits from ISSCC

The International Solid-State Circuits Conference (ISSCC) is the flagship conference of the IEEE Solid-State Circuits Society. The theme for ISSCC 2020 is "Integrated Circuits Powering the Artificial Intelligence (AI) Era." Advances in solid-state circuits and systems have brought ever more powerful communication and computational capabilities into mobile form factors. Such ubiquitous smart devices lie at the heart of a revolution shaping how we connect, collaborate, build relationships, and share information. These social technologies enable people to maintain connections and support networks not otherwise possible; they provide the ability to access information instantaneously and from any location, thereby helping to shape world events and culture, empower citizens of all nations, and create social networks that help worldwide communities develop and form bonds based on common interests.

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ISSCC covers a spectrum of design approaches in various technical areas and advances, broadly categorized as analog systems, power management, analog-to-digital data conversion, communication systems, digital systems (including machine learning and AI), and memory. It also covers innovative topics such as microelectromechanical systems, imagers, sensors, and biomedical devices, including forward-looking solutions that may be several years away from becoming commercialized.

The 12 ISSCC technical subcommittees annually update their analysis of industry trends for the benefit of the community at large. This article summarizes some of these views in selected technical areas.

Analog Systems

Subcommittee Chair: Kofi A.A. Makinwa, Delft University of Technology, The Netherlands

At ISSCC 2020, new analog-circuit techniques are enabling improved performance and reduced power for temperature sensors, frequency references, voltage references, and amplifiers. Copackaged bulk-acoustic-wave technology with stability better than ±30 parts per million (ppm) enables crystal-less radio applications. Gallium nitride (GaN) technology provides the ability to realize voltage references that span the very wide temperature range of –50 to 200 °C. Class-D amplifiers achieve the highest total harmonic distortion to date by utilizing delta-sigma techniques.

In the case of integrated temperature sensors, bipolar and resistor-based designs continue to dramatically improve energy efficiency, as revealed by Figure 1. In addition, single-trim, resistor-based temperature sensors' accuracy is approaching that of their bipolar-junction transistor counterparts. Noncrystal oscillators continue to improve in power efficiency while achieving accuracies below ±500 ppm, as indicated in Figure 2.

Power Management

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, California

Power and energy management is important for a number of applications spanning embedded and performance computing, communications systems, consumer devices, automotive/industrial sensing, and control. Over the past decade, new topologies, semiconductor technologies, and control paradigms have driven fundamental changes at the architecture and system levels. Hybrid and resonant switched-capacitor topologies, which promise better utilization of active semiconductors and passive components, are beginning to mature and spread into diverse applications (from LEDs and display drivers to high-conversion load-power delivery). At lower voltages, hybrid approaches are pushing toward higher integration with all passive components integrated on chip.

The need for higher-voltage power conversion is also growing, with more designs targeting the 48–400-V line, power delivery, and cross-domain isolation interfaces. GaN semiconductor technologies are improving in their integration levels and functionality,

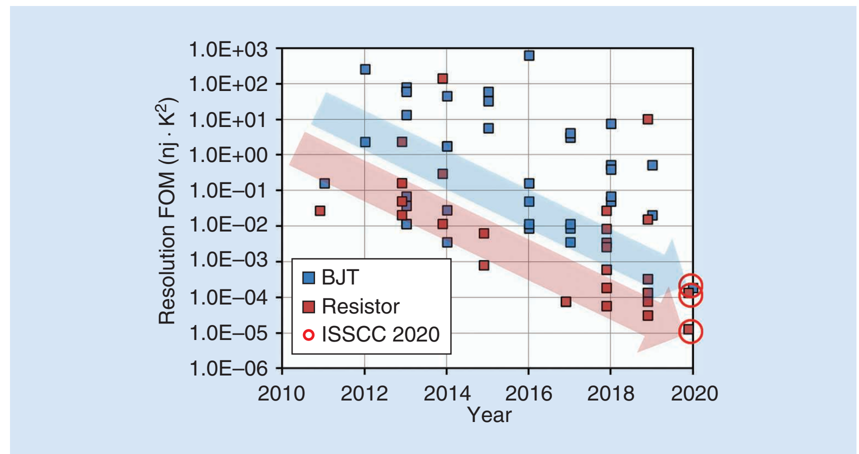

FIGURE 1: Trends in the energy efficiency of integrated temperature sensors: the resolution figure of merit (FOM) versus time. BJT: bipolar-junction transistor.

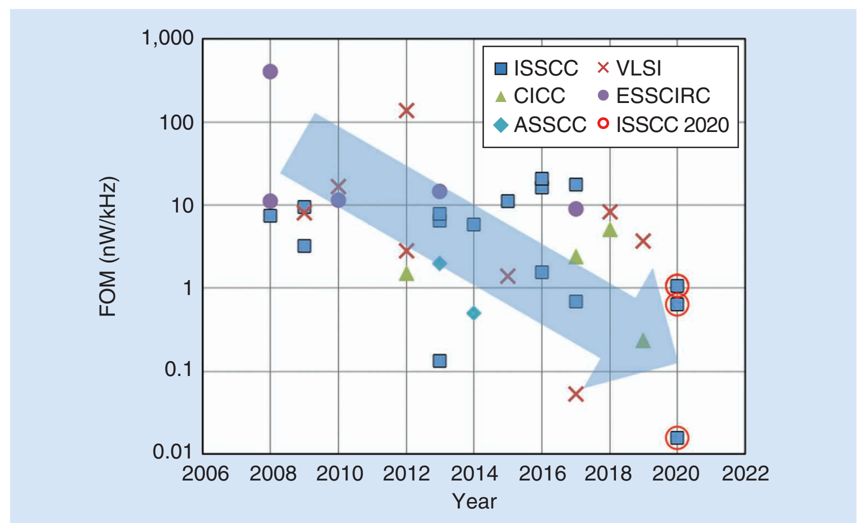

FIGURE 2: Trends in the power efficiency of noncrystal oscillators versus time. CICC: IEEE Custom Integrated Circuits Conference; ASSCC: IEEE Asian Solid-State Circuits Conference; VLSI: Symposia on VLSI Technology and Circuits (VLSI: very-large-scale integration); ESSCIRC: European Solid-State Circuits Conference.

Advances in solid-state circuits and systems have brought ever more powerful communication and computational capabilities into mobile form factors.

with power devices, gate drivers, instrumentation, and interface circuitry starting to share the same die. In addition to high-voltage isolated power delivery, data transmission across galvanic isolation boundaries is increasingly important in many applications. Energy harvesting continues to mature for a variety of piezoelectric, electromagnetic, and optical transducer systems.

Perhaps the most important observable trends in power-management ICs pertain to the diversification of applications, voltage, and power ranges. The following trends are observed at ISSCC 2020:

- As GaN gains greater capability for high-level integration, a variety of circuit techniques is emerging that can improve the electromagnetic interference, efficiency, and reliability of high-voltage, high-frequency switching power converters. These circuit techniques resemble “old school” NMOS-only techniques of many decades ago yet add new and important capabilities.
- Hybrid and resonant switched-capacitor converter techniques are increasingly leveraged in a wide range of topologies to reduce the voltage stress on switches, shrink passive component size, and enable a higher switching frequency.
- The number and diversity of high-voltage IC designs are increasing to deal with challenges related to the grid interface, signal and power isolation, and powering embedded and sensor interface systems from high dc-voltage domains.

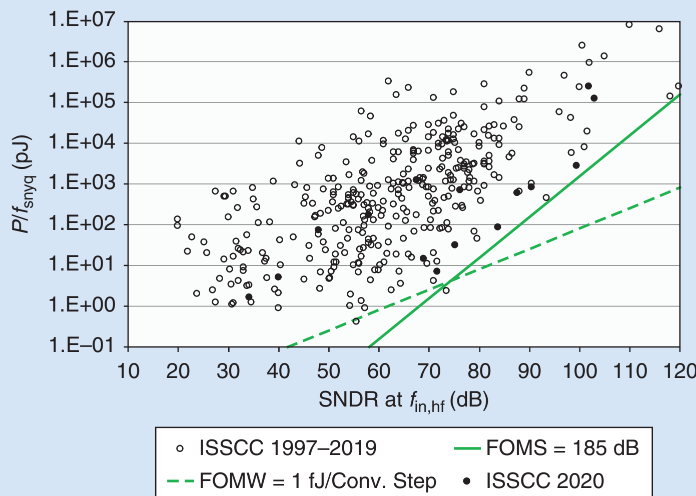

FIGURE 3: ADC power efficiency (P/f_{snyq}) as a function of the SNDR. Conv.: conversion; FOMW: FOM-Walden; FOMS: FOM-Schreier.

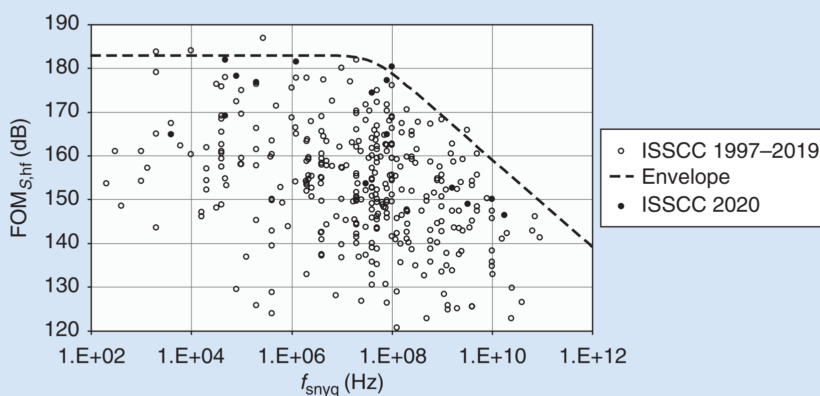

FIGURE 4: Power-normalized noise and distortion versus the Nyquist sampling rate.

Data Converters

Subcommittee Chair: Michael Flynn, University of Michigan, Ann Arbor

Data converters are a critical link between the analog physical world and the digital computing and signal processing prevalent in modern electronics. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver more bandwidth and linearity while continuing to increase power efficiency. ISSCC 2020 continues the trend of highly energy-efficient analog-to-digital converters (ADCs) with a combination of successive-approximation-register (SAR), noise-shaping SAR, and delta-sigma-based designs. Time-interleaved pipeline architectures are pushing the speed limits of converter design.

Figures 3–5 represent traditional metrics that capture the innovative progress in ADC design. Figure 3 plots the power dissipated relative to the Nyquist sampling rate (P/f_{snyq}) as a function of the signal-to-noise and distortion ratio (SNDR) to give a measure of ADC power efficiency. Note that a lower P/f_{snyq} metric represents a more efficient circuit on this chart. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus, the overall

efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend line represents a benchmark of the 1fJ/conversion-step. Circuit noise becomes more significant with higher-resolution converters, necessitating a different benchmark proportional to the square of the signal-to-noise ratio, represented by the solid line. Designs published from 1997 to 2019 are shown in circles. ISSCC 2020 designs are shown in black dots, which continue moving toward the lower right of the figure.

Figure 4 shows the signal fidelity versus the Nyquist sampling rate normalized to power consumption. At low sampling rates, converters tend to be limited by thermal noise, independent of the sample rate. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner, indicated by the roll-off versus frequency in the dashed line. The past 10 years have resulted in an improvement of more than 10 dB in power-normalized signal fidelity, i.e., a 10× improvement in speed for the same normalized signal fidelity. Of note at this year's ISSCC is that two designs are pushing toward thermal-noise-limited efficiency, using delta-sigma and noise-shaped SAR architectures. A pipelined SAR architecture delivers record-setting performance in the speed-versus-efficiency corner of the graph.

Figure 5 illustrates the ADC bandwidth as a function of the SNDR. Sampling jitter and aperture errors coupled with an increased noise bandwidth make achieving high resolution and bandwidth a particularly difficult task. While a state-of-the-art data converter showed an aperture error of approximately 1ps_{rms} 10 years ago, designs with aperture errors below 100fs_{rms} have been published in recent years. ISSCC 2020 further advances the state of the art with an extremely high-performing, time-interleaved pipeline architecture that surpasses the 100-fs_{rms} aperture line.

New analog-circuit techniques are enabling improved performance and reduced power for temperature sensors, frequency references, voltage references, and amplifiers.

Communication Systems: Radio-Frequency Subcommittee

Subcommittee Chair: Piet Wambacq, IMEC, Leuven, Belgium

ISSCC 2020 features terahertz imaging demonstrators, CMOS power amplifiers (PAs), and phase-locked-loop (PLL) prototypes. Applications driving advances in the field of radio-frequency (RF) ICs in silicon technologies include 1) broadband and 5G communications using massive multiple input/multiple output (MIMO) and millimeter-wave (mm-wave) technologies, 2) the Internet of Things (IoT), and 3) sensing and imaging at sub-mm-wave frequencies.

PLL Synthesizers

Visible highlights are PLLs generating mm-wave frequency carriers directly or via on-chip multipliers; synthesizers offering lower integrated jitter and power consumption (for example, a –250-dB jitter-power FOM); and wideband, frequency-modulated, continuous-wave radar-chirp generation. Overall, subsampling PLLs continue to trend lower in power consumption and integrated timing jitter, with all-digital PLLs continuing to displace traditional analog designs. Fractional-N bang–bang, all-digital, and hybrid fractional-N/integer synthesizers are also demonstrating continuing innovations in more traditional PLL designs.

The trend in the FOM for PLLs, which depends on integrated jitter (jitter variance) and power consumption, is illustrated in Figure 6. ISSCC 2020 presents two fractional-N PLLs with outstanding timing-jitter performance:

1) a 12.8–15.2-GHz digital bang–bang PLL that realizes 66-fs_{rms} jitter and performs a 1-GHz hop to within 0.1% of the steady-state frequency in 18.55 μs
2) a 12.5-GHz fractional-N sampling PLL in 28-nm CMOS that incorporates a digital background phase-error correction to enable 58-fs integrated jitter (fractional mode) and 51 fs (operating in integer mode).

The overall FOM for these PLLs is consistent with previous designs, as seen in

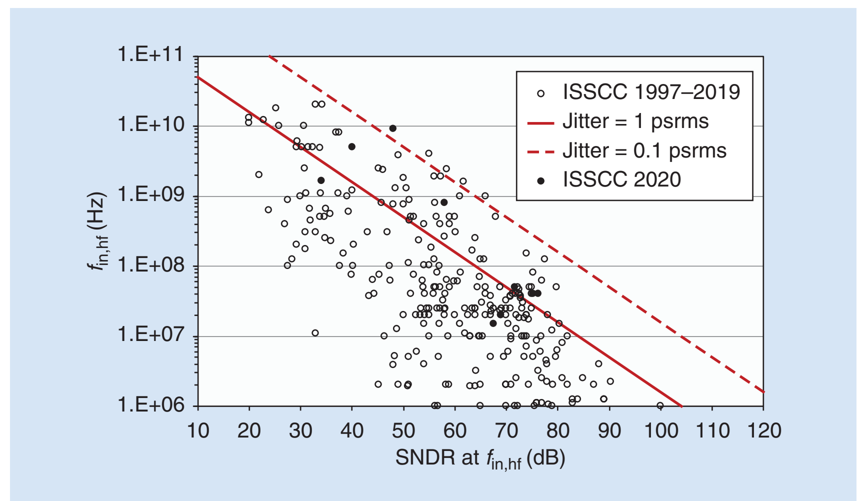

FIGURE 5: The bandwidth versus the SNDR. psrms: picoseconds/root mean square.

FIGURE 6: Oscillator trends for (a) subsampling PLLS and (b) frequency synthesizers above 20 GHz. *JSSC*: *IEEE Journal of Solid-State Circuits*.

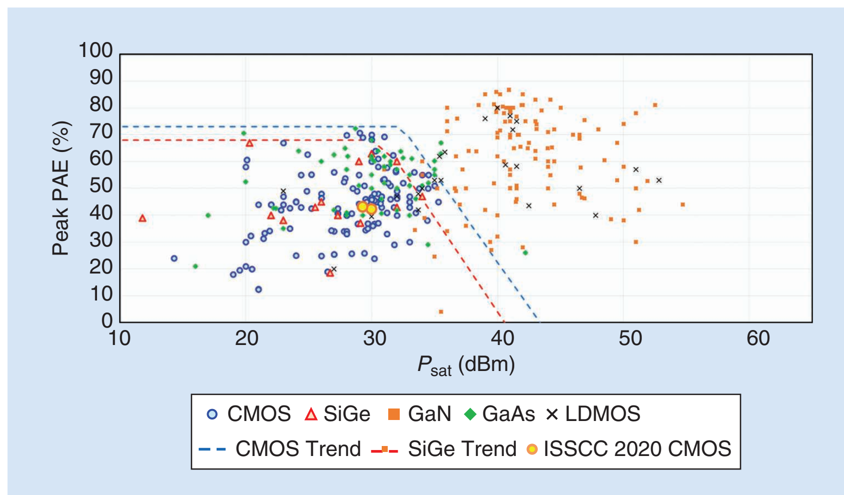

FIGURE 7: The under-6-GHz PA trend. SiGe: silicon germanium; GaAs: gallium arsenide; LDMOS: laterally diffused metal-oxide semiconductor.

the figure. Advanced voltage-controlled oscillator and mm-wave output frequency-generation circuit designs operating with greater stability at a lower power consumption redefine the state of the art in CMOS designs and ensure that advances in frequency synthesis will continue for the foreseeable future.

RF and mm-Wave PAs

Doherty-type PAs integrated in CMOS are demonstrating an improved power-added efficiency (PAE) at the higher peak-to-average power ratios demanded by advanced modulation formats, such as 5G New Radio (NR). A 24–30-GHz watt-level Doherty PA fully integrated in 45-nm silicon-on-insulator CMOS employs a multiprimary distributed active-transformer power combiner and is capable of supporting 5G NR transmissions. Multiway power combing and active load modulation are achieved simultaneously. A digital polar PA prototype operating in class-G mode also functions above 1 W but in the 2.4-GHz industry, science, and medicine band (Figure 7). Remarkably, when the output power is reduced by 18 dB, this PA can still provide drain efficiencies approaching 50% of peak performance. The signal quality under 1,024 quadrature amplitude modulation (QAM) is excellent at a −44.5-dB error vector magnitude for a 23.2-dBm RF power output (Figure 8). ISSCC 2020 will also

feature the first d-band PA in 16-nm CMOS [fin field-effect transistor (FinFET)]. It demonstrates a peak gain of 25.6 dB, saturated output power of 15 dBm, and peak PAE of 11.7%. The active chip area for this 135-GHz PA is just 0.062 mm^2 (Figure 9).

Emerging Technologies for Communication and Terahertz Sensing/Imaging

At ISSCC 2020, terahertz (THz)-frequency imaging and sensing chips—demonstrating higher levels of complexity and power outputs than ever before—and radio front-end circuits enabling full duplex communication are important developments. Computational THz imaging debuts at ISSCC 2020 with an 8×8-pixel source-array system-on-chip (SOC) with an on-chip, built-in self-test that radiates up to 9.2 dBm at 0.42 THz and can support imaging at up to 30,000 frames per second. The highest radiated power for silicon-based sources above 0.35 THz is produced by a beam-steerable array implemented in 40-nm CMOS. It combines 36 coherent radiators producing 24.1 dBm of equivalent isotropically radiated power and a beam-steering range of 30° at a frequency of 0.59 THz.

Future low-latency radio-access networks demand clocks with 0.1 parts per billion (ppb) stability. A 70-mW chip-scale molecular clock probing the 231.06-GHz transition of carbonyl sulfide demonstrates a stability of ±3 ppb with changing temperature. Finally, a sub-THz backscattering wireless tag operating at 260 GHz has a 5-cm range for bidirectional communication via an on-chip antenna array capable of beam steering across 30°.

Communication Systems: Wireless

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, Oregon

The continuing demand for faster wireless-data rates in the context of mobile-battery limitations drives the development of high-throughput and power-efficient transceivers. At ISSCC 2020, Wi-Fi and cellular standards continue to evolve with 5G NR and Wi-Fi 6 (IEEE Standard 802.11ax) to deliver ever increasing data throughput using dense 1,024-QAM modulation, a wide bandwidth of up to 200 MHz, and multiple parallel data streams employing uplink and downlink MIMO. Furthermore, carrier aggregation and concurrent operation enable cellular and Wi-Fi radios to obtain larger spectrum resources when a single contiguous frequency range is not available.

Figure 10 shows the trend in the number of downlinks for recent cellular SOC implementations as well as the shift in process nodes. It indicates an increasing interest in carrier aggregation to support higher data rates. This year, an advanced cellular transceiver features 10 downlinks in 12-nm FinFET CMOS. The transceiver extends carrier aggregation to support up to six interband 3G, 4G, and 5G carriers while also enabling NR and LTE protocols with dual connectivity (evolved universal terrestrial radio access NR dual connectivity).

Operation at the low supply voltages available from energy harvesting and small form factors are vitally important for IoT and insertable medical devices. A low-voltage Bluetooth low-energy transceiver capable of operating through energy harvesting is being introduced at ISSCC 2020;

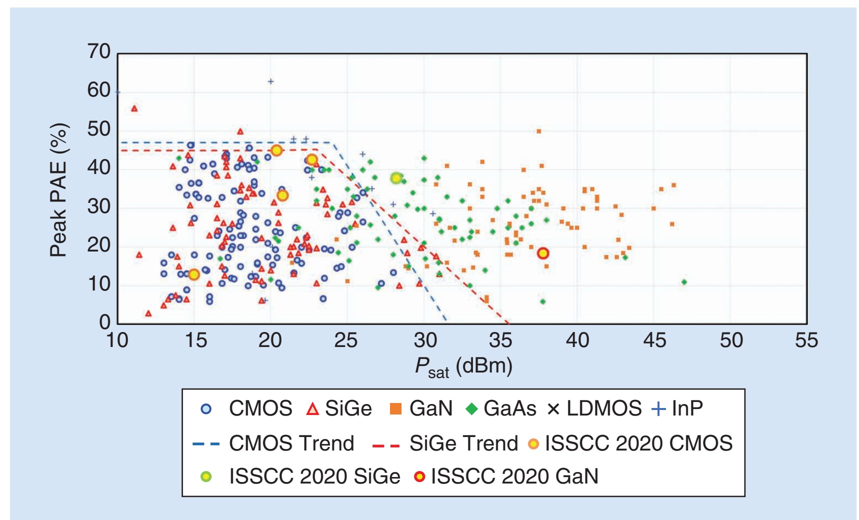

FIGURE 8: The over-20-GHz PA trend. InP: indium phosphide.

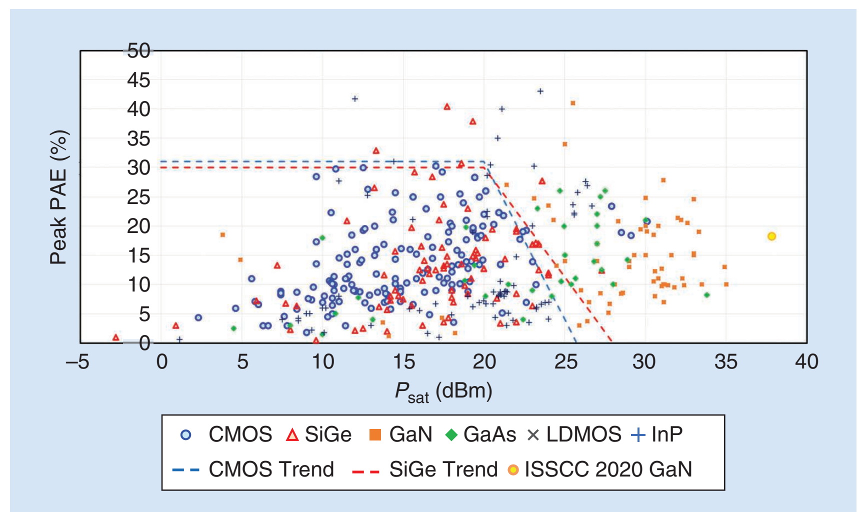

FIGURE 9: The over-50-GHz PA trend.

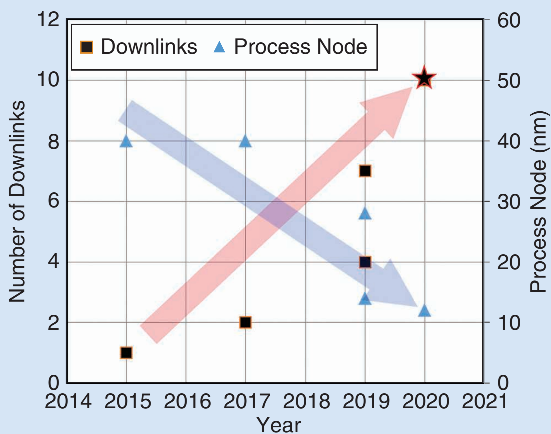

FIGURE 10: Trends in the number of downlinks and process nodes for recent cellular SOC implementations.

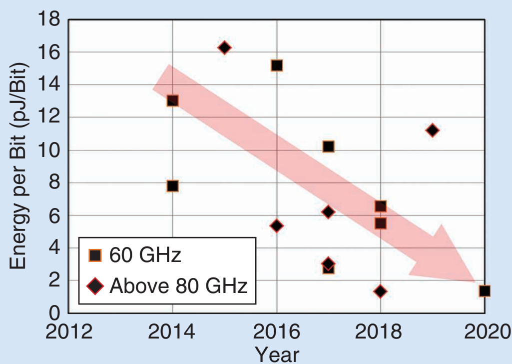

FIGURE 11: The receiver power-efficiency trend.

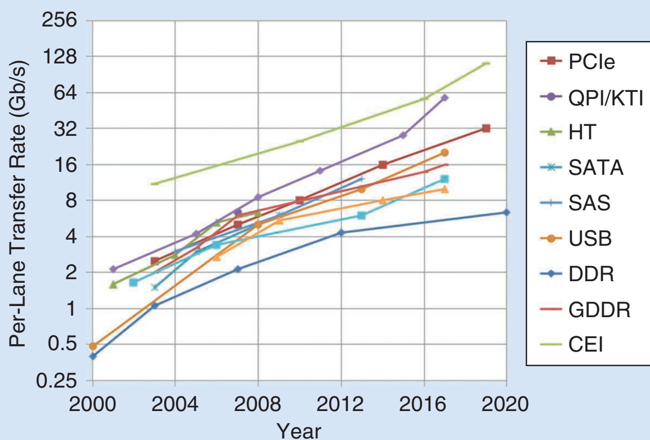

FIGURE 12: The per-pin data rate versus year for a variety of common I/O standards. PCIe: peripheral component interconnect express; QPI/KTI: QuickPath Interconnect/Keizer Technology Interconnect; HT: HyperTransport; SATA: serial advanced technology attachment; SAS: serial attached small computer system interface; GDDR: graphics DDR; CEI: comparably efficient interconnection.

it has a –96.4-dBm sensitivity and 4.1-dB adjacent-channel rejection while dissipating 1.9 mW. Furthermore, a small-form-factor, crystal-less medical implant communication system transceiver for insertable smart pills is being presented with a 3.5- × 3.8-mm footprint.

Figure 11 displays the trend in energy efficiency for 60-GHz and beyond-80-GHz receivers. A receiver being presented at ISSCC 2020 leverages dual-polarization and circuit techniques to demonstrate a <2 pJ/b efficiency while achieving throughputs of >50 Gb/s at mm-wave frequencies, reaching a 64-Gb/s data rate. This is the first 60-GHz phased-array receiver with >50 Gb/s throughput. The growing demands on high-data-rate transceivers are reflected in cellular communications, with the development of mm-wave systems for 5G NR in the 28- and 39-GHz bands.

Communication Systems: Wireline

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, Oregon

Over the past few decades, electrical and optical interconnects have been key components bridging the gap between the exponentially growing demands for data bandwidth across electronic components/systems and the relatively gradual increase in pin/cable density. Ranging from handheld electronics to supercomputers, wireline data-communication bandwidth must grow exponentially to avoid limiting the performance scaling of these systems. By increasing the data per pin or cable of various electronic devices and systems, such as memory, graphics, the chip-to-chip fabric, the backplane, rack-to-rack, and local area networks (LANs), wireline input–output (I/O) has fueled incredible technological innovation in electronic devices and systems. Figure 12 shows that the data rate per pin has approximately doubled every four years across I/O standards ranging from double data rate (DDR) to graphics and the high-speed Ethernet. Figure 13 demonstrates that the data

rates for published transceivers have kept pace with these standards while taking advantage of CMOS scaling. Figure 14 depicts the published transceiver energy efficiency versus channel losses at the Nyquist frequency in the 40–50-dB range.

In part, this incredible improvement is enabled by the power-performance benefits of process technology scaling. However, sustaining this exponential trend for I/O bandwidth scaling requires more than just transistor scaling. Significant advances in energy efficiency, channel equalization, and clocking must be made to enable the next generation of low-power, high-performance computing systems. ISSCC 2020 includes examples of short-reach electrical interconnects operating at up to 25 Gb/s, long-reach copper interconnect transceivers operating at up to 112 Gb/s, and optical transceivers and components operating at up to 112 Gb/s (direct modulation) and 640 Gb/s (coherent). New techniques for noise and power reduction, channel equalization, and clock recovery are reported. These transceivers and transceiver building blocks are implemented in CMOS and bipolar CMOS (BiCMOS) technologies.

Scaling Electrical Interconnects to 100 Gb/s

Bandwidth requirements in data centers and telecommunication infrastructure continue to drive the demand for ultrahigh-speed wireline communication. During the past few years, complete transceivers operating at up to 56 Gb/s were demonstrated across a variety of channel lengths. Two notable trends in these transceivers, especially for long-reach channels, are the adoption of pulse amplitude modulation (PAM)-4 and a transition to digital-to-analog converter (DAC)/ADC architectures with digital signal processor (DSP)-based equalization. Although PAM-4 provides twice the data rate at the same baud rate as conventional nonreturn to zero (NRZ) and thereby relaxes channel loss requirements for bandwidth doubling, it also comes with more stringent requirements for linearity, noise, and multilevel signaling.

This trend motivated the development of low-power data converters, digital equalization, and clock recovery as well as linear high-bandwidth transceiver and receiver analog front ends. During the past two years, the first such components were demonstrated to extend these transceivers to 112 Gb/s. At ISSCC 2020, a 56-Gb/s DAC/ADC-based transceiver, a 100-GBd DAC-based transmitter, and the first descriptions of complete 112-Gb/s PAM-4 long-reach transceivers in 7-nm CMOS will be presented. Xilinx will describe a 112-Gb/s PAM-4 transceiver for long-reach copper interconnects employing a 36-way, time-interleaved, 56-gigasamples/s, 7-b ADC. MediaTek will present a complete four-lane, 112-Gb/s DAC/ADC-based transceiver. Both transceivers exhibit flexible equalization capability and consume <5 pJ/b (not including the DSP power).

Silicon Photonic Bandwidth Scaling and Integration

The explosive growth of data and data-centric computing places stringent demands on the bandwidth and energy efficiency of data-center interconnects, spurring the development of several 200–400-Gb Ethernet standards. Within the rack, much of the interconnect bandwidth is provided by electrical links over copper interconnects, and optical interconnects are increasingly used to bridge longer distances. Silicon-photonics-based solutions are of particular interest for low-cost 50+-Gb/s/λ optical transceivers. Furthermore, multilevel modulation schemes, such as PAM-4,

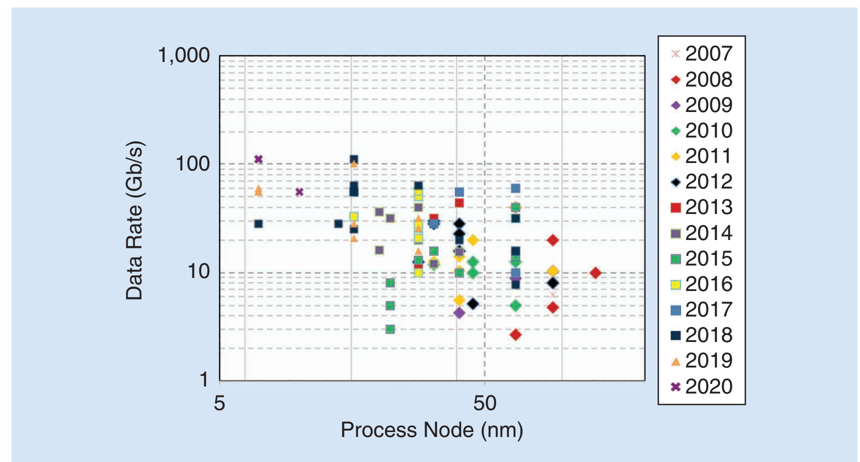

FIGURE 13: Data rate versus process node and year.

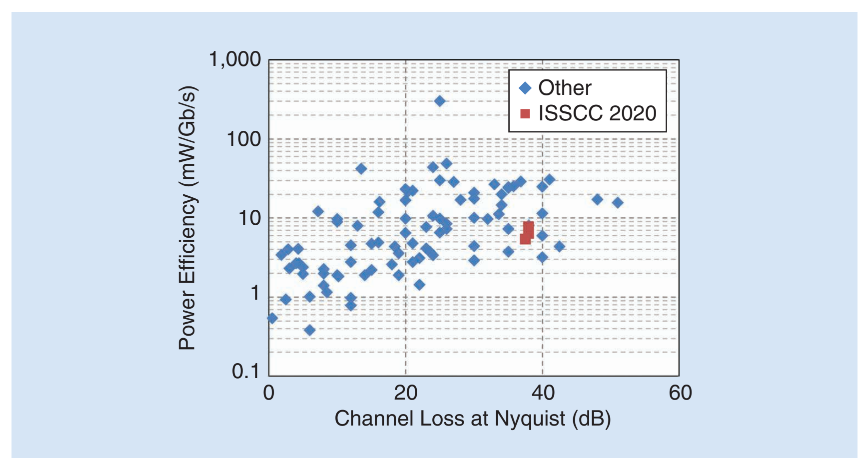

FIGURE 14: Transceiver power efficiency versus channel loss.

improve the tradeoff between circuit bandwidth, power consumption, data rate, and optical-link range compared with NRZ optical signaling. Since many such modules are packed side-by-side in networking and computing infrastructure, low power consumption is required to prevent the equipment from overheating. The highly integrated silicon-photonic approaches presented at ISSCC 2020 will address this need by communicating at 50–100 Gb/s across each fiber using PAM-4 modulation with low-power consumption, reducing the need for expensive cooling and pushing classical discrete implementation toward obsolescence.

Intel will describe a PAM-4 microring-based optical transmitter using a 3D-integrated silicon-photonic and CMOS circuit assembly with a robust 112-Gb/s operation. The thermal variability and nonlinearities that usually plague such modulators are addressed with nonlinear equalization and closed-loop thermal control. STMicroelectronics will demonstrate a transceiver for the IEEE P802.3bs 200GBASE-DR4 standard. The four-channel electro-optical transceiver provides an aggregate bandwidth of 200 Gb/s using a 55-nm BiCMOS technology that is 3D-assembled onto a silicon-photonic front-end IC through copper pillars. Data-rate scaling of coherent optics for longer-reach optical interconnects is also being highlighted at ISSCC 2020. NTT will demonstrate a four-channel Mach-Zehnder modulator driver capable of transmitting 640 Gb/s over a single fiber, using dual-polarization 32-QAM modulation while consuming only 1.4 pJ/b.

Continuing to aggressively scale the I/O bandwidth is essential for the industry, but the tradeoffs among bandwidth, power, area, cost, and reliability are extremely challenging. Advances in circuit architecture, interconnect topologies, transistor scaling, and integrated silicon photonics are changing the way that I/O will be done during the next decade. The most exciting and promising of these emerging technologies for electrical and optical interconnects will be highlighted at ISSCC 2020.

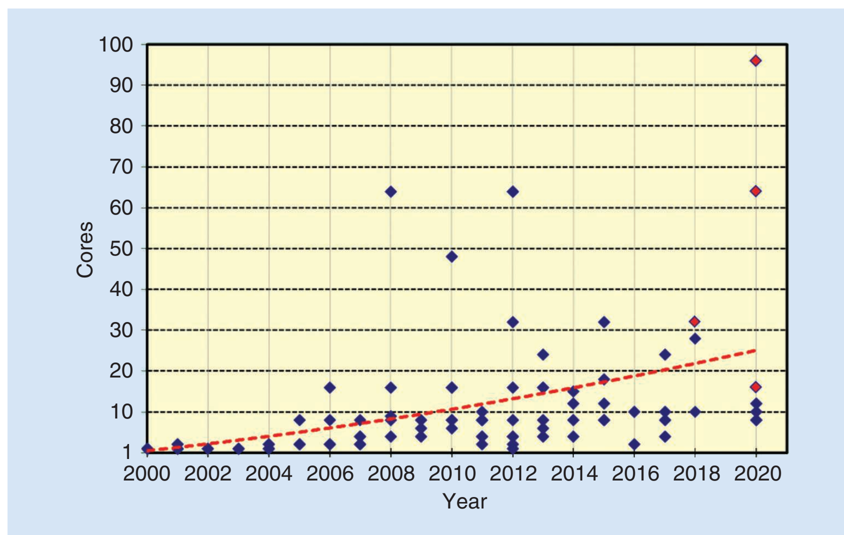

FIGURE 15: Core-count trends (the red diamonds designate a multichip module).

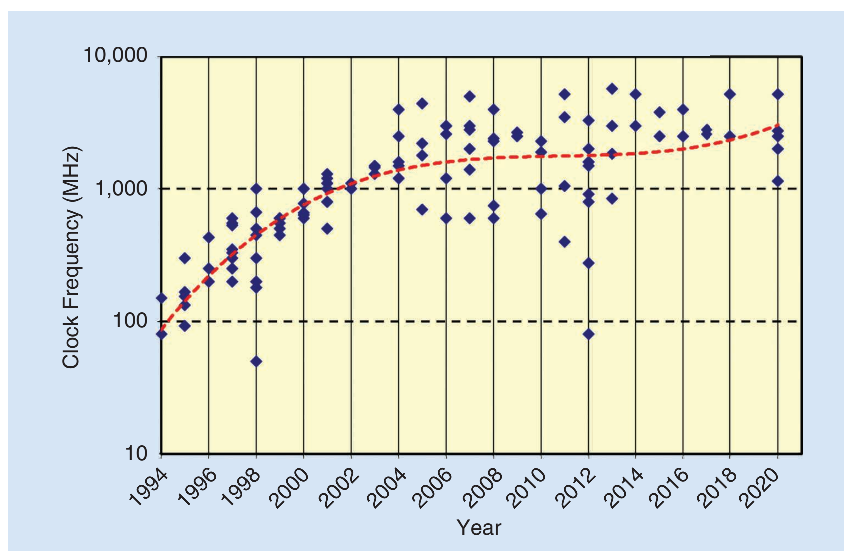

FIGURE 16: Clock-frequency-scaling trends.

Digital Systems: Digital Architectures and Systems

Subcommittee Chair: Thomas Burd, Advanced Micro Devices, Santa Clara, California

ISSCC 2020 features a plethora of flagship industry processors covering servers, desktops, mobile application processors (APs), and automotive processors ranging from 28- to 7-nm CMOS. Additionally, there are invited industry papers on graphics processing units (GPUs) (a first for ISSCC), a field-programmable gate array, an industry full-3D mobile processor, and a next-generation, high-performance ARM core. The trend continues to exploit multichip integration technologies to drive the core count and on-die cache (Figure 15).

The computational performance of mobile AP SOCs historically grew as silicon process technology advanced (Figure 16). AP SOCs continue to gain more features, including 5G modems, multimedia intellectual-property cores (Figure 17), and accelerators on chip to enhance functionality (Figure 18).

Mobile phones are receiving more camera sensors, which drives additional complexity onto SOCs (Figure 19). Dedicated neural-network accelerators execute machine-learning functions faster and with higher energy efficiency than generic CPUs and GPUs. Neural-network processing units (NPUs) will be adopted in most future AP SOCs, establishing an important direction in which an efficient software solution utilizes heterogeneous computing combining CPUs, GPUs, and NPUs. On-device training features continue to be incorporated for private-data security and device personalization.

Wired and wireless links continue to increase in bandwidth, with a trend of 10 times higher data rates every five years (Figure 20). The changes are modest this year at ISSCC 2020 relative to last year. mm-wave and massive MIMO technologies are being actively studied to realize 5G communication. The first 5G mobile device was commercialized in 2019. The explosion of Internet of Everything (IoE) devices will require the evolution of narrow-band, wide-area networks.

Circuits for Hardware Security

With the growing risk and cost of information theft, hardware-implemented security has become a common circuit component. Although the focus on cryptographic implementation continues, cost-effective physically unclonable functions (PUFs) (Figure 21) are now a focus area in, for instance, smart cards, consumer devices, and automotive applications. True random-number generators are also commonly leveraged to strengthen secret-key generation in cryptographic applications.

Digital Systems: Digital Circuits

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, California

The demand for higher performance across ubiquitous, connected, and energy-constrained platforms, ranging from the IoE to cloud data centers, continues to drive innovations in all CMOS digital-circuit building blocks, with the goals of improving energy efficiency and performance, lowering the cost/design effort, and enhancing security. Classic technology scaling has slowed, and circuit-design efforts are exploiting technology features such as body biasing and passive-device advancements to enable circuit innovation. In addition, variation mitigation has become a major trend in digital circuits to improve robustness and power efficiency across process, voltage, and temperature (PVT). Specifically, all-digital sensors and adaptive (clocking) techniques continue to be proposed to mitigate these effects on chip, with the goal of reducing the PVT margins and enabling circuit-driven, chip-level performance gains.

A trend toward application-specific accelerators is leading to the development of new circuit techniques that benefit a range of emerging applications, including navigation in microrobotics, deoxyribonucleic-acid-sequencing engines, and annealing processors for solving large combinatorial problems. Some of these accelerators leverage compute-in-memory (CIM) strategies, while others rely on circuit operation in nonconventional modes/domains, including time-and charge-domain computation.

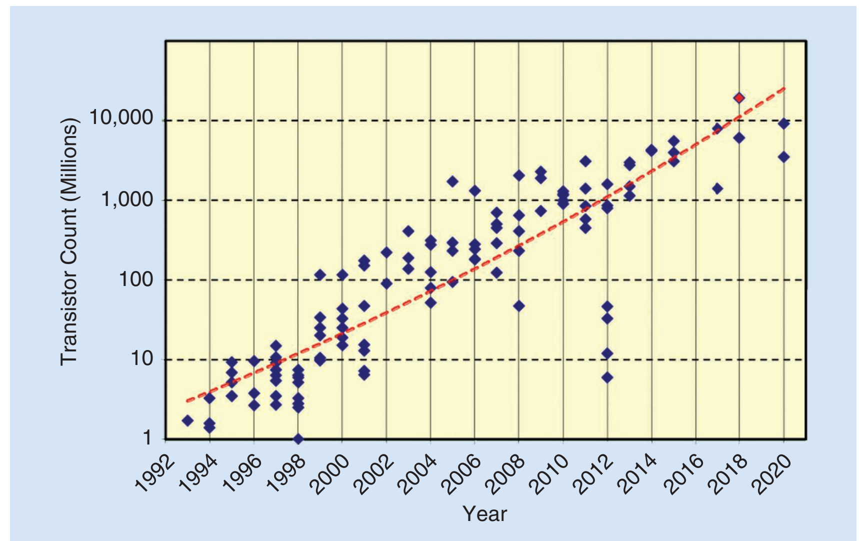

FIGURE 17: Chip-complexity-scaling trends (the red diamond designates a multichip module).

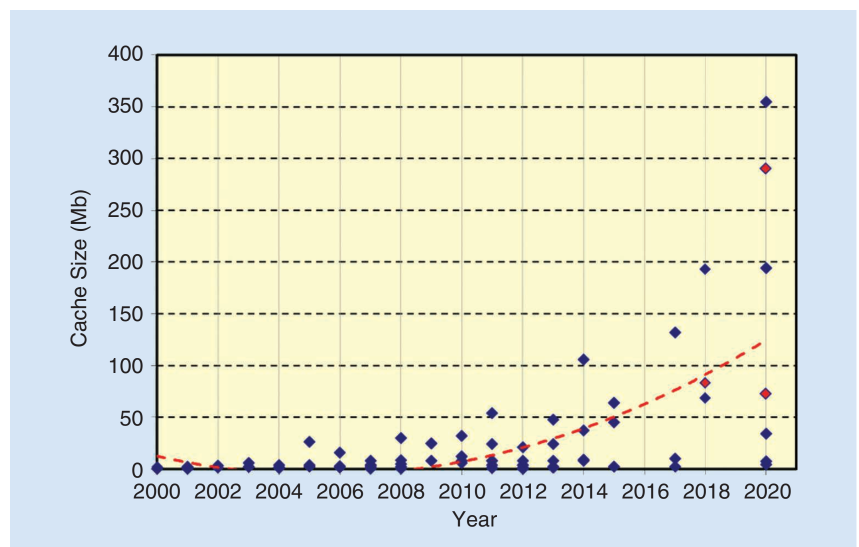

FIGURE 18: On-die cache-size trends (the red diamonds designate a multichip module).

Graphics	OpenGL (ES1.1)	OpenGL/VG/MAX (ES2.0)	AR	VR Vulkan			
Display	VGA	WVGA at 60 f/s	SXGA at 60 f/s	WQXGA/WQXGA+ at 60 f/s	WQXGA/WQXGA+ at 60 f/sx2 (VR)	WQXGA/ WQXGA+at 120 f/s	
Camera	5–8 M	10 M	16 M	20 M	24 M	12 MxDual 360° VR	16 MxDual 3D Depth/AR	80 M Triple
Image/Video	H.264/AVC (VGA)	H.264/AVC (D1)	H.264/AVC (Full HD)	H.264/MVC H.264/SVC	H.265/VP9	H.265/VP9 HDR	AV1 HDR10+
Audio	AAC	AAC Plus	WMA Dolby 5.1	Dolby TrueHD/Digital+	DSD Dolby Atmos	TWS Truly Wireless	
Accelerator	FPU	SMID Multicore (2–4)	Multicore (4–8)	Heterogeneous Multiprocessing	Neural-Net Processor	5 TOPS	
Downlink (Mb/s)	UMTS 0.4–2	HSPA 1.8–7	HSPA+ 7–42	LTE 100	LTE-A 150–750	LTE-A 1,600	LTE-A 2,000	5G 5,000
CPU (MI/s)	300 500	500 800	800 2,400	2,400 6,000	6,000 12,000	12,000 100,000	13,000 112,000	19,000 162,000	22,000 180,000

2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020

FIGURE 19: AP trends in smartphones. OpenGL: Open Graphics Library; VG: vector graphics; MAX: media acceleration; AR: augmented reality; VR: virtual reality; VGA: video graphics array; WVGA: wide VGA; SXGA: super extended GA; WQXGA: wide quad-extended GA; fps: frames per second; AVC: advanced video coding; HD: high definition; MVC: multiview video coding; SVC: scalable video coding; HDR: high dynamic range; AV1: Alliance for Open Media Video 1; AAC: advanced audio coding; WMA: Windows Media Audio; DSD: direct-stream digital; TWS: true wireless stereo; FPU: floating-point unit; SIMD: single instruction, multiple data; TOPS: tera operations; UMTS: universal mobile telecommunications service; HSPA: high-speed packet access; MI/s: million instructions per second; M: megapixel.

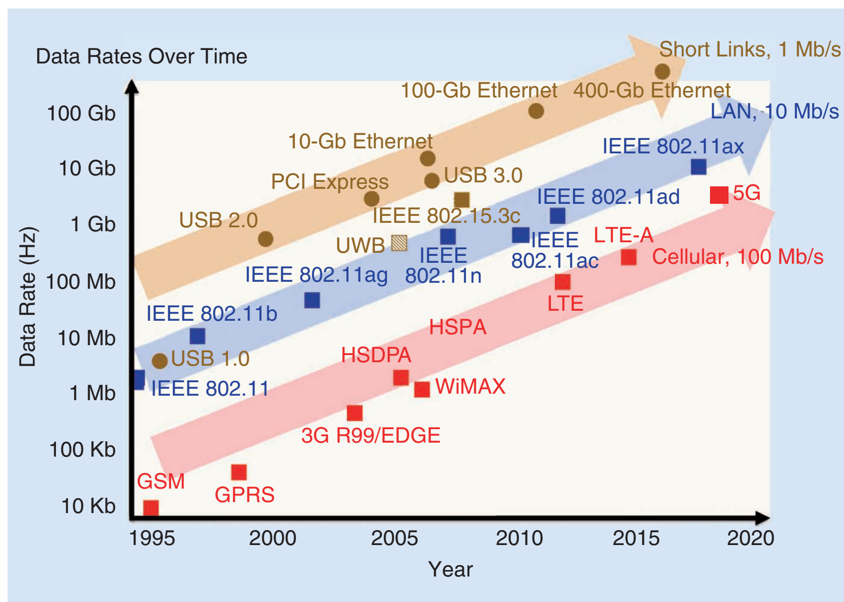

FIGURE 20: Data-rate trends in wired, wireless, and cellular communication. UWB: ultrawideband; GSM: Global System for Mobile Communications; GPRS: general packet radio service; HSDPA: high-speed-downlink packet access; WiMAX: Worldwide Interoperability for Microwave Access.

Integrated Voltage Regulators

At ISSCC 2020, energy reduction remains a top priority as power density continues to increase. Voltage regulators, while traditionally being off chip, have increasingly been integrated on chip to reduce cost. Low-dropout (LDO) linear regulators, switched-capacitor voltage regulators (SCVRs), and even inductor-based buck-voltage regulators (LCVRs) are integrated in scaled process nodes to enable faster and fine-grain dynamic voltage and frequency scaling (DVFS) of individual functional blocks. In turn, the low voltages supported in DVFS systems necessitate a move from analog-based LDOs to digital implementations.

There is a recent movement toward making these digital LDOs synthesizable, reducing the design effort and easing portability. Another trend is toward hybrid LDOs that incorporate the best features of analog and digital designs. Figure 22 shows the conversion efficiency and current density of these integrated voltage regulators, which continue to improve.

Synthesizable Digital PLLs for Low-Jitter Applications

PLL trends include the migration from analog to digital to include more functionality, cope with variability, and ease scaling to finer geometries. Demand for compact, low-jitter PLLs is increasing. The use of more automated digital design flows (such as synthesis and automated placement and routing) dramatically reduces development costs but can degrade the jitter, requiring new compensating techniques. Figure 23 highlights the metrics for PLLs and digital PLLs (DPLLs) published at ISSCC over roughly the past 10 years. The plot shows the relationship between the reference (input) frequency and FOM, demonstrating the tradeoff between cost (a higher reference frequency) and overall PLL performance.

Machine Learning and AI

Subcommittee Chair: Marian Verhelst, KU Leuven, Heverlee, Belgium

Owing to the worldwide trend of deep-learning enthusiasm in recent years, ISSCC 2020 has established a dedicated subcommittee on machine learning and AI. As deep neural networks succeed in achieving better accuracy in a wide variety of tasks, their computational complexity rises. For data center, mobile, and IoT workloads, this results in continuous demand for more energy-efficient and higher-throughput neural-network computing. This year's submissions have targeted those objectives across a broad power spectrum, ranging from 0.5-μW always-on accelerators to 276-W data center AI processors.

It is important to note that the metrics that matter at the system level are energy/inference and inference/s for a specific task and a given inference accuracy. This year's submissions again significantly push the state of the art of these efficiency and throughput numbers by combining multiple enhancement techniques in tandem within a single chip, implemented in the most advanced technology (Figure 24):

1) Support for different levels of computational precision is now almost omnipresent to efficiently allow multiple tasks. In addition to fixed-point accuracies between 2 and 8 b, some architectures support floating-point (FP)8 and FP16 for training as well as pixel-manipulation workloads.
2) It is clear that the exploitation of sparsity has become a common theme; it boosts throughput between two and four times and energy efficiency up to an order of magnitude. In fact, more than 50% of the techniques at ISSCC 2020 specifically leverage input, output, and/or weight sparsity as one of their key innovations. We further see an increase in the number of approaches concerned with multibit, in-memory computing, gradually perfecting resolution and accuracy as well as energy efficiency. A particular challenge in this context is to combine the exploitation of sparsity with in-memory computing, a topic that will also be addressed.
3) At ISSCC 2020, it can be noted, in general, that machine-learning processors are increasingly realized in the most advanced technology, with chips exploiting 7 and 12 nm.

As different chipsets are often characterized on a different set of tasks, network topologies, and accuracy levels, comparing the true system-level benchmarking metrics, such as energy/inference and inference/s, is not always straightforward. It is, therefore, interesting to look at the achieved low-level metrics of operations/s and energy/operation within the neural network,

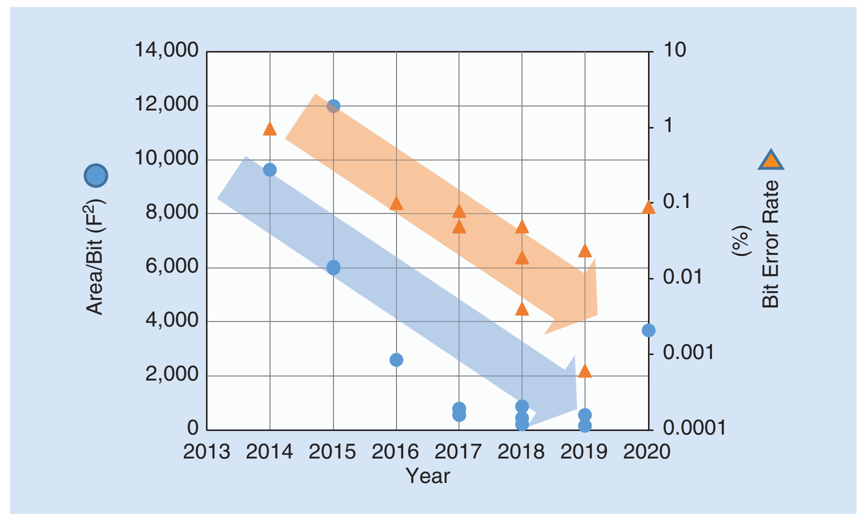

FIGURE 21: Area/bit and bit-error-rate trends for the PUFs published recently at ISSCC. F²: feature squared.

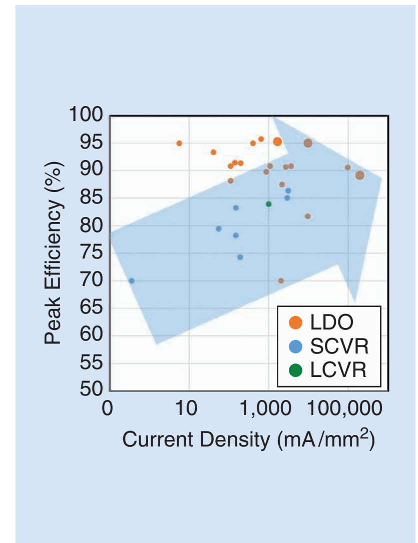

FIGURE 22: The integrated voltage regulators (large LDO symbols represent 2020 papers).

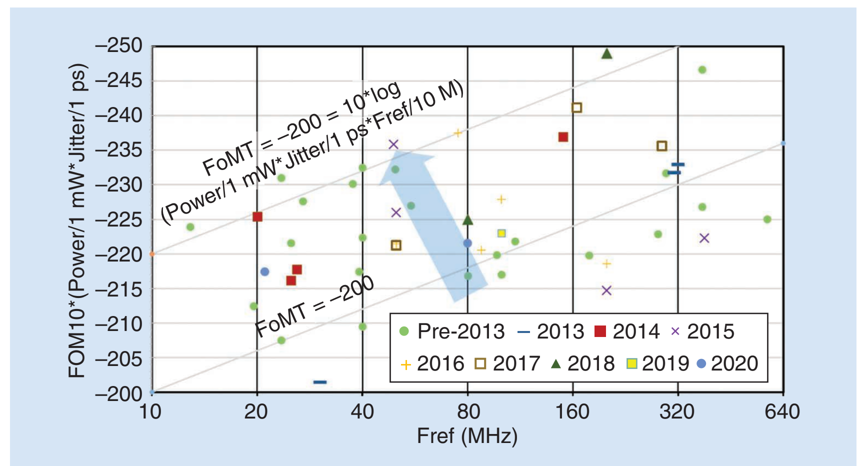

FIGURE 23: PLL and multiplying-delay-locked-loop trends. FoMT: FOM with tuning.

Continuing to aggressively scale the I/O bandwidth is essential for the industry, but the tradeoffs among bandwidth, power, area, cost, and reliability are extremely challenging.

as illustrated in Figure 25 for new datapoints from ISSCC 2020 compared to the state of the art in 2018 and 2019. Yet one should be well aware that these tera operations (TOPS)/W and TOPS/s are strongly dependent on the exercised neural-network topologies, computational precision, and network sparsity. Going forward, as the field matures, we believe that a common benchmarking methodology must be established, accounting for the application context. But, without any doubt, the clever combination of sparsity, variable precision, and in-memory computing technologies enables continued enhancement of deep-learning processor efficiency and throughput.

Memory

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

The demand for high-density, high-bandwidth, and low-energy memory systems continues to grow everywhere, from high-performance computing to SOCs, wearables, and the IoT. ISSCC 2020 presents the first 5-nm FinFET static random-access memory (SRAM). CIM boosts the performance and energy efficiency of multiplication-and-accumulation (MAC) operations in 7-nm SRAM as well as in a leading-edge, 22-nm resistive RAM (ReRAM). In dynamic RAM (DRAM), the performance of high-bandwidth memory evolution (HBM2E) is extended to 640 GB/cube and 8.5 Gb/s for low-power double data rate 5 (LPDDR5) components. For NAND, the lowest latency is reported as well as a quad-level cell NAND with the highest program bandwidth ever publicized. For span-transfer-torque magnetic RAM (STT-MRAM), the highest read bandwidth ever is shown as well as the first near-memory STT-MRAM. The growing number of papers on high-speed memory interfaces emphasizes the trend to push memory bandwidth limits further.

Papers of note at ISSCC 2020 include the following:

- A 5-nm, 135-Mb SRAM in extreme ultraviolet lithography (EUV) and high-mobility-channel FinFET technology, with metal coupling and charge-sharing, write-assist circuitry schemes for high-density and low-V_{MIN} applications
- A 351-TOPS/W and 372.4-GOPS CIM SRAM macro in 7-nm FinFET CMOS for machine-learning applications
- A 1.1-V, 16-GB, 640-GB/s HBM2E DRAM with a data-bus-extension technique and a synergetic on-die scheme
- An 8.5-Gb/s/pin, 12-Gb LPDDR5 synchronous DRAM with a hybrid bank architecture, skew-tolerant and low-power schemes, and speed-boosting techniques
- A 128-Gb, 1-b/cell, 96-word-line-layer 3D flash memory to improve random-read latency with $t_{PROG} = 75\ \mu s$ and $t_R = 4\ \mu s$
- A 32-Gb/s, digital-intensive, single-ended PAM-4 transceiver for high-speed memory interfaces with a two-tap, time-based decision-feedback equalizer
- An 8-nm, 18-Gb/s/pin graphics double-data-rate type-six synchronous dynamic random-access memory (GDDR6) PHY with a transceiver-bandwidth extension and receiver-training technique
- A 22-nm, 2-Mb ReRAM CIM macro with 121–128 TOPS/W for multibit MAC computing for tiny AI edge devices
- A 22-nm, 1-Mb, 1,024-b read and near-memory-computing, dual-mode STT-MRAM macro with a 42.6-GB/s read bandwidth for security-aware mobile devices.

SRAM

Scaling in SRAM continues, and the first 5-nm FinFET EUV SRAM is being presented. Innovations in SRAM support high densities, CIM, high energy efficiencies, and applications with very low latency requirements. Shifting computation inside the memory array (CIM) is a leading approach

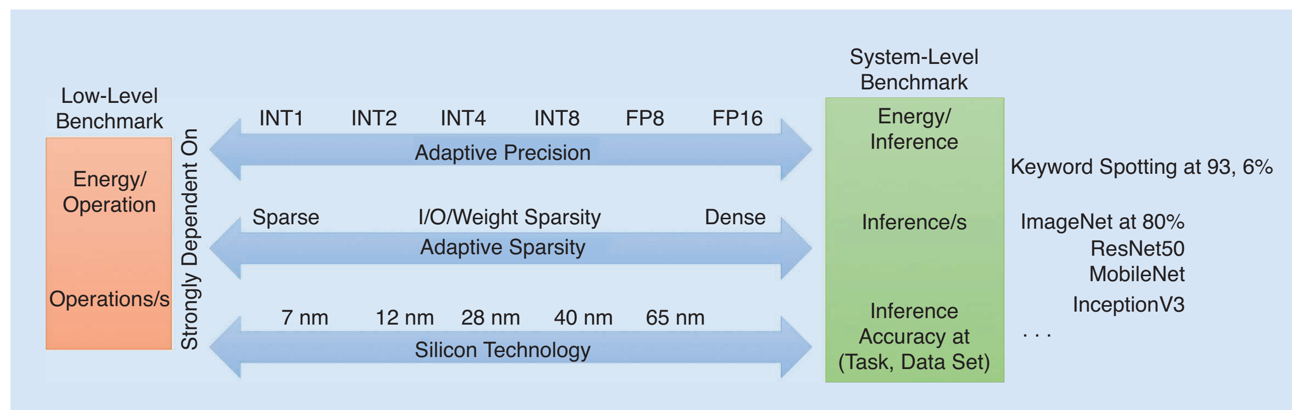

FIGURE 24: Various parameters impacting the low- and system-level benchmarking metrics. INT: integer.

enabling breakthroughs in energy efficiency and throughput. Four SRAM (with CIM) papers are being presented, with the potential of enabling further breakthroughs for AI and deep-learning applications, featuring low-power and/or high-performance operation; high-accuracy, in-memory, multibit MAC operation; and the ability to run forward as well as backward calculations for inference and training. Figure 26 shows the SRAM bit-cell area and V_{MIN} scaling trend.

High-Bandwidth and Low-Power DRAM

To keep pace with the ever-increasing performance requirements in various applications from mobile to supercomputing, DRAM continues to scale in density, form factor, and bandwidth. ISSCC 2020 will include benchmarks for the latest interface standards, e.g., an 8.5-Gb/s LPDDR5 for high-speed mobile and a 640-GB/s HBM2E for the highest performance applications (cloud and AI). Three papers focus on improvements for very-high-speed interfaces, such as a PAM4 32-Gb/s transceiver and an 18-Gb/s GDDR6 PHY. Figure 27 illustrates DRAM bandwidth scaling over the past 12 years.

Nonvolatile Memory

During the past decade, significant investment has been put into the emerging-memories field to find an alternative to floating-gate-based nonvolatile memory (NVM). The emerging NVMs, such as phase-change memory (PCM), ferroelectric RAM (FeRAM), STT-MRAM, and ReRAM, exhibit the potential to achieve a high cycling capability and lower power per bit in read/write operations. At ISSCC 2020, a 22-nm, 1-Mb STT-MRAM macro demonstrates a high read bandwidth of 42.67 GB/s, while a 4-b/cell NAND improves the write bandwidth up to 30 MB/s. Figure 28 highlights the achievement of MRAM read bandwidth as well as improvement of the 4-b/cell NAND flash write throughput. Such high densities are achieved through advancements in 3D vertical bit-cell

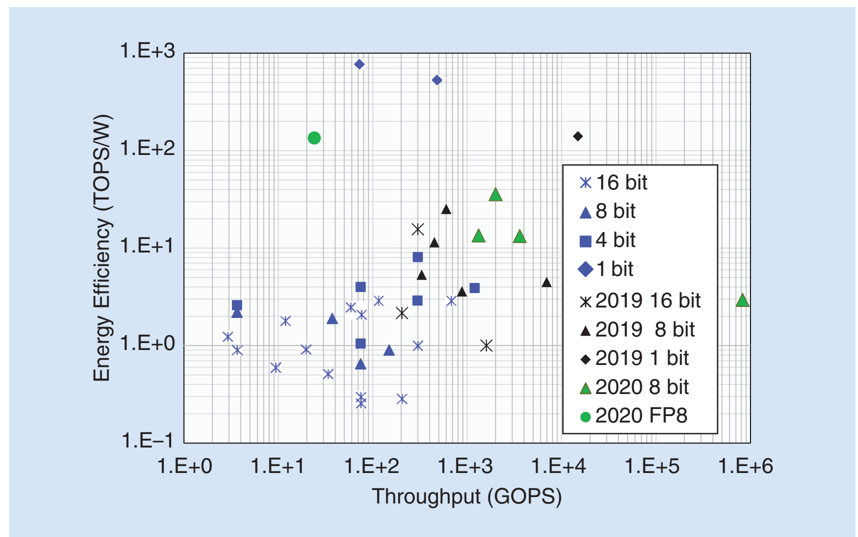

FIGURE 25: Deep-learning processor throughput and efficiency. GOPS: giga operations/s.

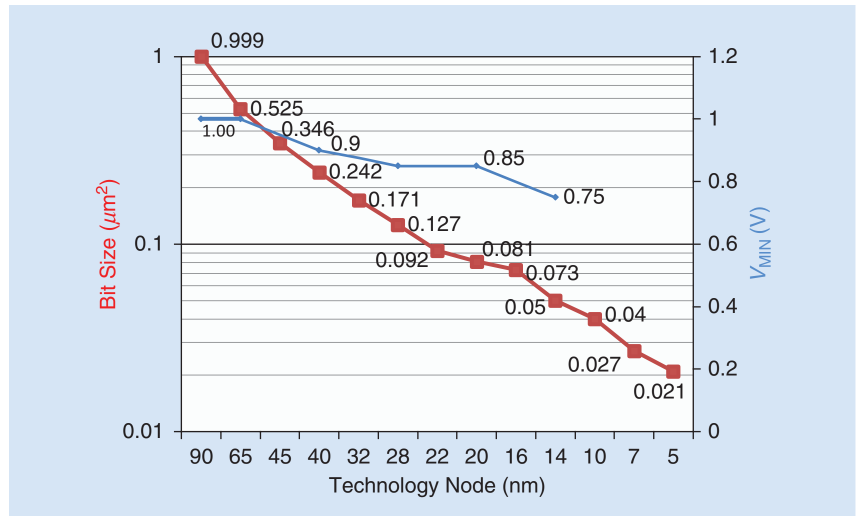

FIGURE 26: The bit-cell area and V_{MIN} scaling trend for SRAM.

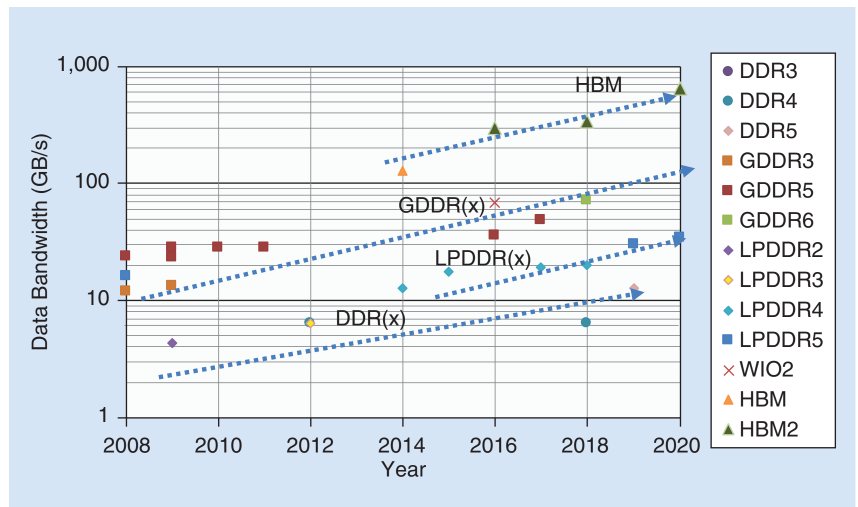

FIGURE 27: DRAM data-bandwidth trends. WIO: wide I/O.

stacking and multibits (2–4 b) per bitcell technologies. Figure 29 presents the trend in NVM capacity.

NAND Flash Memory

NAND flash memory continues to advance toward a higher density and lower power, resulting in low-cost storage solutions that replace traditional hard disks with solid-state disks. In the semiconductor industry, 3D-memory technology has been the mainstream for NAND flash memory in mass production. At ISSCC 2020, there are two papers demonstrating improvement of the write bandwidth of 4-b/cell, 3D NAND flash at 1-Tb capacities. One is a 92-stacked-word-line, 3D vertical NAND (VNAND) flash memory featuring 5G technology with 1.2-Gb/s high-speed interfaces. Another exhibits a 30-MB/s program throughput utilizing the highly area-efficient technology of peripheral circuits under the memory cell array, which achieves an 8.4-Gb/mm^2 area capacity. On the other hand, fast-speed 3D NAND with a 75-μs program time and 4-μs read latency was developed. With a flexible suspend operation for program and erase, a smaller random-read latency of fewer than 50 μs is achieved. Figure 30 describes the observed trend in NAND-flash capacities at ISSCC during the past 20 years.

Innovative Topics: Medical

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium

As illustrated during ISSCC 2020, sensor and actuator systems for on-body wearable and in-body implantable use continue to evolve toward more robust, functionally complex, and energy-efficient solutions as well as closed-loop operation. Wearable and implantable SOCs record weak biopotential signals in the presence of real-life interference and under stringent power and size constraints. These new SOCs and corresponding techniques for wireless power/data transfer pave the way toward robust microdevices that involve direct sensing, multisensor fusion, and implantable closed-loop sensor/actuator systems. These advancements enable multimode physiological recordings from nearly every major organ system.

The state of the art in biomedical ICs and systems is being advanced at ISSCC 2020, with miniaturization, higher sensitivity, higher dynamic range, and interference mitigation presented as major trends in implantable and in vivo diagnostic devices at the same time that power efficiency continues to improve. High-dynamic-range sensing systems (>100 dB) improve tolerance to large amplitude interference and motion artifacts, while new techniques are introduced to sense physiological

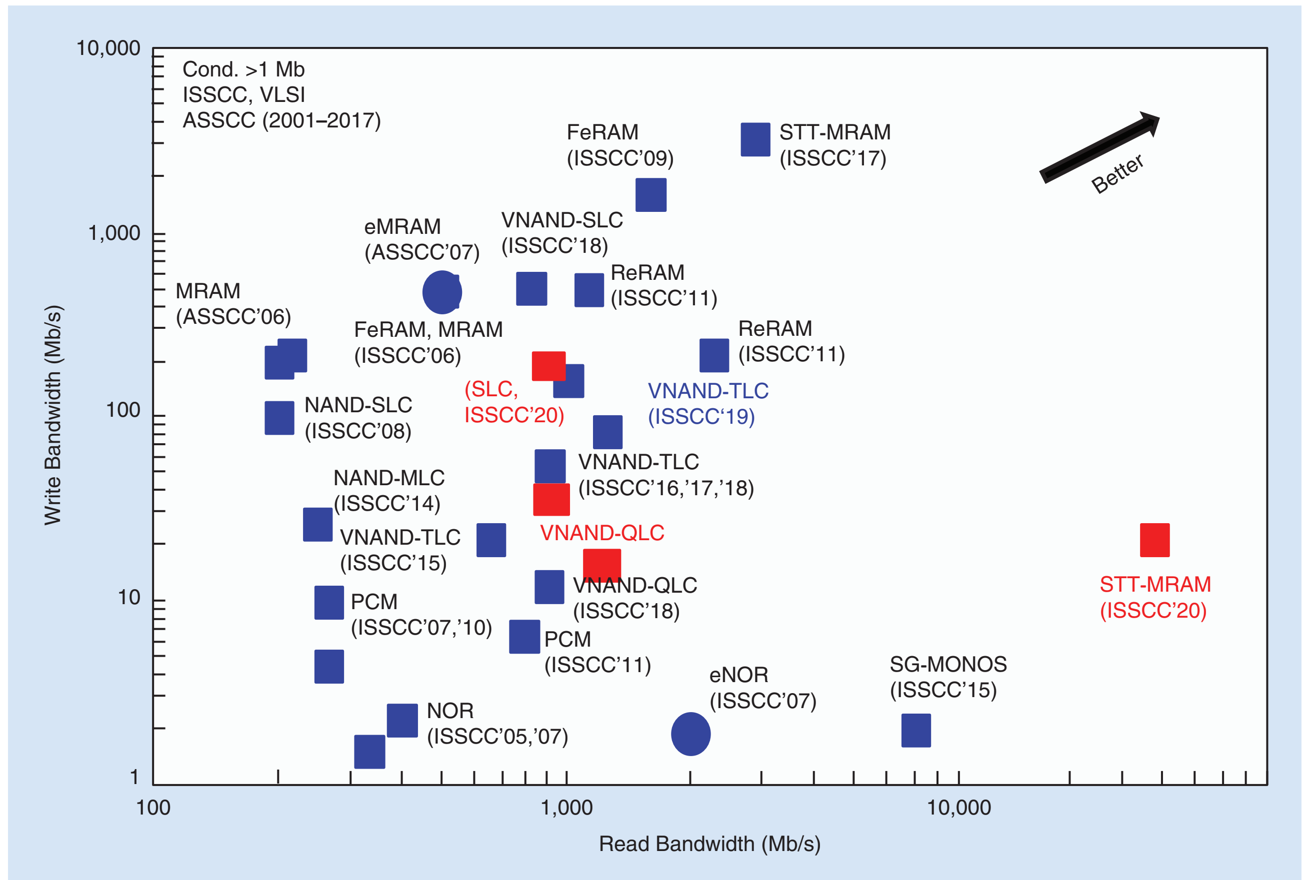

FIGURE 28: A comparison of read/write bandwidth for NVMs. VLSI Circuits: Symposia on VLSI Technology and Circuits. SLC: single-level cell; TLC: triple-level cell; MLC: multilevel cell; eMRAM: embedded MRAM; PCM: phase-change memory; SG-MONOS: split-gate metal-oxide–nitride-oxide–silicon; QLC: quad-level cell; NOR: an inverted NAND; eNOR: embedded NOR.

signals, such as photoplethysmograms and electrocardiograms. Miniaturization combined with a high level of integration enables minimally invasive implants with low tissue displacement for interfacing with the body. Multimodal physiological sensors have the potential to offer improved monitoring and diagnosis of a number of chronic conditions. The form factor of a low-cost, easy-to-use wearable device will enable continuous monitoring of multiple vital signs, facilitating health tracking outside the hospital. These advances offer tremendous market potential in the medical and consumer market spaces.

Innovative Topics: Imagers

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium

CMOS image-sensor business remains one of the fastest-growing segments of the semiconductor industry, expected to reach US$18 billion in 2024, up from US$11.8 billion in 2018. Image sensors are essential components in mobile devices and are found in many consumer-electronics products. Strong demand for automobile driver assistance and autonomy propels progress in time-of-flight sensors as well as high-performance 2D imagers. Backside illumination and 3D-stacked processing offer improved performance with increased on-chip functionality and new features integrated at the pixel level.

At ISSCC 2020, four of the 10 image sensors were designed for direct and indirect time-of-flight imaging. Progress has been made in spatial and depth resolution compared to previous designs, leading to a longer range and higher accuracy. In Toshiba's lidar chip, circuit optimizations facilitate a 2× higher channel density in the same die size. Four other image sensors being presented at ISSCC 2020 target mainstream applications with improvements in pixel size, global shutter, low noise, and high dynamic range.

Samsung has scaled down the pixel pitch to 0.7 μm while improving or maintaining critical performance parameters. Robust backside-illuminated global shutter pixels with −105-dB parasitic-light sensitivity have been announced. Sony reports noise-level improvements and selectable in-pixel gain without adding transistors. A single-exposure, 132-dB dynamic range that maintains a high signal-to-noise ratio across the full range is presented. Finally, two image sensors are intended for low-power/low-data-rate applications, with always-on imaging and event-based dynamic vision. Improvements in the architecture and data conversion have continued to drive down power consumption while providing the necessary compression, image quality, and detection for targeted applications.

Innovative Topics: Technology Directions

Subcommittee Chair: Makoto Nagata, Kobe University, Japan

Technology innovations bring the promise of enabling new system functionalities and substantially increasing the efficiency of existing ones. Harnessing such innovations for solving tangible real-world problems requires novel system-level solutions. With a focus on envisioning the future, emerging trends in technology directions presented at ISSCC 2020 cover a wide range of topics, including quantum engineering; embedded NVM-based computing devices

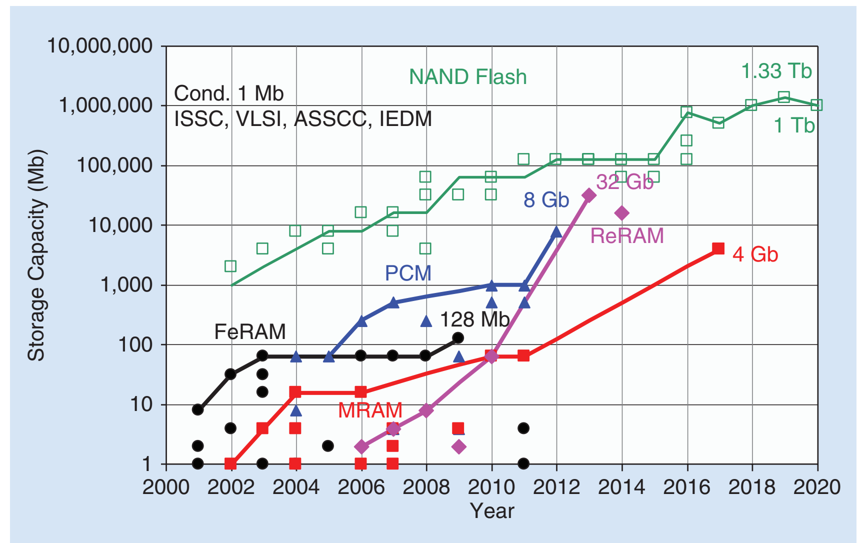

FIGURE 29: The memory-capacity trend for emerging NVMs. IEDM: IEEE Electron Devices Meeting.

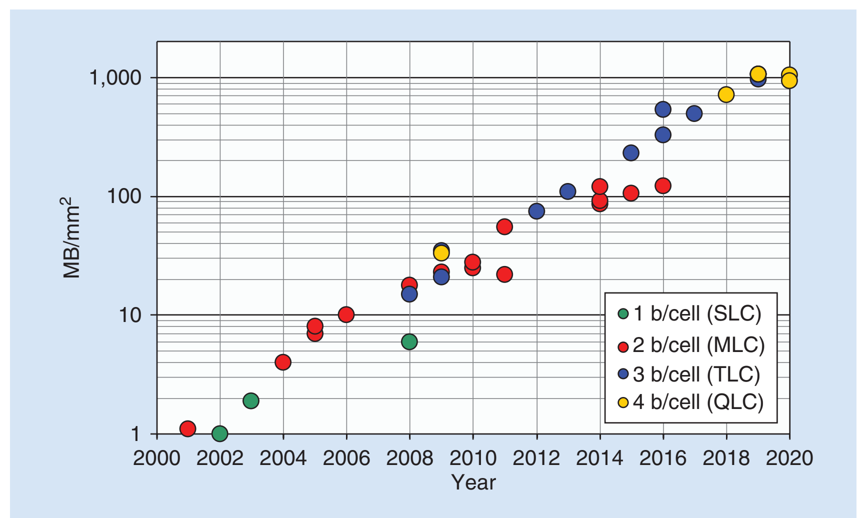

FIGURE 30: NAND flash-memory trends.

Multimodal physiological sensors have the potential to offer improved monitoring and diagnosis of a number of chronic conditions.

for next-generation AI architectures; low-power circuits for IoT and health technologies; and biomedical sensing, stimulation, and harvesting. ISSCC 2020 features four sessions representing the latest technological innovations in the following areas.

Quantum Engineering

Quantum technologies are emerging as a major multidisciplinary research topic, including computing, sensing, telecommunications, information technology, and security. Common to these technologies are properties typical of quantum mechanics, such as superposition and entanglement. Recently, engineers have developed techniques to exploit these properties using solid-state circuits, employed to control and observe a growing number of quantum devices. Since most quantum devices must be operated at deep cryogenic temperatures, circuits must also operate at those or comparable temperatures to ensure compact, reliable, and, especially, scalable systems. Leveraging more than 60 years of CMOS-technology development, researchers are increasingly engaged in cryogenic CMOS (cryo-CMOS) circuits and systems to fill this gap. Cryo-CMOS technologies will serve a range of quantum devices that can be used in several quantum-engineering problems. ISSCC 2020 will feature a session devoted to some of these topics, including a cryo-CMOS controller for spin and superconducting qubits and an integrated system for the control of a double quantum dot that is also integrated in CMOS.

Next-Generation Nonvolatile Devices

Nonvolatile devices are enabling novel architectures with improved energy and area efficiencies. A relentless push to intersect evolving AI applications embodies larger-scale NVM-based CIM implementations featuring neural-network processors. The trend continues this year with CIM support for multibit inputs/weights/outputs and low-power, parallel-data-path operations. ISSCC 2020 highlights two ReRAM-based energy-efficient silicon chips using analog in-memory operation: one with a reconfigurable dataflow and the second with fast, parallel multibit computation enabled by a signed-weighted ReRAM array.

Low-Power Circuits for the IoT and Health

The papers from ISSCC 2020 in this area push the frontiers of lower-power solutions in IoT and health applications. One paper presents an ultralow-power IC designed for communicating with commodity Wi-Fi transceivers via backscattering. Another introduces a nanowatt-class (54-nW) always-on wake-up chip for general-purpose IoT devices. A third describes an electronic nose with very accurate limit of detection. In addition, advances in silicon for 3D localization based on magnetic-field-gradient sensing for surgical implants is presented.

Biomedical Sensing, Stimulation, and Harvesting

ISSCC 2020 includes innovative and emerging biomedical systems for wearables and implantable components for timely medical intervention. The developing trends encompass advances in implantable sensors and stimulators, human-body coupled communication, ambient energy harvesting, and novel magnetoelectric effects for power and data transfer. The technologies demonstrate the promise to advance cancer therapy, neurostimulation, retinal prosthesis, and diagnostic devices.

Summary

According to the Semiconductor Industry Association, the industry generated US$468.8 billion in sales in 2018, an increase of 13.7 percent compared to 2017! In this environment, ISSCC continues to be the premier technical forum for presenting advances and predicting trends in solid-state circuits and systems. Beyond this article, a complete trends document will be available at www.isscc.org. These trends will be highlighted in papers presented at the 67th ISSCC, being held at the San Francisco Marriott Marquis on 16–20 February 2020. Attendance at ISSCC 2020 is expected to be around 3,000. Corporate attendees from the semiconductor and system industries typically represent about 60% of attendees. We look forward to seeing you there!

Acknowledgments

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Kenneth C. Smith is a professor emeritus and serves as chair of the Board of Advisors for the Division of Engineering Science, University of Toronto, Canada. Since 1975, he has volunteered for ISSCC in various capacities, including as a member of the Program Committee, in press-related roles, and, for 40-plus years, as chair of the Awards Committee.