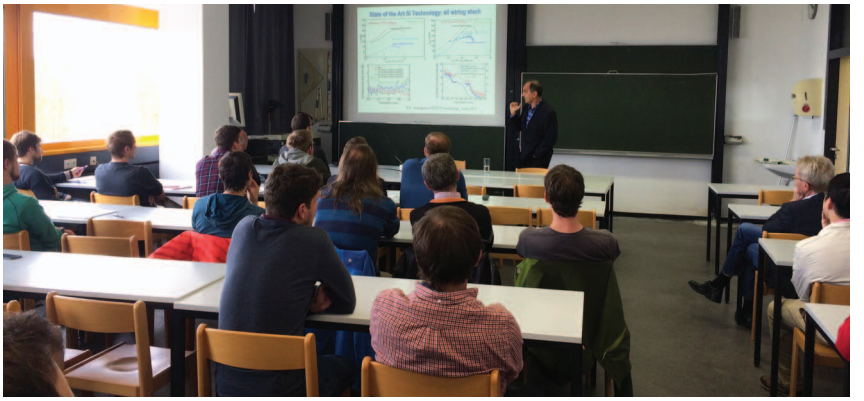
SSCS Germany Chapter Holds DL Talk at the University of Erlangen

On 9 October 2017, Distinguished Lecturer (DL) Prof. Sorin P. Voinigescu of the University of Toronto, Canada, spoke at the Friedrich-Alexander-University of Erlangen-Nuremberg (FAU), Germany. The talk was organized by the IEEE Solid-State Circuits Society Germany Chapter and was moderated by Prof. Robert Weigel of FAU.

Voinigescu's talk, "Circuit Topologies and Design Methodologies for High Data-Rate mm-Wave Radio Transceivers in SOI and FDSOI CMOS," explored fully digital architectures and circuit topologies for future wireless backhaul systems with aggregate data rates comparable to those of future 64-Gbaud fiberoptic systems. The main features of fully depleted silicon-on-insulator (FDSOI) complementary metal–oxide–semiconductor (CMOS) technology and how to efficiently use its unique features for radio frequency and mm-wave system-on-chips were reviewed first. Also discussed was the impact of the back-gate bias on the measured I-V, transconductance, f_T and f_{MAX} characteristics and comparison of the maximum available gain of FDSOI MOS field-effect transistors with those of planar bulk CMOS, SOI, and silicon-germanium BiCMOS transistors through measurements up to 325 GHz. Voinigescu provided examples of FDSOI low-noise amplifiers, mixer, switches, and power amplifier circuit topologies and layouts that make efficient use of the back-gate bias to overcome the limitations associated with the low breakdown voltage of sub-28 nm CMOS technologies. Examples of measured 45-nm SOI

Prof. Voinigescu (center) with (from left) Prof. Liang Zhou (Jiao Tong University, Shanghai), Mandred Berroth (University of Stuttgart), Robert Weigel (FAU), and Renato Negrat (Rheinisch-Westfälische Technische Hochschule Aachen) pose around an exhibit of the first and 15th edition of the Tietze–Schenk book, the German bible of semiconductor circuit design.



An audience of over 40 people attended the talk.

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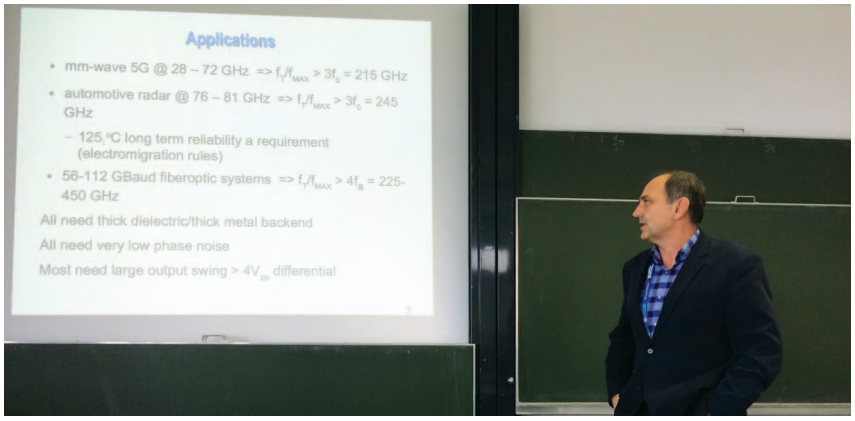


Prof. Voinigescu presents "Circuit Topologies and Design Methodologies for High Data-Rate mm-Wave Radio Transceivers in SOI and FDSOI CMOS."

CMOS digital transmitters with free space constellation formation at 100 and 140 GHz were presented along with a 1–30 GHz fully digital I-Q transmitter with 20-dBm output power for 5G terminals. Finally, predistortion and spectral shaping techniques in the transmitter and receiver analog-to-digital converter-based equalization at 64 GBaud were discussed.

An audience of over 40 people attended the talk, which was held in the Tietze-Schenk Room of the FAU.

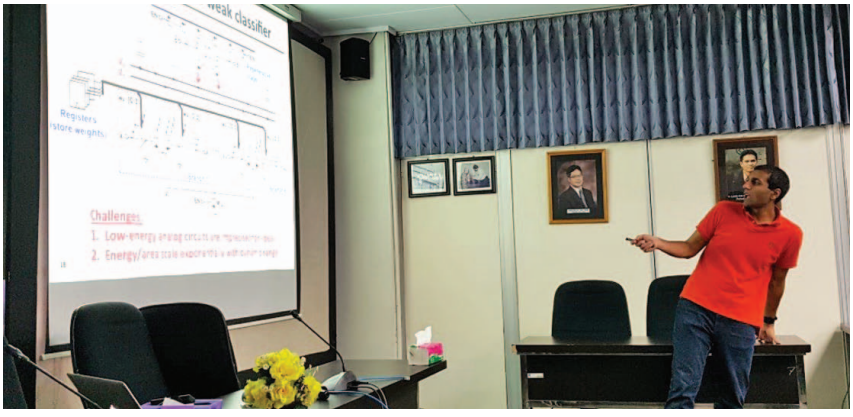
—Robert Weigel

SSCS DL Naveen Verma Visits Universitas Gadjah Mada

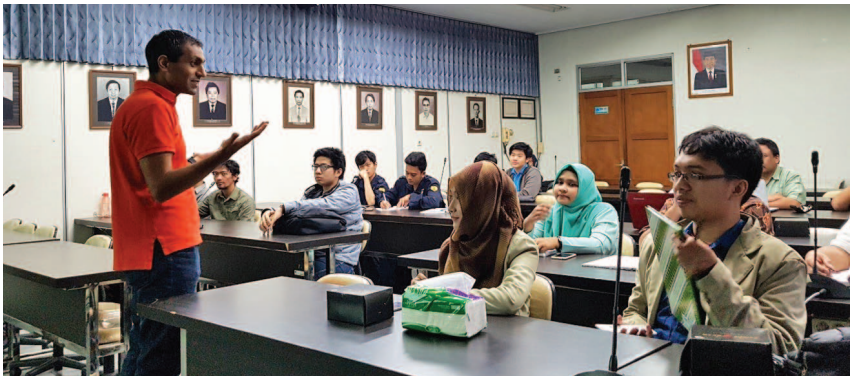
The IEEE Solid-State Circuits Society Indonesia Chapter organized a talk by Distinguished Lecturer (DL) Dr. Naveen Verma on 10 August 2017. The talk was held at the Universitas Gadjah Mada (UGM) at the Department of Electrical Engineering and Information Technology (DEEIT).

Verma, an associate professor with the Department of Electrical Engineering, Princeton University, New Jersey, is an expert on ultra-low-power systems and platform components for low-power processing and communication in advanced and emerging technologies.

Verma delivered the lecture "Exploiting Machine-Learning Algorithms for Very Low-Power Implementations," which was attended by approximately 30 people consisting of faculty, staff, and students. The lecture was moderated by Dr. Agus Bejo, a member of the Digital System Laboratory.



Dr. Verma presents "Exploiting Machine-Learning Algorithms for Very Low-Power Implementations" at UGM.



Audience members listened to Dr. Verma's lecture with great enthusiasm.

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