Ali Sheikholeslami

Looking into a Node

Welcome to "Circuit Intuitions." This is the first article of a series that will appear regularly in this magazine. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. If you read this article, I would appreciate your comments and feedback, as well as your requests and suggestions for future articles in this series. Please send your e-mails to ali@ece.utoronto.ca.

What do you see when looking into a node of a linear time-invariant circuit? Most circuit designers simply see the Thevenin or Norton equivalent circuit of that node with respect to ground. We explore this for circuits including transistors. We limit ourselves to metal–oxide–semiconductor (MOS) transistors for now, but the procedure outlined here is also applicable to bipolar transistors.

A well-known, small-signal model for MOS transistors at low frequencies is shown in Figure 1. This is a two-port network consisting of two voltage-controlled current sources, (one controlled by the gate-to-source voltage, v_{gs}, and one by the body-to-source voltage, v_{bs}) in parallel with the transistor's output resistance, r_o. Although this model is quite simple and can be used directly to analyze

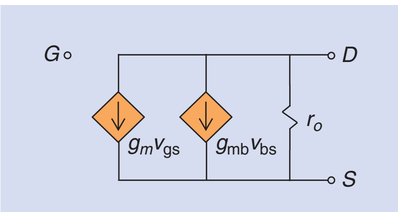

FIGURE 1: An MOS transistor small-signal model.

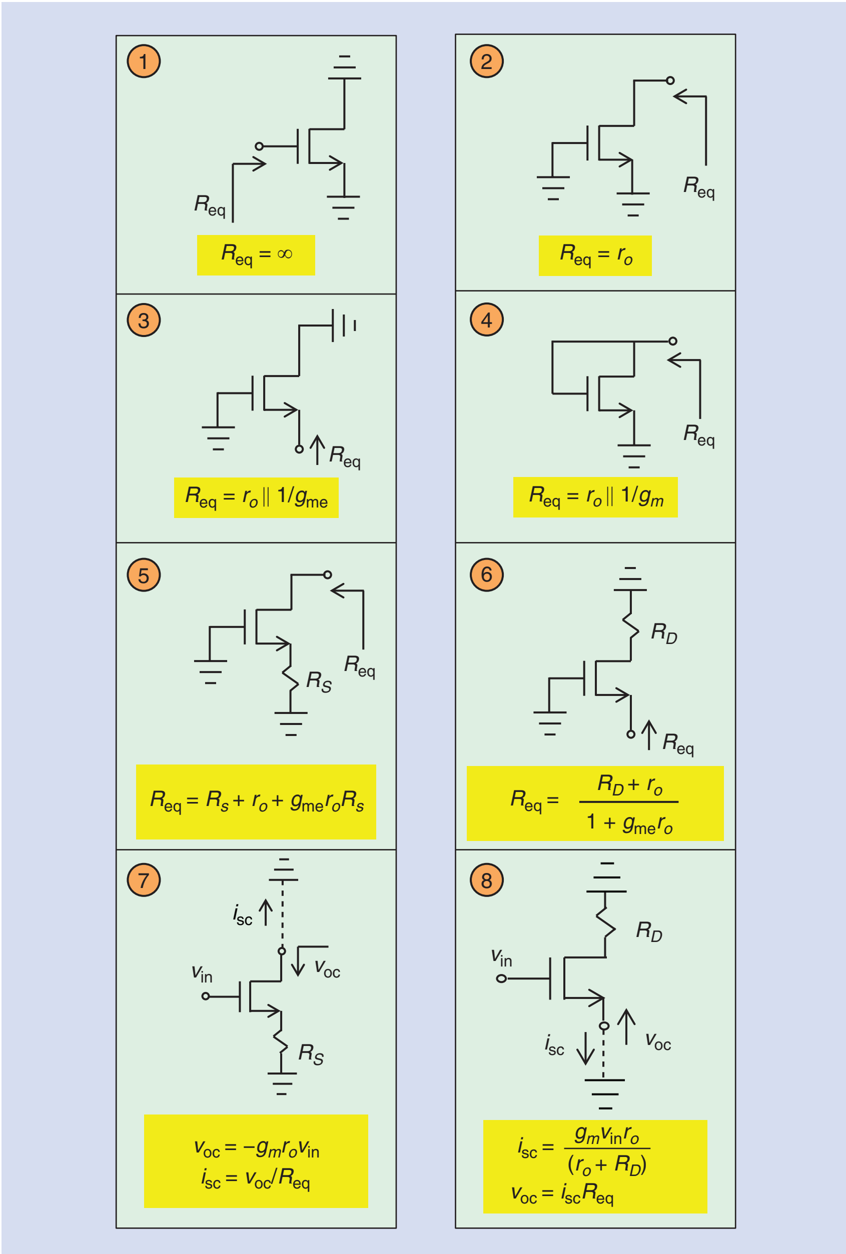

FIGURE 2: Library elements 1–8.

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circuits consisting of several transistors, a brute-force approach in writing KVL/KCL is prone to mistakes and may not provide intuition into how the circuit works. This article provides an alternative approach in analyzing transistor circuits by first building a library of "elements" that are common among many analog circuits. These elements can then be used for analysis and design.

Figure 2 shows eight basic elements, each consisting of a single NMOS transistor. Element 1 consists of an NMOS transistor with its source and drain grounded while looking into its gate. The equivalent circuit in this case is a resistor with infinite resistance (an open circuit). It can be seen easily that the equivalent resistance looking into the gate remains infinity even when there are resistors from the source and drain terminals to ground.

The second library element is an NMOS transistor with its gate and source grounded. Looking into the drain, we simply see r_o. This can be seen clearly from Figure 1 where both dependent sources disappear as a result of both v_{gs} and v_{bs} being zero.

Looking into the source of an NMOS transistor while its drain and gate are small-signal grounded (Element 3), we will see the resistance $r_o \| 1/g_{me}$. Here g_{me} refers to the *effective* g_m of the transistor, which is defined as the sum of g_m and g_{mb}, and "$\|$" denotes parallel combination.

Looking into the drain of a diode-connected transistor while the source is grounded (Element 4), we will see $r_o \| 1/g_m$. Note that in this case, the body effect is not observed simply because the source is grounded.

Next, we combine one transistor and one resistor to create Elements 5–8. Element 5 consists of an NMOS transistor with its gate grounded and its source connected via a resistor, R_S, to ground. It is easy to show that the equivalent circuit looking into the drain is a resistor whose resistance is $(1+g_{me}r_o)$ times R_S plus r_o. Similarly, looking into the source of an NMOS transistor with a resistor in the drain terminal (Element 6), we see a

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resistor whose value is given as the $r_o + R_D$ divided by $(1+g_{me}r_o)$.

In all the above cases (Elements 1–6), we have been finding the equivalent resistance looking into a node. This resistance is the Thevenin or Norton resistance looking into that node. Now, let us find either the Thevenin voltage source of a node, which we refer to as the open-circuit voltage of the node with respect to ground (v_{oc}), or the Norton current source, which we refer to as the short-circuit current (i_{sc}) flowing from the node to ground.

Element 7 consists of an NMOS transistor with source degeneration while its gate is driven by a small-signal voltage source v_{in}. We can either find v_{oc} or i_{sc} of the drain node; however,

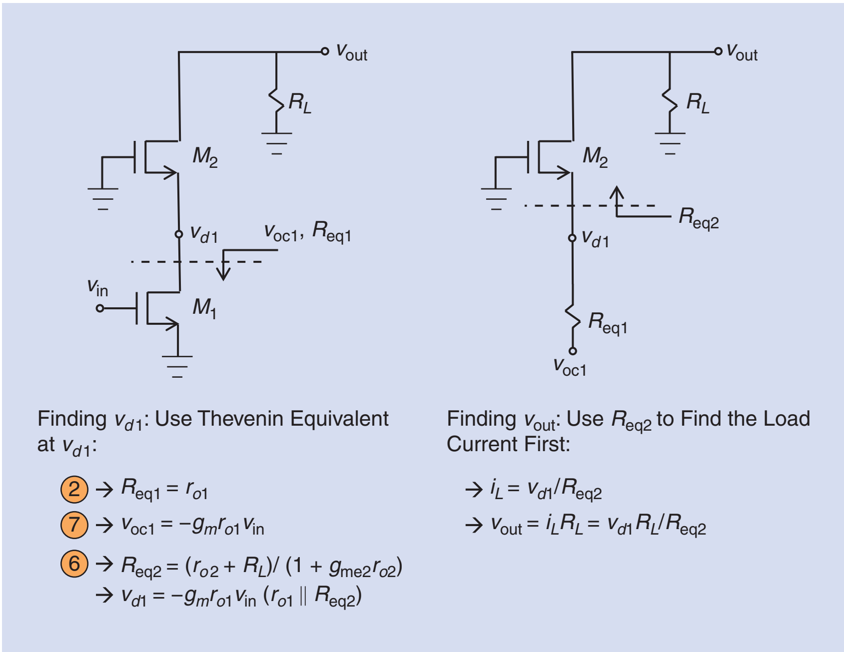

FIGURE 3: Finding v_{d1} and v_{out} in a cascode configuration using library elements.

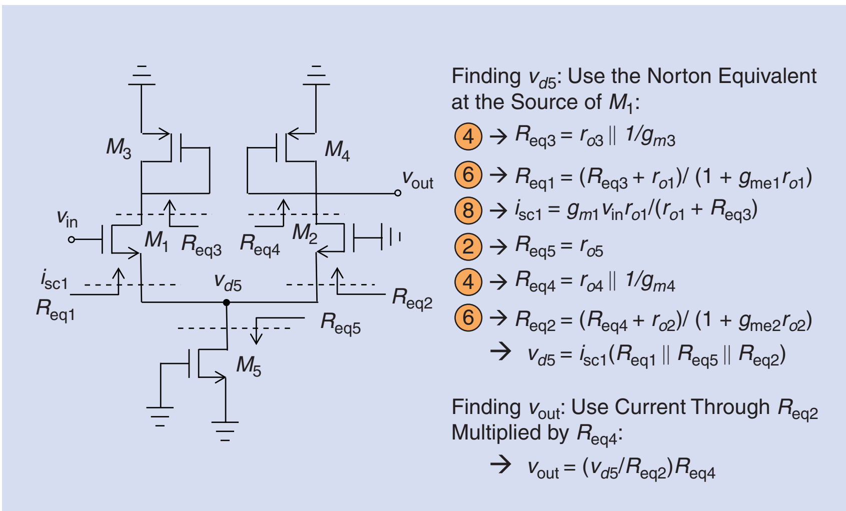

FIGURE 4: Finding v_{d5} and v_{out} in a differential pair using library elements.

it turns out that it is easier to find v_{oc} first. This is because with the circuit being open, the current that flows through R_S will be zero and this in turn makes v_s (and hence $g_m v_s$ and $g_m v_{bs}$) zero. As a result, the equivalent circuit will have an open-circuit voltage that is $-g_m r_o v_{in}$. Given this and the value of R_{eq} found in Element 5, we can find i_{sc} as $-g_m r_o v_{in}/R_{eq}$.

Finding i_{sc} proves to be easier when we look into the source of a transistor. This is illustrated in Element 8. Here, by shorting the source to ground, we effectively zero $g_m v_s$ and $g_{mb} v_{bs}$. The transistor current $g_m v_{in}$ now goes through a current divider consisting of r_o and R_D. Once we find i_{sc}, it is easy to find v_{oc} as i_{sc} times R_{eq} (as found in Element 6).

Now, we will use these elements to analyze two circuits shown in Figures 3 and 4. In Figure 3 (cascode configuration), we are interested in finding v_{out} as a function of v_{in}. We do this in two steps:

- We replace M_1 with its Thevenin equivalent circuit (using Elements 2 and 7) and replace M_2 and R_L with its equivalent resistance (using Element 6).
- Using these equivalent circuits, we find the current going to ground (which is equal to the current going through R_L) and hence the voltage across R_L.

The problem of finding the small-signal voltage of a node in a circuit including transistors reduces to the problem of finding the Thevenin and Norton equivalent circuits at that node.

Figure 4 shows a differential pair with diode connected loads. Here, we are interested in determining the voltage gain from the input to the common node (v_{d5}) and to the output voltage (v_{out}). The circuit consists of five transistors, and as such it would be time-consuming and cumbersome to draw the small-signal models for all the transistors. To find v_{d5}, we use the short-circuit current (i_{scl}) at this node along with the three resistances that are connected to this node in parallel (R_{eq1}, R_{eq5}, and R_{eq2}). v_{d5} can then be found as a simple product of i_{sc} and $R_{eq1} \parallel R_{eq5} \parallel R_{eq2}$. Once we know v_{d5}, we find the current that goes through R_{eq2} (and hence through R_{eq4}). v_{out} is then equal to v_{d5}/R_{eq2} times R_{eq4}.

In summary, using elements introduced in this article, the problem of finding the small-signal voltage of a node in a circuit including transistors reduces to the problem of finding the Thevenin and Norton equivalent circuits at that node.

References

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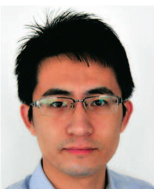
CONTRIBUTORS (Continued from p. 3)

JONAS HANDWERKER is working toward his Ph.D. degree at the Institute of Microelectronics at the University of Ulm, Germany.



TIANYI LIU is a research assistant/Ph.D. candidate at the Institute of Microelectronics, Faculty of Engineering and Computer Science, University of Ulm, Germany.

MAURITS ORTMANNS is a full professor at the University of Ulm, Germany.

HANSPETER SCHMID is the professor for analog microelectronics at IME/FHNW and is also a part-time senior lecturer at ETH Zürich.

ALEX HUBER is with the Institute of Microelectronics of the University of Applied Sciences Northwestern Switzerland, Windisch.