SSCS Circuit Analysis and Design Contest: The Winners of the 2022 Edition

The SSCS Student Circuit Contest is a worldwide competition open to both undergraduate and graduate students around the world. This year the contest changed its format by opening to a more creative format, where each participant has to design his own integrated circuit by starting from a predefined list of components. While the technology adopted can vary, some rules have to be respected:

- The circuit has to have one ground (GND) and one voltage supply (VDD) compatible with the technology you use.
- Each component of the list can be used only once.
- The use of each component must be necessary for the proper functionality of the proposed circuit (e.g., no dummies components).
- The proposed circuits have to have at least an identified output.
- Component parameters specified in the provided list cannot be changed (others will depend on the technology you choose, such as Cox, mobility, voltage threshold, supply voltage, etc.).
- Circuits must be simulated and simulation results must be provided to demonstrate a proper functionality.

This year the list of components was as follows:

- ideal input voltage source
- ideal current source (25 uA)
- GND net
- VDD net connected to a supply
- 10 transistors with the following aspect ratio (W/L):
  - 5 pMOSFET: (20/1) (20/1) (5/1) (5/1) (5/1) - four terminal device (gate, drain, source, body)
  - 5 nMOSFET: (20/1) (20/1) (10/1) (10/1) (10/1) - four terminal device (gate, drain, source, body)
- three ideal resistors 5 kΩ, 10 kΩ, 20 kΩ
- Jolly component: one ideal capacitor with an arbitrary value.

You would be surprised how many circuits can be designed starting from this limited number of devices (operational amplifiers, data converters, voltage regulators, etc.). We received many amazing solutions this year and this column will show you the three most interesting and completed, selected by the circuit contest committee. Enjoy your reading and be prepared for the next edition!

—Antonio Liscidini

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The Three Winners and Their Solutions

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A "Three-Transistor" High-Gain Amplifier

This submission to the 2022 SSCS Student Circuit Contest describes a high-gain amplifier. The goal of the contest is to use as many components from a provided list as possible while implementing a functional circuit. The proposed amplifier is implemented in a 0.18-μm CMOS technology. It achieves a 43-dB voltage gain with a power consumption of 0.66 mW, while using all the components from the list. This amplifier was identified by running a custom-made software that was configured to select all possible functional three-transistor circuits. This particular circuit was chosen because of its uncommon configuration that nearly achieves the highest gain of all 56,280 three-transistor circuits identified, while also exhibiting real input impedance.

Introduction

This submission to the 2022 SSCS Student Circuit Contest describes a high-gain amplifier. The objective of the contest challenge is to use all components from a given list to design an integrated circuit. To participate in this contest, we investigated an unusual amplifier topology that is capable of achieving high voltage gain and can also realize real input impedance for situations when input power matching is required. This circuit was inspired by work in [1]. The following sections describe an implementation of the amplifier based on the components prescribed by the contest rules.

Amplifier Implementation

Circuit Topology Evolution

To introduce the circuit, we start with a common-source (CS) NMOS in Figure 1(a). The voltage gain of this circuit is $-g_{m1}/(g_{ds1}+R_L^{-1})$. The gain can be increased by adding a cascode M_2 in Figure 1(b) to increase the output resistance. However, if R_L is not very high, M_2 has a minimal effect on gain. If the input is applied to both M_1 and M_2 as in Figure 1(c), M_1 tries to sink higher current than provided by M_2, enters triode, and does not amplify the signal, making the stack of two transistors equivalent to a CS NMOS with a longer gate length. We now suppose that the drain voltage of M_1 is controlled to set M_1 to saturation, as in Figure 1(d). The effective transconductance of the whole circuit increases from g_{m1} in Figure 1(b) to $\sim(g_{m1}+g_{m2})$, with the help of the indicated "dc control" circuit (DCC). We require that the DCC does not load the drain of M_1 and is able to accommodate a $g_{m1}v_{in}$ small-signal current flowing through M_1, and $g_{m2}(v_{in}-v_{d1})\approx g_{m2}v_{in}(1+g_{m1}/g_{m2})$ current flowing through M_2, where v_{d1} is indicated in Figure 1(d). This is equivalent to nearly doubling the voltage gain. To increase the gain further, an active load with a high output resistance is used in Figure 1(e). Since now M_1 sees a high resistance at its drain, the voltage gain of M_1 increases (in magnitude) from $\sim -g_{m1}/g_{m2}$ in Figure 1(d) when R_L is not very large to $\sim -g_{m1}/g_{ds1}$. If we again assume that the DCC can accommodate unequal currents in M_1 and M_2, the overall voltage gain becomes $-[g_{m2}g_{m1}+g_{m2}g_{ds1}+g_{m1}g_{ds2}]/g_{ds1}g_{ds2}$. Compared to the gain of the circuit in Figure 1(b), this new gain is slightly higher when R_L is large, and much higher when R_L is not large. However, the flow of current I_1 directly into M_2 may cause some of the transistors, e.g., M_1 or M_2 or in I_1, to enter triode, thereby requiring a means for keeping them in saturation.

Since we would also like to generate a real part to the input impedance for potential future use in RF systems, we configure M_1 in a pseudo diode-connected configuration, in which another transistor, i.e., M_3,

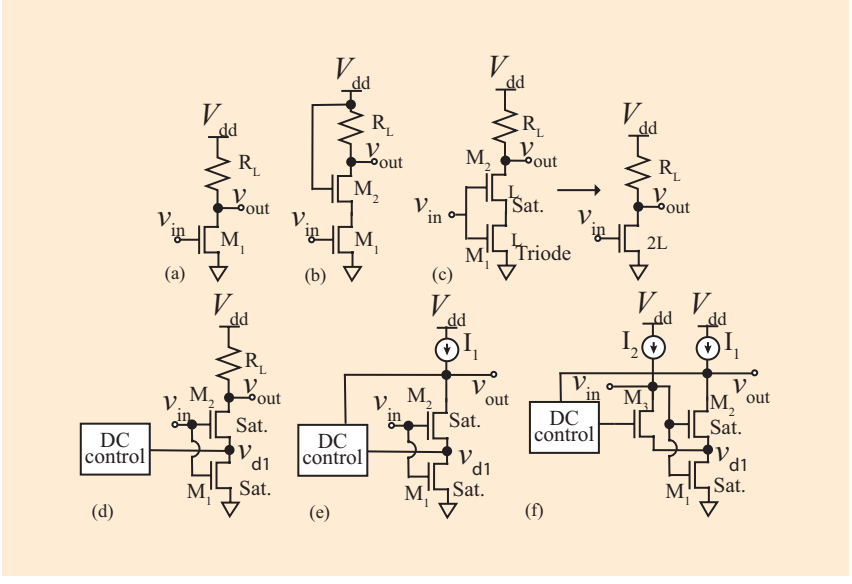

FIGURE 1: Evolution of circuits leading to the prototype circuit in (f). (a) CS amplifier, (b) cascode, (c) stacked, (d) stacked with dc level control, (e) proposed high-gain amplifier, and (f) proposed high-gain "three-transistor" amplifier with real input resistance. Biasing is not shown.

is used at the drain of M_1 as shown in Figure 1(f). When this connection is made, the input impedance becomes $\sim 1/g_{m1}$ and provides a means of input power matching. However, this connection reduces the impedance at the node v_{d1} in Figure 1(f), thereby reducing the gain of the circuit. To reduce the number of circuits connected to node v_{d1}, the DCC can be connected to the gate of M_3. A simplified small-signal analysis, whereby the gate of M_3 is assumed ac-grounded, describes the circuit voltage gain as:

$$A_v \approx -\frac{g_{m2}(g_{m1}+g_{m3}+g_{ds1})+(g_{m1}-g_{ds3})g_{ds2}}{g_{ds2}(g_{m3}+g_{ds1}+g_{ds2})} \quad (1)$$

$$\approx -\frac{g_{m2}}{g_{ds2}}\left(1+\frac{g_{m1}}{g_{m3}}\right), \quad (2)$$

where $g_{m1,2,3}$ and $g_{ds1,2,3}$ are the transconductances and output conductances of M_1 to M_3. Large gain A_v in (1) requires a small g_{m3}. The input resistance of this circuit is:

$$R_{in} = \frac{g_{m3}+g_{ds1}+g_{ds3}}{g_{ds1}g_{ds3}+g_{m1}(g_{m3}+g_{ds3})} \approx \frac{1}{g_{m1}}. \quad (3)$$

M_3 is responsible for supplying current through M_1 in addition to what is coming from M_2. This makes it possible to keep M_1 in saturation. While the requirement for having a real part of input impedance reduces the voltage gain, it is an important feature for high-frequency circuits that require input power matching.

Proposed Circuit

The key element of the three-transistor prototype circuit in Figure 1(f) is the DCC. For a proper functionality of the DCC, it should not reduce the impedance at the drain of M_1 and should sense and adjust the dc voltage at a node, i.e., the output node, in the circuit. Figure 2(a) identifies in green the proposed implementation of the DCC, where R_1 senses DC voltage at node v_{out} without overly loading that node. The $M_{p1}-R_2$ amplifier exhibits a negative gain, A_d, and drives the gate of M_3.

At low frequencies, the $M_{p1}-R_2$ amplifier senses v_{out} and adjusts both the gate voltage of M_3 and the voltage at the source terminal of M_2 to compensate for any unexpected drifts in the drain of M_2. As a result, the combined current through M_2 and M_3 equals the current through I_1 and I_2 while maintaining saturation. To visualize the operation of the $M_{p1}-R_2$ amplifier, let us consider a momentary decrease in the M_2 dc drain voltage due to PVT. Because of M_{p1}, this decrease causes an increase in the gate voltage of M_3, thereby reducing the gate voltage and the current of M_2 and counteracting the initial decrease in the M_2 drain voltage.

With the DCC in place, the gain of the circuit becomes:

$$A'_v \approx -\frac{g_{m2}}{g_{ds2}}\left(1+\frac{g_{m1}+A_d g_{m3}\dfrac{g_{m2}}{g_{ds2}}}{g_{m3}-A_d g_{m3}\dfrac{g_{m2}}{g_{ds2}}}\right) \quad (4)$$

Since at low frequencies A_d is negative, the loop is stable. At higher frequencies, parasitic phase shifts due to the input and output poles of the $M_{p1}-R_2$ amplifier make A_d positive and push the loop toward positive feedback. To prevent this from happening, a capacitor C_f is used in Figure 2(b) to effectively disconnect the loop at high frequencies and facilitate stable operation. With the capacitor in place, at high frequencies A'_v in (4) becomes equal to A_v in (1). The gain of the amplifier is further increased via gain boosting M_2 with a cascode $M_{4,5}-R_3$ stage in Figure 2(c). As the bulk-source voltage of M_2 is positive in this case, the signals at the gate and bulk terminals are out of phase for gain boosting. Current mirrors implement I_1 and I_2.

Amplifier Implementation With the Contest Components

The final implemented circuit is shown in Figure 2(c). As demonstrated in (1), $g_{m1,2}$ prominently contribute to the gain. Therefore, to maximize the gain of the final circuit, M_1 and M_2 are selected with the highest W/L ratios (20/1) available, where the length of M_2 is also increased to 0.9 μm to reduce g_{ds2}. M_3 is selected of the smallest available NMOS size to reduce g_{m3}.

The currents I_1 and I_2 are generated with a current mirror, whose reference current comes from an ideal

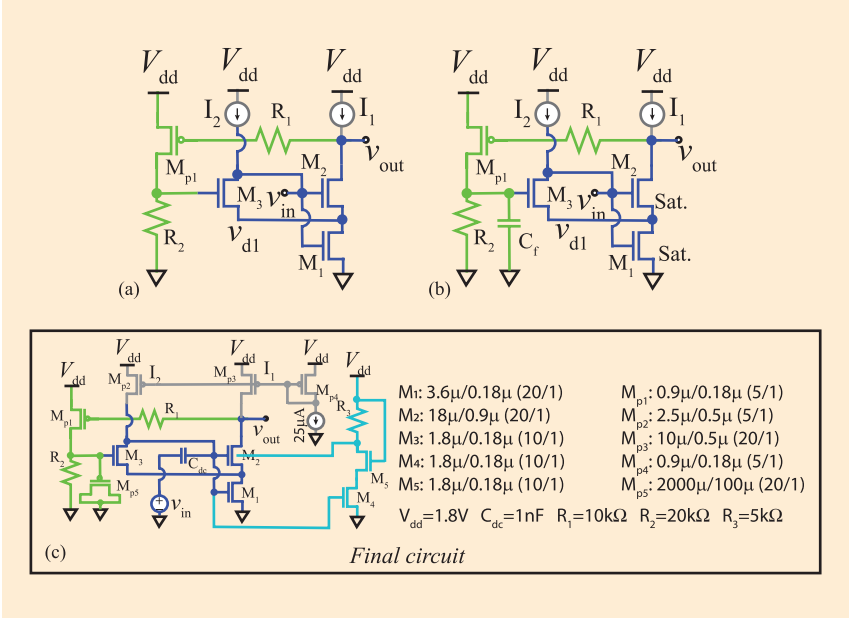

FIGURE 2: Steps leading to the proposed high-gain amplifier. (a) Prototype circuit with the DCC. (b) The circuit in (a) but with capacitor C_f included for stability. (c) Final proposed circuit. The main three-transistor gain stage is in blue. The green part identifies the DCC. The light blue identifies the gain-boosting amplifier. Biasing is shown in gray.

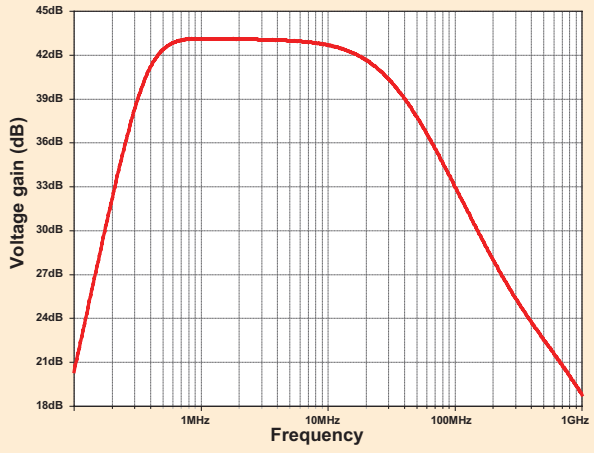

FIGURE 3: Simulated voltage gain.

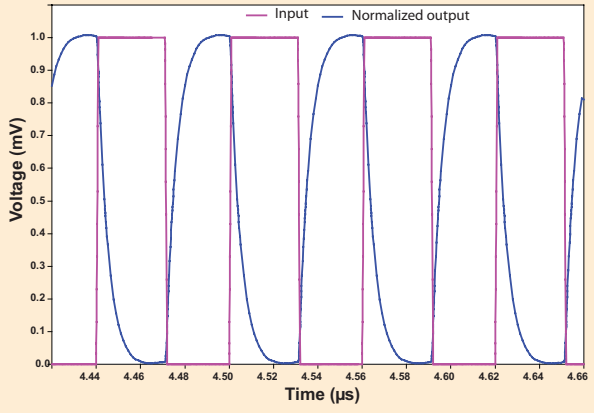

FIGURE 4: Simulated transient response.

25-μA current source. By selecting M_{p3} larger than M_{p4}, a large output current of ~100 μA from the mirror allows us to further increase g_{m2}. In addition, the 0.5-μm length of M_{p3} provides high output resistance and reduces its effect on the amplifier gain. A transistor M_{p2} is used to drive M_3 with a 25-μA current. The M_{p2} length is also set to 0.5 μm for high output resistance. Note that the low input resistance of the amplifier allows I_2 to flow into M_3 without transistors entering triode. A large M_{p5} implements C_f.

Identical, $M_{4,5}$ together with R_3 form a gain-boosting cascode, which increases the overall gain by 3 dB. In the final circuit optimization, the three available resistors were rotated through possible positions in the circuit to determine the ultimate configuration.

Circuit Simulation Results

The circuit was simulated using level 49 (Hspice-enhanced version of BSIM3v3) models in LTspice. The circuit gain, obtained with an ac analysis, is shown in Figure 3. The maximum voltage gain is 43 dB. The upper 3-dB corner is 33 MHz. The lower corner is determined by the feedback through the DCC. The current drawn by this circuit from a 1.8-V supply is 0.37 mA, resulting in the power consumption of 0.66 mW. Half of this current is consumed by the $M_{4,5}$ gain-boosting circuit. Other simulations showed that bandwidths into gigahertz can be achieved with this circuit, but the contest transistor parameters and resistor values limited the power consumption of this amplifier and its bandwidth. The simulated input resistance of this circuit is 1.5 kΩ. For 50 Ω matching, a higher power consumption than what is possible with the available components would be needed. The transient response to a square-wave input is shown in Figure 4. The transient behavior does not exhibit ringing.

Conclusion

This submission to the 2022 SSCS Student Circuit Contest presents a high-gain "three-transistor" amplifier, whose core is based on an uncommon three-transistor circuit that can achieve nearly the highest gain out of 56,280 possible functional three-transistor circuits. To meet the contest criteria, all available circuit components are used in this amplifier that achieve 43 dB of gain with a 0.66-mW power consumption in 0.18-μm CMOS.

Acknowledgment

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Kshitiz Tyagi, Student Member IEEE

A 10-T 20-Gb/s 203-μW CDR

We present a clock and data recovery (CDR) circuit consisting of only 10 transistors. The design comprises a voltage-controlled oscillator based on a new two-stage ring structure, a sample-and-hold–based phase detector, and a C²MOS latch for data recovery. Simulated in 28-nm CMOS technology, the circuit recovers clock and data from a 20-Gb/s nonreturn-to-zero input transmitted through a channel with 6.8-dB loss at the Nyquist-rate while consuming only 203-μW.

Introduction

CDR circuits are widely employed in wireline communication receivers in order to recover a low-jitter clock from random binary data that are distorted by lossy communication channels, and to recover the transmitted bit pattern with a very low bit-error rate (BER) (typically $\leq 10^{-12}$).

Typical CDR implementations [1] are comprised of a phase detector (PD) that is realized with multiple high-speed flip-flops (FF), a loop filter (generally an RC low-pass filter), a voltage-controlled oscillator (VCO), and an FF for data recovery. Even simple FF/latch topologies like TSPC and C²MOS require at least four transistors, and using two to three such FFs in addition to a minimum of four transistors for an LC-VCO exceed the 10-transistor limitation imposed by the contest rules. With a further bar on the use of inductors, a redesign of both the PD and VCO with novel techniques is required.

Here, we present a CDR consisting of only 10 transistors, one capacitor, and one resistor, while operating with a 1-V supply. Using a 20-Gb/s pseudorandom bit-source and a channel with 6.8-dB Nyquist-loss as the input, the circuit recovers a 20-GHz clock and regenerates the input bit pattern without errors, while consuming only 203 μW.

Proposed CDR

The block diagram of the proposed CDR architecture is depicted in Figure 1, which consists of a negative-feedback loop formed by the PD, the loop filter, and the VCO; and a clocked latch for regeneration of received data. To comply with the aggregate count of 10 transistors, each component is designed with a minimalist approach that seeks to utilize only the necessary devices for circuit operation.

The PD and loop filter (dashed box in Figure 1) are thus combined and realized as a compact switched-capacitor sample-and-hold circuit, where the capacitor serves both as a sampler and low-pass loop filter. The switch is realized with an NMOS transistor, with the gate terminal controlled by the binary data received from the channel. This PD topology is similar to that described in [2], and can be analyzed with the aid of the methods presented therein.

The schematic of the new VCO is shown in Figure 2(a), comprising two inverters capacitively coupled to form a ring oscillator (RO) configuration. An RO topology is adopted owing to the nonavailability of inductors. Conventional ROs are composed of ≥ 3 inverters, consequently requiring at least six transistors and thus making it difficult to limit the CDR transistor count to under 10. Hence, we employ a two-stage ring, and avoid the problem of latch-up in such a configuration by making the ring connection capacitive, while

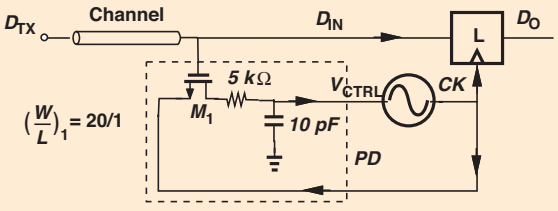

FIGURE 1: CDR block diagram.

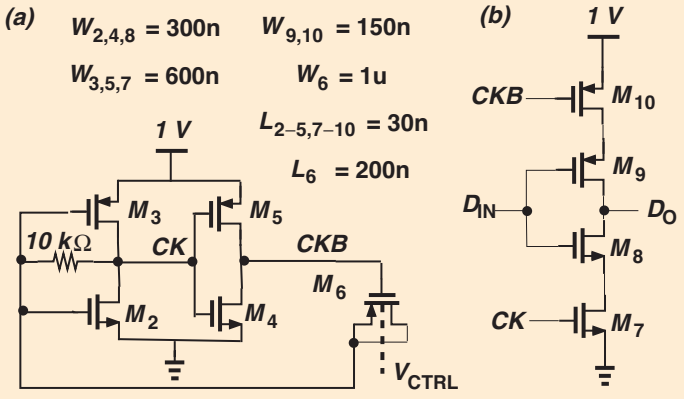

FIGURE 2: Schematic of the (a) VCO and (b) C²MOS latch.

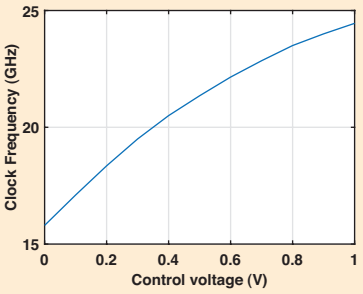

FIGURE 3: VCO output frequency variation with control voltage.

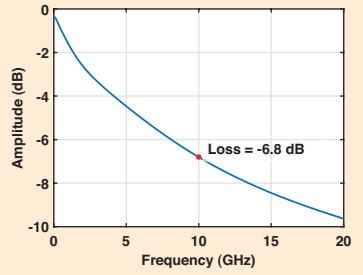

FIGURE 4: Channel loss with input frequency.

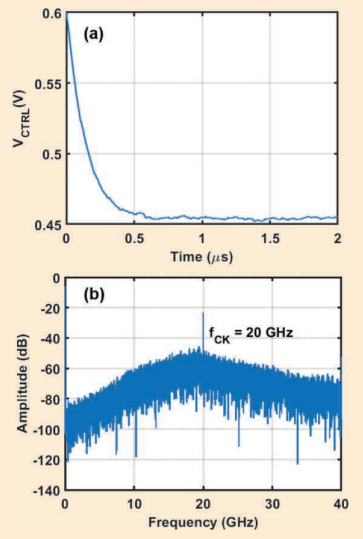

FIGURE 5: (a) Settling of the VCO control voltage and (b) recovered clock spectrum.

providing a well-defined dc operating point for the ring by self-biasing one of the stages. While the dc bias is set by the resistor-based negative feedback, the circuit becomes a high-gain positive-feedback loop at sufficiently high-frequencies. The oscillation frequency is determined by the pull-up and pull-down strengths of the inverters, as well as the relative values of the biasing resistor and coupling capacitor.

Since the contest rules allow the use of only one ideal capacitor, the coupling capacitor in the RO (M_6) is realized as a PMOS transistor with its source-drain terminals shorted together. We also propose a new method of frequency tuning, namely by adjusting the n-well voltage of M_6.

With the PD and VCO utilizing one and five transistors, respectively, the four remaining transistors are used to the design a C^{2}MOS latch for data recovery, whose schematic is shown in Figure 2(b). The two stages of the VCO provide complementary clock phases, thus supporting the latch operation.

As mentioned above, the oscillation frequency is made tunable by connecting the bulk terminal of M_6 with the VCO control voltage. As the oscillation frequency is strongly dependent on the coupling capacitance provided by M_6, this configuration yields a relatively wide tuning range, determined to be about 16 to 24 GHz from simulations (Figure 3).

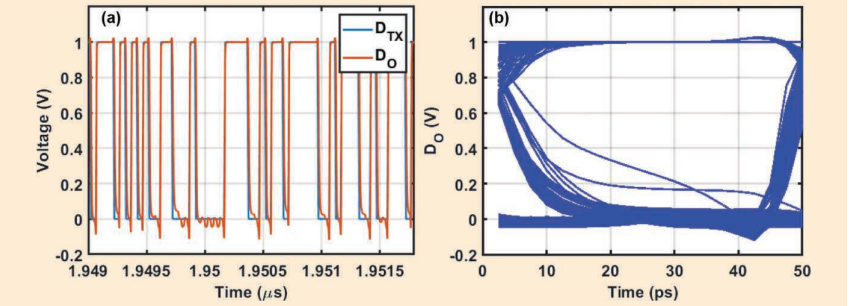

FIGURE 6: (a) Comparison of transmitted and recovered bits and (b) recovered data eye-diagram.

Simulation Results

Transistor-level simulations are performed to verify the operation of the circuit depicted in Figure 1. The input source is composed of an ideal 20-Gb/s NRZ pseudorandom bit sequence generator of bit-length 31 (PRBS-31) and a channel with 6.8-dB loss at the Nyquist frequency (10 GHz) (Figure 4).

Running a transient simulation, we see that the VCO control voltage starts with an initial condition and eventually settles to a steady-state value Figure 5(a). The steady-state value of this node leads to a recovered clock frequency of 20 GHz, which is confirmed by the recovered clock spectrum shown in Figure 5(b).

The locking of the VCO to the input-data ensures that the channel output is sampled at the optimal point and recovered without errors, which is confirmed by the comparison between the transmitted and recovered bit-patterns, as shown in Figure 6(a). The eye diagram of the recovered data is shown in Figure 6(b). All stages in the circuit operate dynamically, and the total average power consumption is determined to be 203 μW.

Conclusion

A CDR composed of only 10 transistors, one capacitor, one resistor, and a single 1-V supply is demonstrated. Simulation results indicate that the CDR can faithfully recover clock and data from a 6.8-dB loss channel at 20 Gb/s, while consuming only 203 μW.

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Matias Jara, Student, IEEE

A 10-Transistor 31.8-dB SNDR 208-kHz BW ADC

This submission presents a 10-transistor analog-to-digital converter (ADC) to participate in the 2022 SSCS Student Circuit Contest. The design is based on a delta modulator, and includes a novel amplifier with hysteresis. Simulation results show that the proposed implementation can convert a 208-kHz signal, achieving an SNDR of 31.8 dB with a power consumption of 126 μW.

Background

Since delta modulators [1] encode an analog signal to a sequence of digital pulses, they can be used as an oversampling ADC. A simple implementation is shown in Figure 1(a), where an integrator is replaced by a low-pass filter and a comparator acts as a one-bit quantizer. As is indicated in Figure 1(b), the comparator itself has a gain of A_0, and it adds a quantization error of Q. Then, the output V_{out} can be expressed as:

$$V_{out} = V_{in} A_0 \frac{1 + R_1 C_1 s}{1 + R_1 C_1 s + A_0} + Q \frac{1 + R_1 C_1 s}{1 + R_1 C_1 s + A_0} \quad (1)$$

Both the signal transfer function and the noise transfer function are depicted in Figure 1(c). At frequencies below $1/(2\pi R_1 C_1)$, the quantization error, Q, sees an attenuation of $1 + A_0$, while the input signal V_{in} only suffers a small loss equal to $A_0/(1 + A_0)$. This noise-shaping effect proves beneficial in an ADC, since the comparator's bang–bang characteristic introduces significant quantization errors.

From a design's perspective, a delta modulator only requires a comparator. A StrongARM latch [2] has a total of 11 transistors, while a double-tail latch [3] needs 12 transistors. Moreover, both circuits demand an RS latch to maintain the output value during the reset state, which adds at least four more transistors. Also, comparators must operate with a clock signal, which is not allowed in this contest. (Private communication with Prof. Liscidini.) These aspects introduce two challenges: first, the quantizer cannot be a typical implementation because of the large number of transistors, and second, the quantizer must include a self-oscillating mechanism to avoid generating a clock.

In this work, an ADC is presented using a delta modulator with a self-oscillating one-bit quantizer using TSMC's 28-nm CMOS technology. The entire design has only 10 transistors, one ideal current source, three resistors, and one capacitor, and it operates with a 1-V supply. It can convert a 208-kHz signal with an SNDR of 31.8 dB sampled at 800 MS/s, and with a power consumption of 126 μW.

Proposed Converter Architecture

The core of the proposed ADC is an amplifier with a self-oscillating mechanism that operates as a one-bit quantizer. In this section, the amplifier topology is presented along with how hysteresis is incorporated to generate a self-oscillation condition.

High-Gain Amplifier

As the quantization noise is attenuated by a factor of $1 + A_0$, a high-gain amplifier is desirable. Given the limitations of the number of

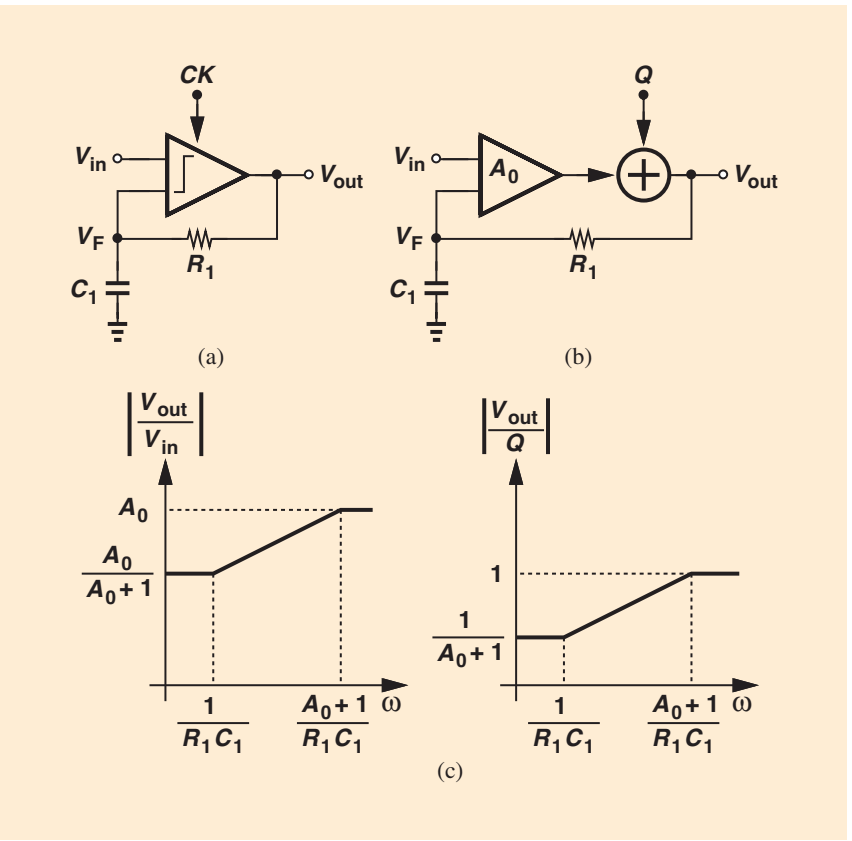

FIGURE 1: Delta modulator. (a) Simple circuit implementation. (b) Quantizer model. (c) Signal and noise transfer functions.

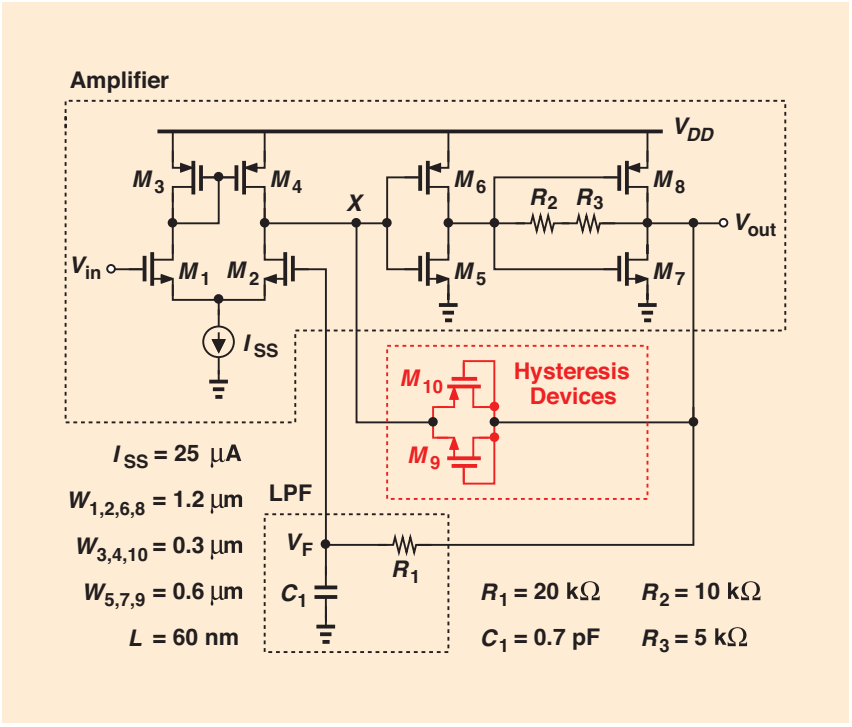

FIGURE 2: Circuit implementation of proposed converter.

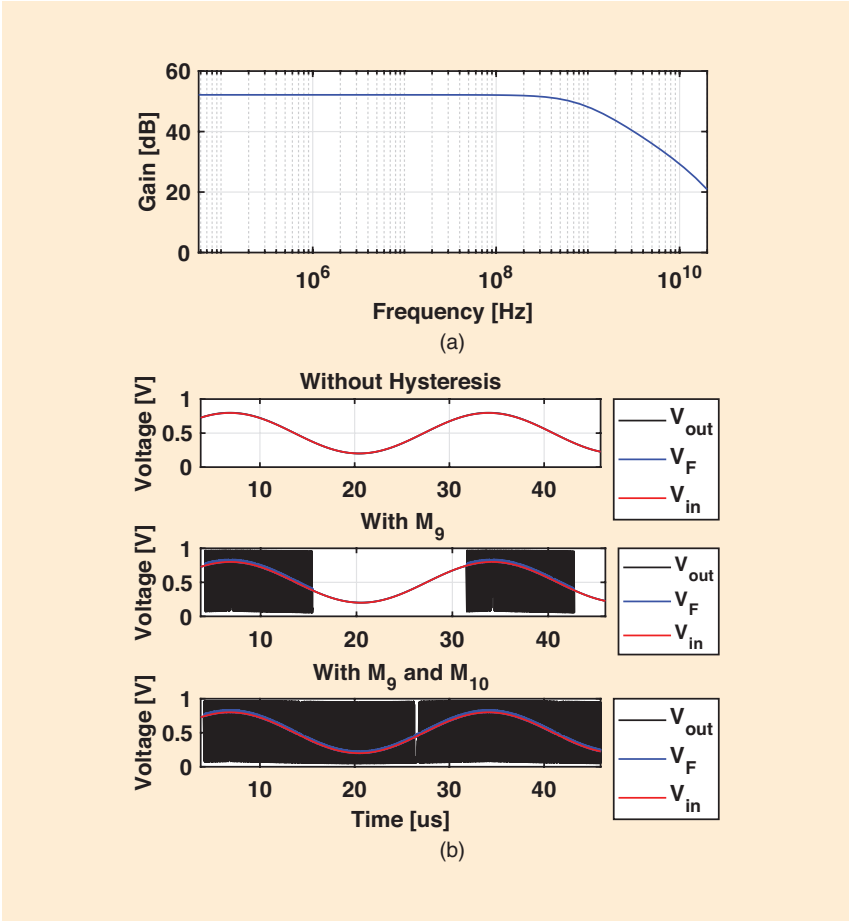

FIGURE 3: Cadence simulation results. (a) Frequency response of the amplifier. (b) Hysteresis mechanism in the amplifier.

components and bias conditions, the design is kept as simple as possible. Figure 2 shows the proposed ADC, including the implementation of a high-gain amplifier with three stages. Taking advantage of the ideal current source of 25 μA, a basic differential pair with single-ended output is used for the first stage. The second stage is an inverter acting as a gain stage. Finally, the third stage is a self-bias CMOS inverter. The self-bias property is necessary to ensure a defined input common mode around half V_{DD}. Even though this circuit is design using a 28-nm CMOS technology, the length for all transistors is doubled to boost the overall gain of the amplifier. Note that as only three resistors are available for the design, some can be used to bias the last stage, and one as part of the low-pass filter. As shown in Figure 3(a), devices dimensions have been chosen to guarantee a 52-dB gain.

Self-Oscillation Using Hysteresis

A conventional amplifier is not able to quantize an input voltage in a delta modulation loop. As the input signal is below the cutoff frequency of the R_1C_1 filter, the entire stage would act as a buffer. It is therefore necessary to include a hysteresis mechanism in the amplifier to generate a self-oscillating condition that translates into binary pulses at the output. This is possible with the aid of transistors M_9, and M_{10} of Figure 2. Figure 3(b) shows three scenarios: a conventional amplifier, one with M_9 only, and one with M_9 plus M_{10}. When V_{out} is close to V_{DD}, M_9 turns on, drawing current from node X, then V_F needs to increase to compensate this disturbance. By the time the amplifier sets a new operation point, V_{out} will go to zero, turning off M_9; consequently V_F ramps down to return the amplifier to its initial state. By turning on and off M_9, an oscillating condition is produced, processing the input as a typical delta modulator. To guarantee this condition for the entire

input swing, a PMOS transistor (M_{10}) is included as well.

Simulation Results

The design of the proposed ADC is shown in Figure 2. The value of $C_1 = 0.7$ pF is selected to attenuate the quantization noise for frequencies below 10 MHz, and to have an output rate of 800 MS/s. Figure 4(a) shows the waveforms for a transient simulation on different sections of an input sine wave. It is clear how the digital output corresponds to a modulated version of the input. The input swing of the signal is kept to 600 mV_{pp} to limit the harmonic levels under the quantization noise. Figure 4(b) shows the output spectrum of V_{out} sampled at 800 MS/s for a 208-kHz input signal. From these results, the SNDR of the converter is 31.8 dB, corresponding to an ENOB of 4.99. (As an oversampled ADC, the SNDR is calculated up to f_{in}.) The total power consumption is 126 μW.

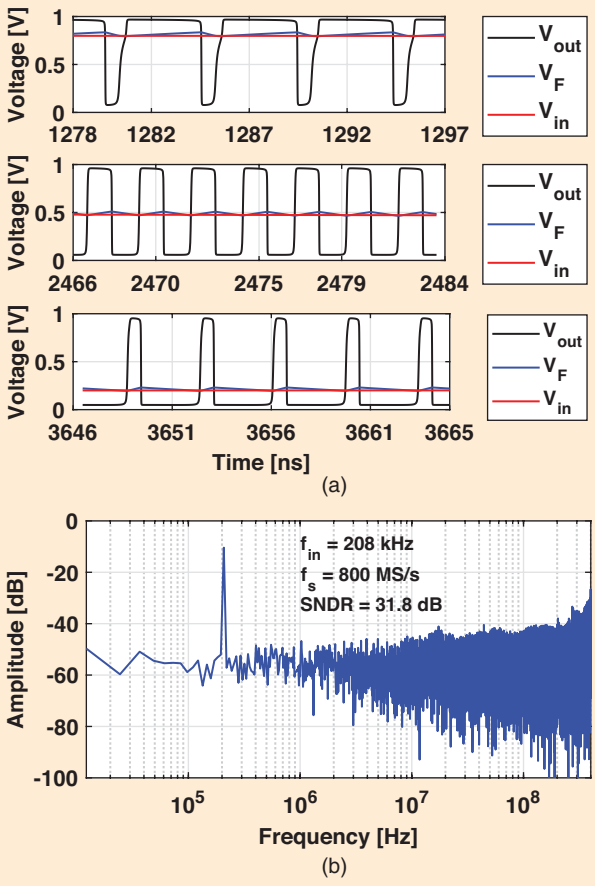

FIGURE 4: Cadence simulation results for a 208-kHz input sine wave. (a) Modulation for different sections. (b) Output spectrum obtained with a sampling rate of 800 MS/s.

Conclusion

An ADC is proposed in 28-nm CMOS technology, that uses all the components given in the contest's list: 10 transistors, three resistors, one capacitor, one ideal current source, one 1-V supply, and one ideal input voltage source. The converter operates at 800 MS/s and can convert a 208-kHz signal, achieving an SNDR of 31.8 dB with a power consumption of 126 μW.

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A Spark of Philanthropy to Inspire Future Generations

Dr. T.J. Rodgers' contribution to support the IEEE Solid-State Circuits Society James D. Meindl Memorial Educational Fund was driven by both his respect for his mentor, Prof. James D. Meindl, and his business savvy and understanding of endowing funds for the next generation.

"Managing money for future generations has a lot in common with managing a business. When I ran Cypress Semiconductor, I was expected to make money for shareholders, and have profit left over to reinvest in the next generation of technology. The goal of endowments is to pick and manage

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