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Nanoelectronics Research Gaps and Recommendations

A Report from the International Planning Working Group on Nanoelectronics (IPWGN)

Nanotechnology exploded in scientific publications in the year 2000. It became clear in the subsequent years that the magnitude and opportunities offered in nanotechnology research and development exceeded the research capabilities of any single entity or any single region, and a new cooperative approach was needed. The first step to this approach consisted of fostering communication among leading researchers with the intent of facilitating subsequent cooperation. As such and as applicable to semiconductors and nanoelectronics, international cooperation and research coordination was instigated via the International Nanotechnology Conference on Communication and Cooperation (INC) initiative, leading the quest to narrow "research to a new product cycle" via a coordinated research strategy and funding initiatives towards solving the grand challenges. The INC conference series first began in 2005 to serve as a central arena for stakeholders to share experiences from various regions on electronics-related nanotechnology research program execution and challenges.

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IPWGN Mission

Supported by both the International Technology Roadmap for Semiconductors (ITRS) Emerging Research Devices chapter (ITRS/ERD) and the INC, the International Planning Working Group on Nanoelectronics (IPWGN) was established to identify technology research funding and program gaps occurring in regions. The goal was to reduce overlaps and to programmatically improve research program planning. Such information allows for recommendations to adjust and justify resource allocation and to encourage interregional research collaboration, particularly where underfunded opportunities may exist, in order to maximize social and economic benefits derived from the funded research. The technical areas of IPWGN focus are aligned with the ITRS/ERD and ITRS/ERM targeting "extended CMOS" including "beyond CMOS" that includes all new approaches proposed to scale some functional performance for

Digital Object Identifier 10.1109/MTS.2015.2425811
Date of publication: 19 June 2015

information processing beyond that attainable by scaled CMOS. Such alternatives are numerous and best documented and catalogued by the ITRS [1], [2] and associated publications [3]–[5]. Since the inception of the INC conference series, the IPWGN working group has been chartered to collect information on research programs, identify gaps, and stimulate international collaboration. Understanding the scope, identifying programs and frameworks, and then rendering useful conclusions is the primary task of the IPWGN [6], and as such, in the effort to disseminate this information, this article aims to synthesize the learning, outcomes, and conclusions from IPWGN activities.

IPWGN Methodology

Our first step begins by identifying potential research gaps via composing a framework of comparison and tabulation based on important nanoelectronics research guiding principles. For our task, we have employed the original guiding principles (research vectors) used by ITRS/ERD and adopted by INC and IPWGN in 2010 [6]. These include:

1) Computational state variables other than electron charge [7].
2) Non-equilibrium systems [8].
3) Novel energy transfer interactions [9].
4) Nanoscale thermal management [10].
5) Beyond lithographic manufacturing processes [11].
6) Alternative architectures [12].

To complement the focus on a digital switch, we have also included the notion of memory device requirements (and those emerging ideas) [13], more generally termed here as "storage." Furthermore, we have embraced and further refined [14] the concept of More-than-Moore (MtM) as initially proposed by Europe and first introduced in the 2005 ITRS roadmap. The "More-than-Moore" approach allows for the non-digital functionalities (e.g., RF communication, passive, MEMS) to migrate from the system board level into the System in Package (SiP) or onto the System on Chip (SoC) [15], [16]. Figure 1 presents the relationship between these various concepts.

Based on the IPWGN committee agreement, our technical framework for evaluating the most relevant challenges have been categorized as follows:

1) Computation and Storage
   a) 0D/1D/2D charge based extended CMOS devices [17] [18]
   b) Computational state variable other than solely electron charge [19]
   c) Non-equilibrium computation [20]
   d) Information Transfer [21]
   e) Thermal Management [22]
   f) Manufacturing [23]
   g) Architectures [24] [5]
2) More-than-Moore (MtM)
   a) Materials and Devices [14]
   b) Manufacturing Techniques [25]
   c) Architecture [26]

Once our technical domain areas were defined, we then nominated regional IPWGN chairs to solicit data inputs. These chairs, along with selected colleagues from government and the private sectors who have their "thumb on the pulse," convened and objectively gauged how research efforts are reflected with respect to our defined technical framework, allowing for inter-region data normalization. For adequate granularity, it was decided to select R&D programs with a minimum funding threshold of $1M. Data was also limited to funding INC regions that were actively engaged in the IPWGN committee. Representation included members from the U.S.A., Europe, and Japan. Analysis from other regions such as Taiwan, China, and South Korea were not included. Absolute funding numbers were not accounted for given that public and government agencies do not publish funding information that corroborate

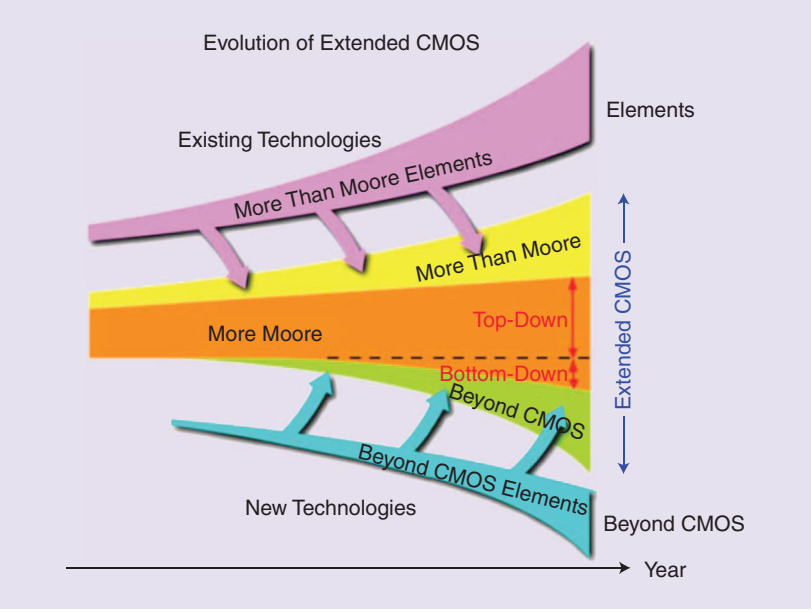

FIGURE 1. The ITRS illustration showing the relationship of concepts in the evolution of extended CMOS. This graph clarifies the relationship between terminologies such as More than Moore, More Moore, and Beyond CMOS. (Used with permission from ITRS ERD.)

with our defined research vectors. The outcome of this analysis yields a bar graph analysis that serves the purpose of regional research vector comparison, and further, can be used to provide a subjective global regional comparison (Figures 4–6). Arbitrary units and patterns are used for comparison. As such, information such as underfunded research areas where re-allocations of resources to "close the gap" may be possible. In addition, over time, key questions that could be answered include "Was funding spent well?," "Did funding lead to breakthroughs?" and "Has the grand challenge been overcome?"

United States Region

Overview of Nanoelectronics Programs in the United States

In the United States, many public-private nanoelectronic initiatives are administered by the Semiconductor Research Corporation (SRC) with funding to over 2300 researchers in 2013. The SRC coordinates primary programs such as the STARNET (previously known as the Focus Center Research Program (FCRP)). The SRC also administers the Nanoelectronics Research Initiative (NRI) cofounded by SRC industry members, NSF, and NIST. The STARnet program has a broader mission compared to the NRI, in that it aims to create breakthroughs that are critical to U.S. security and economic competitiveness goals with member companies from both the defense and semiconductor industries. The STARnet program has six Centers of Excellence, of which three are relevant to nanoelectronics. The NRI has a more focused mission to demonstrate non-conventional, low-energy technologies that can outperform CMOS on critical applications in ten years and beyond. In addition a multitude of NSF programs (labeled NRI-NSF) are reviewed under the NRI umbrella.

The NSF itself has also been instrumental and very active from the very beginning in supporting nanoelectronics research [27]–[29]. The most predominant has been through the National Nanotechnology Initiative (NNI) [30]. Furthermore, the NSF has been active in established Centers of Excellence such as the Nanoscale Science and Engineering Centers (NSEC) [28], [31], Material Research Science and Engineering Centers (MRSEC) [32], [33], Engineering Research Centers (ERC) [34], and Science and Technology Centers (STC). In addition, together with NRI, the NSF spearheaded the program "Nanoelectronics Beyond 2020." Other significant initiatives that have come online in 2014 that direct more funds to nanoelectronics research are the National Network for Manufacturing Innovation (NNMI) [35], more generally known as the "Obama Manufacturing Hubs." It should also be mentioned that state infrastructure funding to enhance regional nanoelectronics capabilities has also played key roles in nanoelectroncs R&D such as the SUNY's College of Nanoscale Science and Engineering (CNSE), California Nanosystems Institutes, and the Texas Emerging Technology Fund. Other outlier initiatives such as the National Institute of Standards and Technology (NIST) Infrastructure fund is slowly but surely adding crucial resources to the U.S. nanoelectronic landscape.

United States Gap Analysis

The gap analysis of the U.S. shows that areas such as devices, materials, and architectures are well funded. The most underfunded areas are exotic non-equilibrium concepts followed by thermal management. Similar results were evident in the 2010 IPWGN report and prior years [6]. However, it should be pointed out that this may be a shortcoming of semantics. For instance, spintronic based devices have seen a rapid increase in funding, publication numbers, and patents. Many concepts employing spin requires non-equilibrium conditions to incur switching as highlighted in [8].

A similar situation seems to be occurring for thermal management. In spite of its importance, no Center of Excellence funded by the United States focuses solely on this topic, or even makes it a distinguished theme.

One recommendation was to bridge the "Valley of Death," the gap between science and research on the one hand and industrial dissemination in the market on the other.

One obvious area of improvement has been "manufacturing." With funding of NSEC manufacturing centers [35] and the notion of "manufacturability," Si compatibility and new nanomanufacturing methods are required to alleviate traditional photolithography costs. A unique example of manufacturing funding can be cited as that of the CNSE facility where researchers with industrial manufacturing pilot lines are able to test concepts and produce test devices at 300-mm wafer levels. New initiatives are championed by the CNSE on a regular basis.

In addition, the U.S. region offers some prime examples of

long lasting programs that link private industry and government and university stakeholders in a collaborative long-term R&D funding paradigm. It has played out to be a win-win situation particularly on the front of private-public partnerships creating desirable and noticeable return on investment (ROI), as a generation of hard assets (intellectual property) and soft assets (training students and workforce on relevant challenges for industry readiness) all towards fulfilling the original grand challenge. One citable example is the creation of the Focus Center Research Program in 1999 (which today is known as the STARnet program [36]) which over the course of its inception has been partly funded by the U.S. semiconductor industry and U.S. DoD, and has been administered by the Semiconductor Research Corporation.

Clear solutions are yet to be found for issues related to personal freedom, privacy, and identify theft.

European Region

Overview of Nanoelectronics Programs in Europe

In Europe, research and innovation programs are the responsibility of the individual member states and numerous funding opportunities for research projects exist at European, member state, and regional levels. During the past several years, nanoelectronics research in Europe was influenced by cautious funding in Germany. A strong effort from the French Government with concentration of many nanoelectronics activities in the Grenoble area, and with Belgian/Flemish and Dutch efforts to stay in tune with the international development of technology, equipment, and materials. Emphasis on enhanced manufacturing-oriented R&D has occurred, with examples such as U.S. based companies having European manufacturing sites (Intel Ireland, Intel Israel, AMD/GlobalFoundries Dresden) and existing fabricators exploiting emerging areas around "More-than-Moore" technologies.

In 2010, Europe defined key enabling technologies (KETs) as the basis for increasing industrial competiveness. KETs include nanotechnology, advanced materials, photonics, biotechnology, advanced manufacturing and micro-/nanoelectronics [37]. One recommendation was to bridge the "Valley of Death," the gap between science and research on the one hand and industrial dissemination in the market on the other, as shown in Figure 2. This recommendation served as a major input for the new framework program for research and innovation, "Horizon 2020" [38].

In 2012, a European research cluster in nanoelectronics, targeting bi-lateral and multi-lateral cooperation between various Member States - the EUREKA cluster CATRENE - and the European Industry Association for micro-and nanoelectronics – AENEAS - identified major European industrial interest areas [39]. As a consequence, the European Commission adopted a strategy of doubling European chip production by 2020 and Commissioner Neelie Kroes set up an Electronics Leaders Group (ELG) to come up with a strategic plan [40]. Following the strategic plan, first implementation actions were taken during 2013 under the 7th Framework for Research and Innovation in the Joint Undertaking (JU) ENIAC, a 5 B€ public-private partnership between the European Commission, European Member States and Industry. In parallel, another JU Advanced Research & Technology for Embedded Intelligence and Systems (ARTEMIS) at 3+B€ aims to implement a coherent research agenda for embedded computing systems.

Also two big flagship projects have been approved to date under the 7th Framework and will continue under the new framework program "Horizon 2020" [38]. The first is the Graphene Flagship (www.graphene-flagship.eu) and the second the Human Brain Project (www.human-brainproject.eu), each of them funded by 1 B€ over the next 10 years.

Beginning in 2014, the new framework program "Horizon 2020" (H2020) covering the period 2014–2020 started delivering activities and funding opportunities. This 70+B€ program targets 6.6 B€ funding for KETs and 7.5 B€ for ICT. The program also includes the participation of the European Commission in a new public private partnership, the 5 B€ Joint Undertaking "ECSEL" combining both the JUs ENIAC and ARTEMIS, the technology platform EPoSS, their member states, and their industry associations under one umbrella. The new JU is covering research and innovation from nanoelectronics technology and components up to cyber-physical systems and related applications. The micro- and nanoelectronics research and innovation activities in H2020, planned to be executed in the JU ECSEL, include areas of opportunity for high demand growth [40] such as 1) areas of above average growth

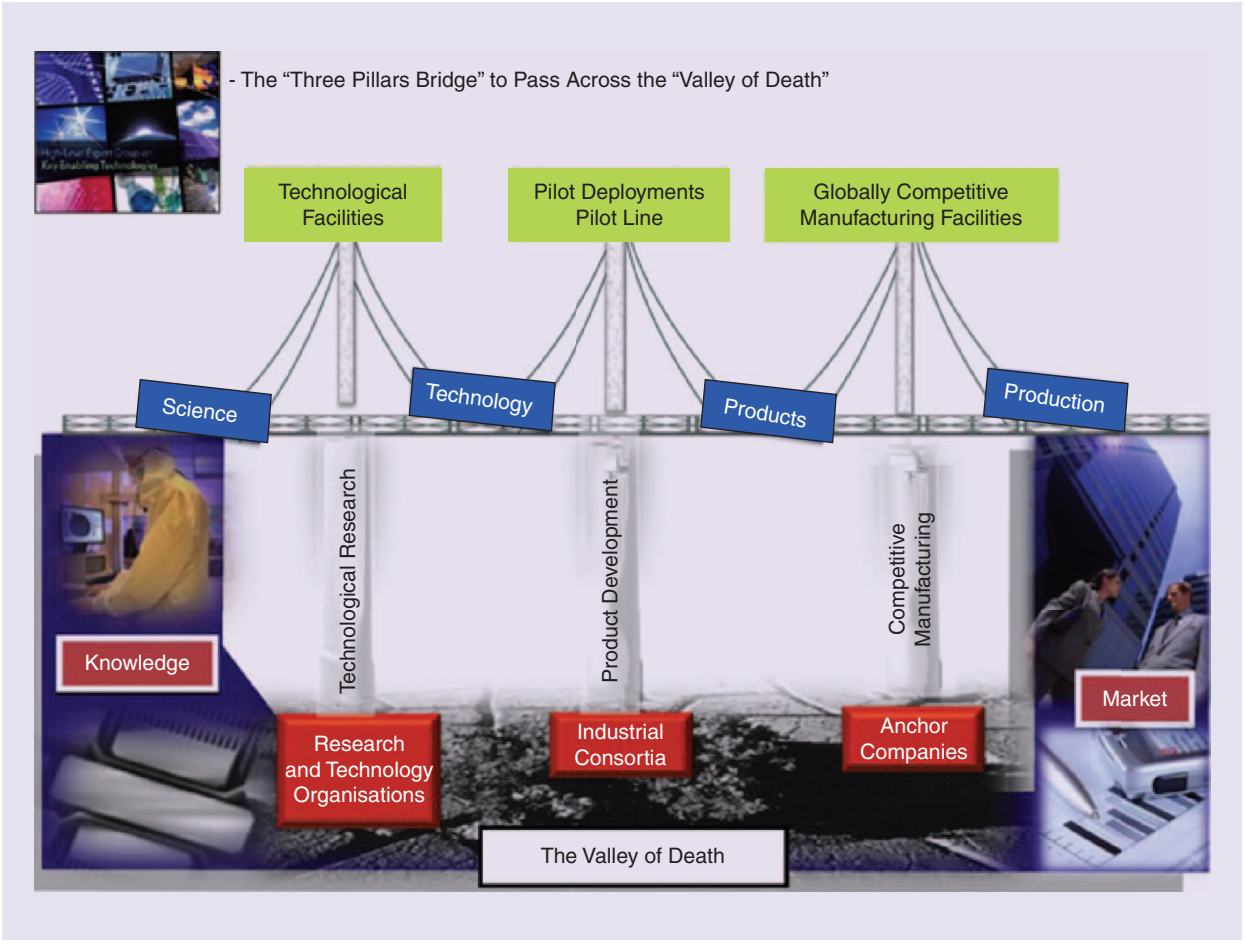

FIGURE 2 A European integrated initiative to bridge the KETs "Valley of Death."

(automotive, energy, industrial automation and security), 2) new high growth areas such as the "Internet of Things" (IoT), and 3) mobile convergence to maintain leadership in the design of low-power processors and leading-edge semiconductor manufacturing.

European Gap Analysis

The injection of direct funding to spur micro- and nanoelectronics R&D in Europe has gained much momentum and aligned with the efforts of INC, ITRS and the IPWGN. In addition, three big European research and technology organizations (RTOs) that involve IMEC, LETI, and Fraunhofer, have agreed to support the major industrial areas of interest in line with their competencies such as a) next-generation equipment and materials, b) enhancement of state-of-the-art manufacturing technologies, and c) functional diversification. As part of this effort, the EU team has participated in the IPWGN and activities covering the different research vectors.

In general, funding in Europe is application-oriented. Thus, technology research is strongly influenced by this strategy and funding of technology research is often "hidden" behind applications. However, a gap analysis of nanoelectronic research shows similar strength and weakness in various research vectors compared to the U.S. and Japan. The most underfunded area is "out of equilibrium" research, and the most funded areas are "materials and devices." Over time, the trend in Europe has been towards increased funding in previously underfunded areas such as manufacturing of MtM, which is a reflection of the pragmatic European approach to manufacturing since the inception of this survey group. Other areas such as the graphene and brain related projects have greatly increased in relative funding strength.

The Japan Region

Overview of Nanoelectronics Programs in Japan

Nanoelectronics research vectors in Japan are well funded by many government organizations

including the Ministry of Education, Culture, Sports, Science, and Technology (MEXT), the Japan Society for the Promotion of Science (JSPS), the Japan Science and Technology Agency (JST), the Ministry of Economy, Trade, and Industry MITI), and the New Energy and Industrial Technology Development Organization (NEDO).

In 2009, The Council for Science and Technology Policy (CSTP), Cabinet Office, Government of Japan announced the "Funding Program for World-Leading Innovative R&D on Science and Technology: FIRST" program. The program included projects in spintronics, green nano electronics, electron/photon fusion for optical interconnection, and heterogenous integrations for more than Moore technology. These FIRST programs were concluded in 2014.

For low power electronics, a research association called "Low Power Electronics Association & Project: LEAP" started in 2010 supported by NEDO and MITI. The main topics of this project are MTJ for non-volatile memory, phase change memory, atomic switch for FPGA, carbon based interconnection, and nano scale transistors.

Another national driver is the need for new photoresistance to handle extreme ultraviolet (EUV) light. For resistant materials development, the EUVL Infrastructure Development Center (EIDEC) was organized in 2010, supported by NEDO and METI. This program involved EUV mask inspection, gas protection from photo resistance, resistant materials development, and direct self assembly of resistant polymers. Indeed, nano scale lithography and fine pattering are not the only solutions for future electronics. Therefore, in parallel, "post scaling" has been discussed and some other ideas are proposed with heterogeneous integration [41].

These four FIRST programs, LEAP and EIDEC programs were operated mainly in the National Institute of Advanced Industrial Science and Technology (AIST) West Campus, and some of them are related to the Tsukuba Innovation Arena (TIA-Nano) research network.

Another funding agency, JST is an independent public body of MEXT. The JST had been supporting the Core Research for Evolutional Science and Technology (CREST) program, which is a five year project focusing on topics proposed by a program manager. Since 2005, a CREST program entitled "Research of Innovation Materials and Process for Creating Next Generation Electronic Devices" began and drove much innovation.

In 2013, the JST launched another CREST program, Innovative Nano-Electronics through Interdisciplinary Collaboration among Material, Device, and System Layers. The areas are related to tunneling FET, sensing devices with Si nano wire, and image sensors for spin mapping. The projects are expected to lead innovative information processing and electronics to contribute to high impact societal needs such as smart houses, traffic, next-generation automobiles, robots, and human interfaces. IPWGN Japan members believe it is absolutely imperative to bridge the gap between nanoelectronics and the business model of the semiconductor industries. This challenge is highlighted in Figure 3.

Of key importance to the Japan approach has been MEXT. MEXT has been instrumental from the very beginning in constructing a user-facility network in Japan, which is similar to the U.S. NNIN program. The integrated partnership of user facilities, "Nanotechnology Support Program," started in 2002, followed by the "Nanotechnology Network Program" started in 2007. The newly launched "Nanotechnology Platform (2012–2021)" is a nationwide user facilities platform covering three technological areas of "advanced characterization," "nanofabrication," and "molecule and material synthesis."

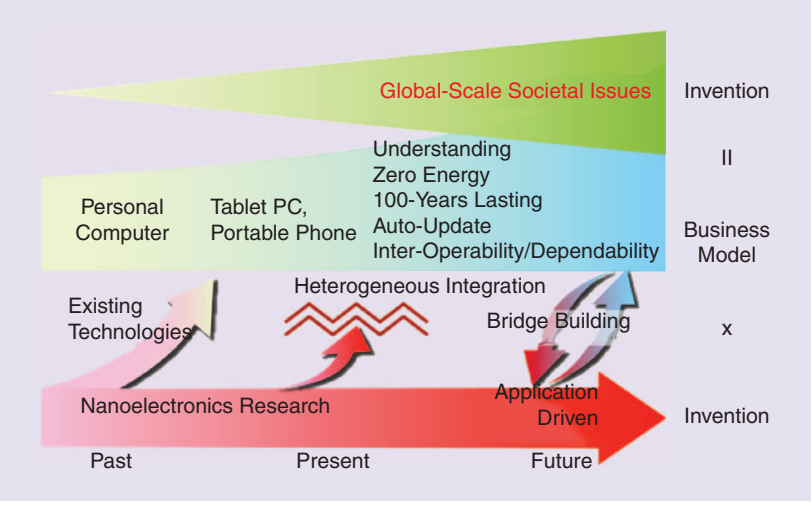

FIGURE 3 Bridge building between nanoelectronics and the business model of semiconductor industries (with permission from Naoki Yokoyama, INC10).

Japan Gap Analysis

Looking at the Japan gap analysis, the more-than-Moore architecture, 0D/1D/2D, and state variables seem to be well funded in Japan. Actually, many programs deal with MEMS sensors, circuit/

system architecture for normally-off computing, nanocarbon, and spintronics, enhancing the activities in these areas in Japan. Compared with topical maps in prior years, funding of MtM is increasing and funding in architecture and state variables remain high. Although funding on manufacturing and 0D/1D/2D seem to be decreasing (on a relative basis), they still remain high. On the other hand, the underfunded areas include out of equilibrium, information transfer, and thermal management. Some programs on spintronics are also related to the non-equilibrium nature of spin, but as already mentioned, the categorization may have to best captured this effort.

In reviewing yearly trends, it seems Japan has made efforts to bolster funding in strategic areas such as MtM, architecture, manufacturing, and materials and devices. Other areas that have not reflected a relative increase, and are presumed to be underfunded, include out of equilibrium, information transfer, and thermal management.

Social Implications and Recommendations

It is well known and documented that the semiconductor industry is credited for major innovations, impacting modern social life and economies, so much so, that in the U.S., from 1960–2007 the industry accounted for 30.3 percent of all economic growth due to innovation (42). The innovation and progress of the semiconductor industry has had a dramatic impact on everyday consumer electronics, businesses, and industries that have been transformed by information technology. For instance, modern factories employ robots and computers to do much work, and United Airlines employs supercomputers like IBM's Deep Blue to analyze and determine the most efficient flight path combinations, and not to mention, many companies pivoting into new markets and digital product offerings. Think of Amazon.com being the world's largest book selling company, now also leading the digital consumption market of digital reading on Kindle and personal devices.

However, the social story is not just a rosy one. There are challenging and contentious social issues resulting from rapid innovation and growth in technology. Think of your old devices and processors that become outdated that then become "e-waste." They often end up in China, South Asia, or certain parts of Africa. Other challenges include job losses resulting directly from human tasks being replaced by computers and automated systems. More recently, issues such as personal freedom, privacy, and centralized "cloud" storage and identify theft are issues where clear solutions are yet to be found (43).

Another challenge faced by the industry itself that may have broader market ramifications is ever-increasing fabricator costs, resulting in the semiconductor industry moving towards an oligopoly, where only a few silicon device manufactures survive, allowing for control and manipulation of market prices. State-of-the art fabricators cost $10 billion or more resulting in few companies capable of financing next-generation

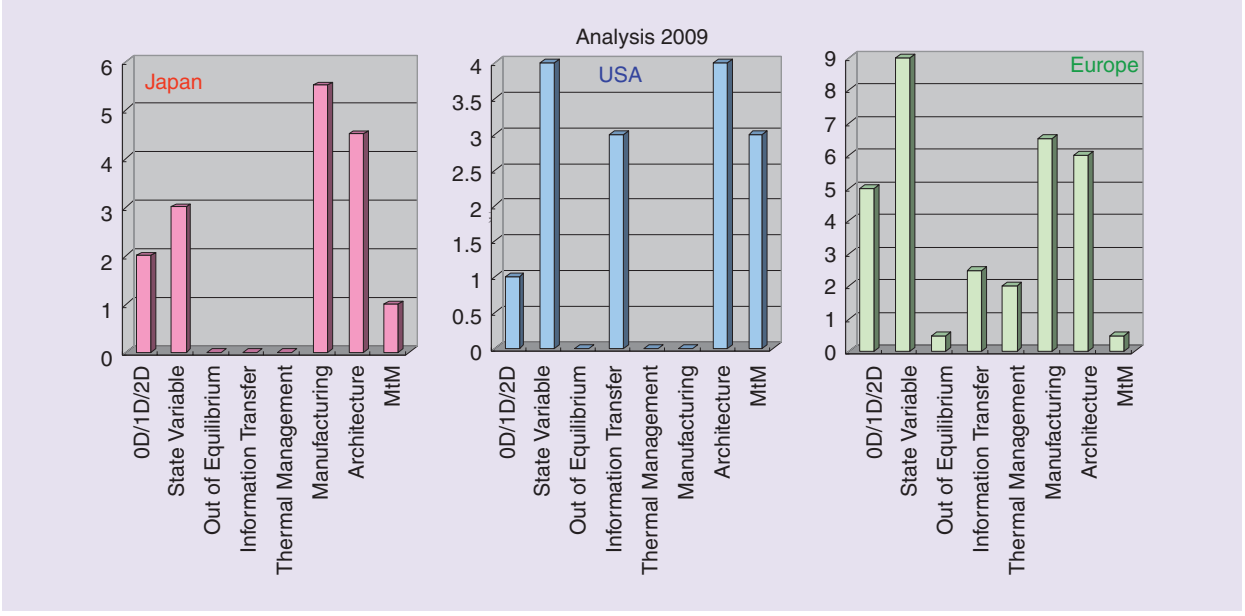

FIGURE 4 Summary of 2009 IPWGN survey results.

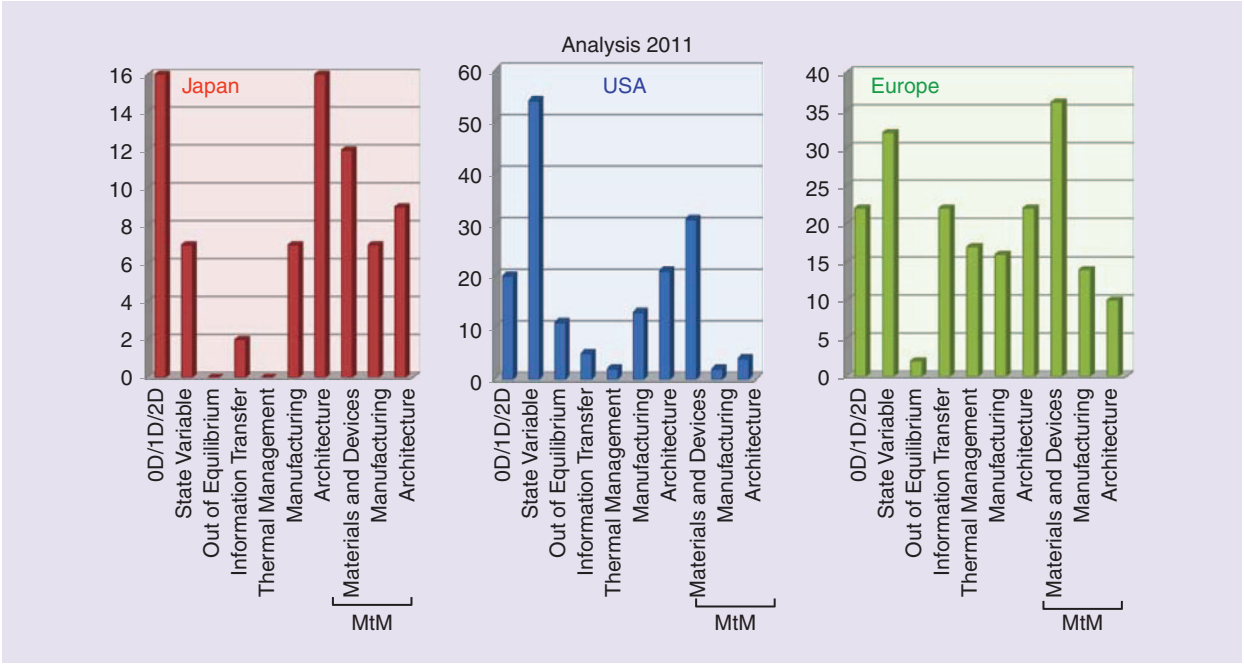

FIGURE 5 Summary of 2011 IPWGN survey results.

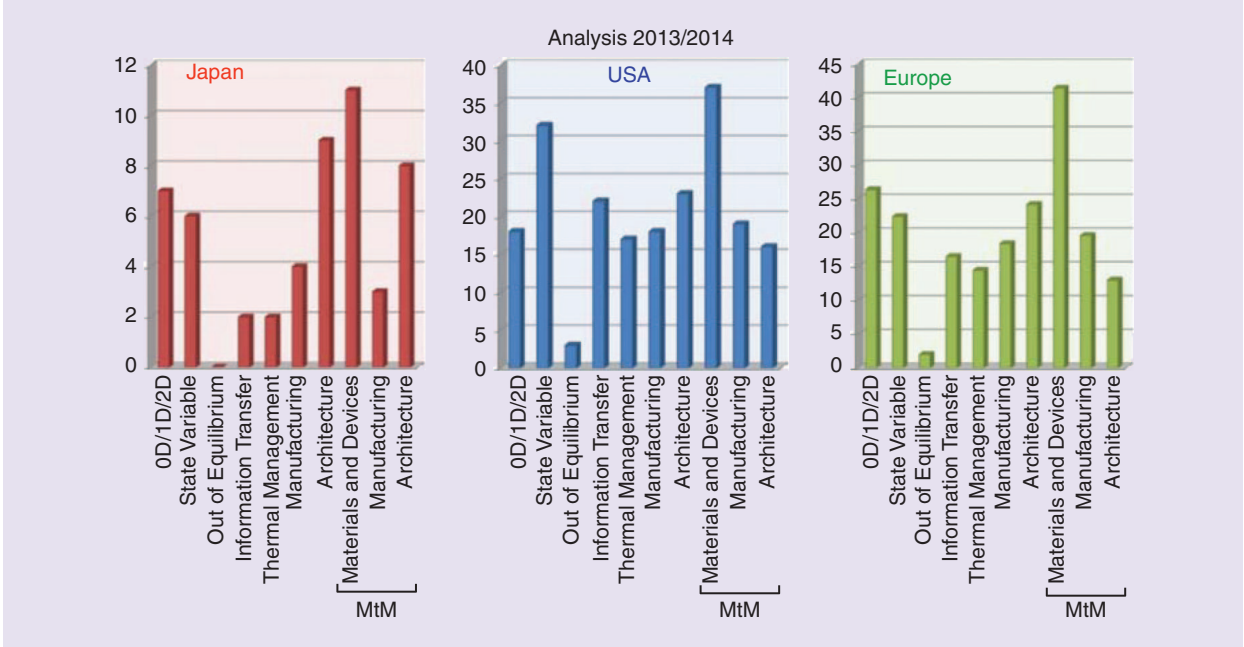

FIGURE 6 Summary of 2013 and 2014 IPWGN survey results.

nodes and fabricators. While Moore's Law continues, there are sign of it slowing down due to fundamental physical and quantum limits being reached (44). The point of diminishing returns will eventually catch both sides of the equation, resulting in a slowdown in technology innovation as a result of insurmounting fabricator costs (45). As such, a real world effort to discover new technologies and fabricator methods is being pursued, amounting to rigorous R&D public and private funding programs to solve the technological challenges

the semiconductor industry is currently facing.

The urge to maintain the innovation rate of progress that sustains the semiconductor industry is one of the prime objectives in ensuring R&D efforts continue to provide necessary enhancements and innovations. Hence the existence of the INC and IPWGN, where the objective in this study is to document funding allocation effectiveness per a well defined technical framework, "research vectors," and to answer numerous questions such as: "Was funding spent well?," "Have research gaps been fixed?," "How do global funding profiles compare?,","Has the mission been accomplished?"

Data gathering began in 2006. An early analysis of the landscape is shown in Figure 4, where major gaps (underfunding) can be seen in several research vectors. This was the first such side-by-side comparison of funding intensity at a global scale in the area of nanoscience, nanotechnology and nanoelectronics. This first insight began a movement of internal regional discussions that stimulated the initiation of programs (and redirected many existing programs) in each region to reduce such research vector omission. Hence, by 2010, the number and the relative magnitude of the gaps was substantially reduced, as shown in Figures 4 through 6. This "filling of the gaps" continued.

A key observation is the regional agreement of the most funded technical areas. For instance, all regions continue to present "non-equilibrium" as the most underfunded area, while areas such as materials/devices and 0D/1D/2D materials are most funded. After nearly a decade of data collection, one could conclude that all regions agree that the areas of opportunity to overcome the grand challenges remain as the "most funded" areas and least opportunity with the "underfunded" areas. Furthermore, this uncanny resemblance of alignment in each region is also a reflection of the international agreement and influence that has occurred within the INC, IPWGN, and ITRS. As such, not only have these efforts allowed us to track relative funding/opportunity, but they have also been used as a feedback mechanism in determining top-down R&D funding effectiveness.

In summary, the IPWGN meetings have largely contributed to filling and reducing most of the gaps in the research agenda when considering the combined efforts of all the regions. Together with disseminating this information, the IPWGN continues to scan and coordinate efforts among global regions to ensure effective funding mechanisms towards solving our grand challenges, to maximize effectiveness on a global scale.

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Acknowledgment

The authors thank all International Planning Working Group on Nanoelectronics (IPWGN) members. IPWGN U.S. members include Paolo Gargini, Barbara Goldstein, David Seiler, Yumiko Takamori, Kosmas Galatsis, and Phil Lippel. IPWGN Europe members include David Guedj, Roger De Keersmaecker, Adrian Ionescu, Joachim Pelka, Lothar Pfitzner, Serge Tedesco, and Renzo Tomellini. IPWGN Japan members include Hiroyuki Akinaga, Toyohiro Chikyow, Noburu Fukushima, Toshiro Hiramoto, Shintaro Sato, and Ken Uchida. In addition, we would like to acknowledge the support and contributions of the International Nanotechnology Conference on Communication and Cooperation (INC) conference series Executive, Program, and Organizing Committee members.

U.S. INC members include Paolo Gargini, Gernot Pomrenke, Mihail Roco, David Seiler, Kosmas Galatsis, Kang L Wang, Yumiko Takamori, Ian Steff, Tom Theis, Robert Doering, and Barbara Goldstein.

Europe INC members include Laurent Malier, Dirk Beernaert, Gilbert Declerck, Hubert Lakner, Renzo Tomellini, Marcel Annegarn, Dominique Thomas, Livio Baldi, Heico Frima, Roger De Keersmaecker, Serge Tedesco, Norbert Lehner, Fred van Roosmalen, Joachim Pelka, David Guedj, Jörg Stephan, and Jo De Boeck.

Japan INC members include Teruo Kishi, Hideyuki Yamagishi, Tsutomu Handa, Toshihiko Kanayama, Junichi Sone, Naofumi Moriya, Toshio Baba, Toshiro Hiramoto, Yasuhiro Tokura, Michitaka Kubota, Ryosho Kuwae, Hiroyuki Akinaga, Satoshi Tochiori, Ichiro Hirata, Shigemitsu Kusuda, Hiroshi Iwata, Takahiro Shinada, Toyohiro Chikyo, and Katsumi Suzuki.

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