Guest Editorial
Special Section on Physical Design Techniques for Advanced Technology Nodes

Advanced technology nodes have engendered new challenges in the design of integrated circuits (ICs), which can only be addressed through innovations in physical design techniques and algorithms. These challenges stem from factors such as increasingly complex manufacturing design rules, cell pin access in technologies utilizing multiple patterning and FinFETs, various types of restrictions and blockages on the routing layers, and complexity of the physical floorplan, for example due to irregular shapes of placeable areas.

Examples of physical design algorithms which need to be revised or completely redesigned to account for the above factors include place and route algorithms to address the routability challenge, and interconnect timing and power optimization techniques in light of significant restrictions on how routing resources may be used. Physical design algorithms may further need to be redesigned to address these challenges in emerging technologies such as 3-D ICs.

This issue and the next issue feature the special section on physical design aimed at addressing these challenges.

Four papers focus on place and route techniques, which target manufacturability in advanced technology nodes. These include detailed placement and routing optimization techniques for double, triple, and quadruple patterning lithography.

Three papers address physical design techniques to improve pin access and routability. These include standard cell optimization technique to improve pin access for double patterning technology, and global routing procedure to evaluate routability, taking into account the significant variation in wire size and spacing across the metal layers.

Three papers focus on timing and power optimization in view of the advanced technology challenges. These works address clock network analysis and optimization in the presence of significant manufacturing variations, as well as physical design solutions for power-gated design domain.

Finally, the remaining papers address challenges of advanced technology nodes for emerging technologies. These include partitioning techniques to reduce congestion in 3-D monolithic ICs, placement techniques to improve coupling between through-silicon vias (TSVs), and utilizing spare TSVs to improve yield and timing. Other emerging technology options include physical design for sub-threshold design paradigm and digital microfluidic biochips.

This special section highlights the continued need for innovations in physical design to address the increasing complexity of digital implementation. We would like to thank the authors and reviewers for their tremendous efforts in making the special issue possible.

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