A Study of the Electroforming Process in 1T1R Memory Arrays

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Abstract—For reproducible resistive switching in memristive devices, electroforming is a crucial process. However, a deeper understanding of the electroforming process is still lacking due to unavailability of a proper simulation tool. Here, we propose a physics-based compact model for the electroforming of valence change mechanism (VCM) memristive devices. The developed JART VCM Forming model is experimentally validated with the ZrOx-based memristive device. Furthermore, the electroforming process in different 1T1R memristive arrays is simulated with this model. The study shows that the electrical characteristics of each device in the array after the forming process are influenced by word/bit line series resistance. In addition, control effects depending on the channel width and applied gate voltage of transistor in the 1T1R cell are also investigated with the compact model simulation.

Index Terms—Compact model, crossbar array, electroforming, memristive device, ReRAM.

I. INTRODUCTION

VALENCE change mechanism (VCM)-based memristive device is one of the most attractive candidate for next-generation memory because of its energy-efficient, fast, scalable characteristics. The structure of the VCM device cell consists of a simple metal/oxide/metal stack, which makes it suitable for nm-scale electric device integration processes. In various type of oxides, such as HfO_2, TiO_2, Ta_2O_5, or $SrTiO_3$, memristive switching phenomena were shown [1]–[3], with different combinations of metal electrode [4]. Typically, a pair of one reactive metal with a low work function, reactive electrode (also called ohmic electrode), and one inert metal with a high work function (also called electronically active electrode) are usually chosen. The different chemical reactivity of the electrodes leads to the partial reduction of switching oxide layer, which takes place dominantly at the interface with an
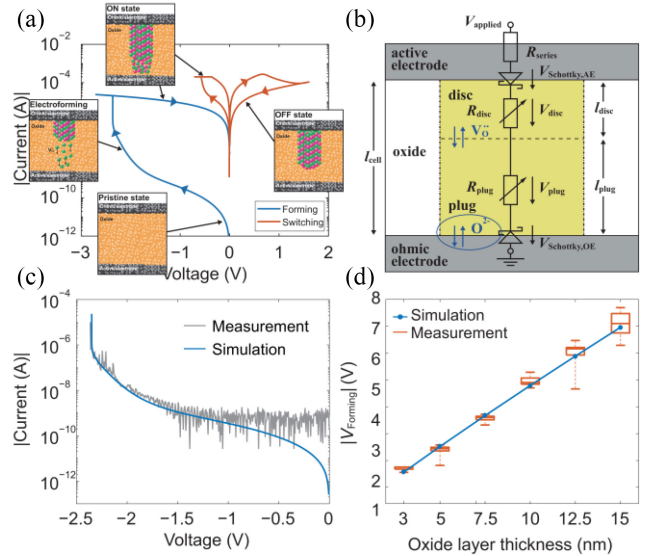
Fig. 1. (a) Illustration of the mechanism of electroforming and switching process in VCM memristive device. (b) Equivalent circuit diagram and the compact model components for the electroforming simulation on VCM memristive device. The blue arrows show the exchange process of the ionic defects between each regions. (c) Simulated electroforming *I-V* sweep curve (blue) compared to the experimental data of a ZrOx-based VCM device. Both in simulation and experiment, the thickness of the oxide layer is 5 nm. (d) Corresponding forming voltage as a function of the oxide thickness compared to measurement data of a ZrOx-based VCM device (orange) VCM cell [10]. For the simulation of the thickness variation, $v_0 = 2 \cdot 10^{12}$ Hz was used instead of the listed value in Table I.

ohmic electrode due to an anodic oxidation [5]. This is the driving force for the electroforming process and leads to a nonuniform distribution of oxygen defects during the electroforming [6]–[9]. To understand the main kinetics of this process and the corresponding change in the electrical characteristics of the VCM cell, a physically well-defined simulation compact model is required.

Fig. 1(a) shows the detailed mechanism of the electroforming and switching process in a filamentary VCM cell. The process is induced by the migration of oxygen vacancies within a filamentary region provided that an electric field across the VCM cell. The filament is divided into a plug region (nearby the surface between the ohmic electrode and the oxide) and a disc region (nearby the surface between active electrode and oxide). To trigger the electroforming process from the pristine state of the VCM cell, a positive potential is applied at the ohmic electrode (or a negative potential at the active electrode). Due to an anodic oxidation process, oxygen ions are extracted from the oxide and partially oxidize

the ohmic electrode [11]. The partially oxidized electrode will be still conducting. The anodic oxidation leaves behind two positively charged oxygen vacancies in the oxide, which will move toward the disc region with the applied electric field. Because the vacancies act as mobile donors, the resistance of the disc/plug region decreases with an increased oxygen vacancy concentration creating a conducting path. When a high current starts to flow through the filament region, the electroforming process is completed. The successive switching process is controlled by the polarity of applied voltage inducing a partial increase/decrease of vacancy concentration in the disc. The electrical characteristics of the VCM cell are highly influenced by the electroforming process. For example, the total number of oxygen vacancies in the filament is varied by the current compliance (I_{cc}) and overshoot during the forming process [6], [12].

While various type of compact models for the VCM switching mechanism has been proposed [12]–[15], compact models for the electroforming process have been rarely reported. We have recently proposed a compact model for the electroforming process that includes the concept of oxygen exchange between the plug region and the ohmic electrode. The equivalent circuit diagram of the compact model is shown in Fig. 1(b) [16].

For memristive-based neuromorphic computing applications, such as the convolutional neural network (CNN), an 1T1R array is required for vector matrix multiplication (VMM) [17], [18]. The VCM-based memristive devices offer multilevel programming capability, structural simplicity, and energy efficiency and have attracted attention for the kernel node device. For this application, the electrical characteristics after the forming process in the 1T1R array should be well understood for avoiding the poor device yield and nonuniformity. Furthermore, one must investigate various type of the array configuration, because the signal path of VMM-based learning process could be different with organization of the 1T1R array [19], [20].

In this work, a physics-based compact model for the electroforming process is applied to different 1T1R memristive crossbar array configuration for studying the electrical characteristics at each node. Especially, the influence of the parasitic line series resistance in different array configurations is investigated. Furthermore, the influence of the transistor parameters in the 1T1R cell is analyzed. The simulation results obtained with the VCM compact model in the 1T1R array give a guideline for the parameter design of memristive crossbar arrays for neuromorphic computing application.

II. ELECTROFORMING MODEL AND ITS VALIDATION

For modeling the electroforming process, a similar approach as in the Jülich Aachen resistive switching tool (JART) VCM models proposed in [13] is applied. The electroforming model was originally reported in [16], but the full equation system has been not well explained, yet. Thus, we here report a comprehensive model for the forming process. Each layer component in a memristive cell should be included in the equivalent circuit of the model. Fig. 1(b) shows the equivalent

circuit diagram of the VCM cell. It consists of the resistance of the two electrodes, and the electrical components of the filamentary region as outlined below. The voltage is applied to the active top electrode while the bottom ohmic electrode is grounded.

In the proposed model, the filament is considered as a cylindrical region and divided into two regimes: 1) the disc region with the length l_{disc} and resistance R_{disc} and 2) the plug region with the length l_{plug} and resistance R_{plug}. The cross-sectional area of the filament is given by $A = \pi r_{fill}^2$ and length l_{cell} is equivalent to the oxide layer length. The interface between AE/disc and OE/plug denoted as $V_{schottky,AE}$ and $V_{schottky,OE}$ describes the electrical transport at each of the two interfaces. The electrical model is identical to the previous JART VCM v2 model [13]. In contrast to the JART VCM v2, oxygen exchange processes between the electrodes and the oxide region are also considered. The oxygen vacancy concentration in the disc N_{disc} and the plug N_{plug} is defined as state variables in the JART VCM forming model, but also the oxygen concentration in the OE $N_{O,OE}$ and the AE $N_{O,AE}$ are state variables. In the following, we first describe the electrical model and then the ionic model constituting together the JART VCM Forming model.

For calculating the main electrical characteristics of the VCM cell, the current flow through the cell is defined with Kirchhoff's law

$$V_{applied} - \left[V_{schottky,AE} + V_{schottky,OE} + I \cdot (R_{disc} + R_{plug} + R_{series}) \right] = 0. \quad (1)$$

The resistances of the two regions of the filament are calculated with

$$R_{disc} = \frac{l_{disc}}{A \cdot z_{V_o} e N_{disc} \mu_n(T)}$$
$$= \frac{l_{disc}}{A \cdot z_{V_o} e N_{disc} \mu_{n0}} \exp\left(\frac{\Delta W}{k_B T}\right) \quad (2)$$

$$R_{plug} = \frac{l_{plug}}{A \cdot z_{V_o} e N_{plug} \mu_n(T)}$$
$$= \frac{l_{plug}}{A \cdot z_{V_o} e N_{plug} \mu_{n0}} \exp\left(\frac{\Delta W}{k_B T}\right). \quad (3)$$

In (2) and (3), e is the elementary charge, z_{Vo} is the charge number of the oxygen vacancies, k_B denotes the Boltzmann constant, T is the temperature, μ_{n0} is the temperature-independent prefactor of the mobility, and ΔW is an activation energy for the temperature-dependent mobility.

The current flow through the Schottky diode is defined using thermionic and thermionic field emission in forward and reverse bias, respectively. In the VCM cell, the Schottky diode at the AE/oxide interface and the OE/oxide interface is connected in the opposite directions. The calculation of the current flow considers with a forward/reverse bias of applied voltage [21]

$$I = \begin{cases} \text{sign}(V_{applied}) \cdot I_{TE} & V_{forward} > 0 \\ \text{sign}(V_{applied}) \cdot I_{TFE,reverse} & V_{forward} \leq 0. \end{cases} \quad (4)$$

At the AE/oxide interface, a positive voltage equals a forward bias ($V_{forward} = V_{Schottky,AE}$, $V_{reverse} = -V_{Schottky,AE}$). In

contrast, at the OE/oxide interface, a positive voltage corresponds to a reverse bias ($V_{\text{forward}} = -V_{\text{Schottky,OE}}$, $V_{\text{reverse}} = V_{\text{Schottky,OE}}$).

The thermionic emission current I_{TE} at the Schottky interface within a forward bias voltage is calculated by

$$I_{\text{TE}} = AA^*T^2 \exp\left(-\frac{e\phi_{\text{Bn}}}{k_{\text{B}}T}\right)\left(\exp\left(\frac{eV}{k_{\text{B}}T}\right) - 1\right). \quad (5)$$

In (5), A denotes the cross-sectional area. The effective barrier height $e\phi_{Bn}$ and the effective Richardson constant A^* are calculated according to [21]

$$\phi_{\text{Bn}} = \phi_{\text{Bn0}} - \sqrt{4\frac{e^3 N_D(\phi_{\text{Bn0}} - \phi_{\text{n}} - V)}{8\pi^2\epsilon_{\phi_{\text{B}}}^3}} \quad (6)$$

$$A^* = \frac{4\pi e m_{\text{eff}} k_{\text{B}}^2}{h^3}. \quad (7)$$

Here, N_D denotes donor concentration in the oxide, in VCM cell oxygen vacancies take a role of double-charged donor, and it is applied within $N_D = 2N_{Vo}$. The oxygen vacancy concentration N_{Vo} is defined as the disc vacancy concentration N_{disc} at the AE interface and the plug vacancy concentration N_{plug} at the OE interface. $e\phi_{Bn0}$ is the energy difference between the metal work function and oxide electron affinity, m_{eff} is the effective mass of the carrier, and $\epsilon_{\phi B}$ is the permittivity related to the barrier lowering.

Under reverse bias voltage, the thermionic field emission current I_{TFE} is calculated by [21]

$$I_{\text{TFE,reverse}} = A\frac{A^*T^2}{k_{\text{B}}}\sqrt{\pi W_{00}e\left(-V + \frac{\phi_{\text{Bn}}}{\cosh^2(W_{00}/k_{\text{B}}T)}\right)}$$
$$\cdot \exp\left(-\frac{e\phi_{\text{Bn}}}{W_0}\right) \cdot \left(\exp\left(\frac{-eV}{\zeta}\right) - 1\right). \quad (8)$$

The parameters W_{00}, W_0, and ζ are described as

$$W_{00} = \frac{eh}{4\pi}\sqrt{\frac{N_{\text{D}}}{m_{\text{eff}}\epsilon_{\text{s}}}} \quad (9)$$

$$W_0 = W_{00}\coth\left(\frac{W_{00}}{k_{\text{B}}T}\right) \quad (10)$$

$$\zeta = \frac{W_{00}}{(W_{00}/k_{\text{B}}T) - \tanh(W_{00}/k_{\text{B}}T)}. \quad (11)$$

The energy difference between the Fermi level and the conduction band edge on each electrode is denoted with $\phi_{\text{n,AE/OE}}$, calculated based on the Fermi–Dirac integral by Nilsson [22]

$$\phi_{\text{n,AE/OE}} = -\frac{k_{\text{B}}T}{e}\mathcal{F}_{1/2}^{-1}\left(\frac{z_{V_{\text{o}}}N_{\text{disc/plug}}}{2\left(2\pi m_{\text{eff}}k_{\text{B}}T/h^2\right)^{2/3}}\right) \quad (12)$$

$$\mathcal{F}_{1/2}^{-1}(u) = \frac{\ln(u)}{1 - u^2} + \left(3\sqrt{\pi}u/4\right)^{2/3}$$
$$- \frac{\left(3\sqrt{\pi}u/4\right)^{2/3}}{1 + \left(0.24 + 1.08\left(3\sqrt{\pi}u/4\right)^{2/3}\right)^{2/3}}. \quad (13)$$

For implementing the electroforming process, the extracted oxygen ions, which is stored in the OE, is also considered. Thus, three main state variables, N_{disc}, N_{plug}, and the oxygen ion concentration in the OE $N_{\text{O,OE}}$, are used for simulating this process. Three coupled ordinary differential equations (ODEs) are calculated in the model for these three state variables. The change of N_{disc} and N_{plug} is modeled with three types of ionic currents: I_{ion} denotes the flux of oxygen vacancies between the plug and the disc. The oxygen exchange between disc and active electrode and the oxygen exchange between plug and ohmic electrode are described by the ionic currents $I_{\text{ion,BV,AE}}$ and $I_{\text{ion,BV,OE}}$. The corresponding ODEs are read

$$\frac{dN_{\text{disc}}}{dt} = -\frac{1}{z_{V_{\text{o}}}eAl_{\text{disc}}} \cdot I_{\text{ion}} + \frac{1}{z_{V_{\text{o}}}eAl_{\text{disc}}} \cdot I_{\text{ion,BV,AE}} \quad (14)$$

$$\frac{dN_{\text{plug}}}{dt} = +\frac{1}{z_{V_{\text{o}}}eAl_{\text{plug}}} \cdot I_{\text{ion}} - \frac{1}{z_{V_{\text{o}}}eAl_{\text{plug}}} \cdot I_{\text{ion,BV,OE}}d \quad (15)$$

The ionic current I_{ion} between the plug and the disc is represented with the drift current $I_{\text{ion,drift}}$ and the diffusion current $I_{\text{ion,diffusion}}$ and corresponds to [13]

$$I_{\text{ion}} = I_{\text{ion,drift}} + I_{\text{ion,diffusion}}$$
$$= ACN_{\text{real}}\sinh\left(\frac{az_{V_{\text{o}}}eE}{2k_{\text{B}}T}\right) \cdot F_{\text{limit}}$$
$$- AC\frac{a}{2}\frac{dN}{dx}\cosh\left(\frac{az_{V_{\text{o}}}eE}{2k_{\text{B}}T}\right) \quad (16)$$

with

$$N_{\text{real}} = \sqrt{N_{\text{disc}} \cdot N_{\text{plug}}} \quad (17)$$

$$\frac{dN}{dx} = \frac{N_{\text{plug}} - N_{\text{disc}}}{0.5 \cdot l_{\text{cell}}} \quad (18)$$

$$C = 2z_{V_{\text{o}}}eav_0\exp\left(-\frac{\Delta W_{\text{A}}\left[\sqrt{1 - \gamma^2} + \gamma \arcsin\gamma\right]}{k_{\text{B}}T}\right) \quad (19)$$

$$\gamma = \frac{az_{V_{\text{o}}}eE}{\pi \Delta W_{\text{A}}} \quad (20)$$

$$F_{\text{limit}} = \begin{cases} \left[1 - \left(\frac{N_{\text{plug}}}{N_{\text{max}}}\right)^{10}\right] \cdot \left[1 - \left(\frac{N_{\text{min}}}{N_{\text{disc}}}\right)^{10}\right] & V_{\text{applied}} > 0 \\ \left[1 - \left(\frac{N_{\text{disc}}}{N_{\text{max}}}\right)^{10}\right] \cdot \left[1 - \left(\frac{N_{\text{min}}}{N_{\text{plug}}}\right)^{10}\right] & V_{\text{applied}} < 0. \end{cases} \quad (21)$$

In (16)–(21), a is the hopping distance, v_0 is the attempt frequency, ΔW_A is the migration barrier, and N_{min} and N_{max} are the limits of the vacancy state variables. The minimum vacancy concentration N_{min} is defined as one defect in the respective volume and calculated as listed in Table I.

During electroforming, the oxygen exchange process happens at the OE due to anodic oxidation. The oxygen exchange reaction at the AE can be neglected in this case. The influence of $I_{\text{ion,BV,AE}}$ element is also neglected in the ODEs. The change of the oxygen concentration in the OE is determined by $I_{\text{ion,BV,OE}}$, and its ODEs are given by

$$\frac{dN_{\text{O,OE}}}{dt} = -\frac{1}{z_{V_{\text{o}}}eAl_{\text{OE,eff}}} \cdot I_{\text{ion,BV,OE}}. \quad (22)$$

In (22), $l_{\text{OE,eff}}$ denotes the active thickness of the OE in which the extracted oxygen is stored.

To define the ionic exchange current density at the interface of an electrode, the exchange reaction is described with

$$O''_{\text{ad(M)}} + V^{\cdot\cdot}_{\text{O(ox)}} \rightleftharpoons V^\times_{\text{ad(M)}} + O^\times_{\text{O(ox)}}. \quad (23)$$
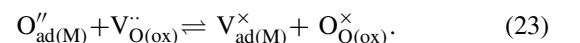
The ionic exchange current density by oxidation/reduction of the oxide is modeled using a Butler–Volmer equation, $J_{O,I}$ denotes the current density for forward reaction, and $J_{O,II}$ for reverse direction as

$$J_{O,I} = z_O e N_{O,ad(M)} k_I^0 \exp\left(-\frac{\Delta G_I}{k_B T}\right)\exp\left(-\frac{\alpha z_O e}{k_B T}\eta\right) \quad (24)$$

$$J_{O,II} = -z_O e N_{O,ox} k_{II}^0 \exp\left(-\frac{\Delta G_{II}}{k_B T}\right)\exp\left(-\frac{(1-\alpha)z_O e}{k_B T}\eta\right). \quad (25)$$

k_I^0 (k_{II}^0) is the reaction rate coefficient for the reduction (oxidation) of the oxide, α is the charge transfer coefficient, z_O is the charge of an oxygen ion, and η is the overpotential in the Helmholtz layer of the ion transfer system. $N_{O,ad(M)}$ is the concentration of oxygen ions absorbed in the metal, and $N_{O,ox}$ is the concentration of oxygen on lattice sites in the oxide. The corresponding activation energy for reduction (oxidation) of the oxide is denoted as $\Delta G_I (\Delta G_{II})$ [23].

At the surface of each filament region, the total ionic current density is defined by the oxygen exchange from metal electrode (M) to the oxide (Ox), and $J_{O,M\rightarrow Ox}$ is calculated with the sum of the oxidation and reduction ionic exchange current densities

$$\begin{aligned} J_{O,M\rightarrow Ox} &= J_{O,I} + J_{O,II} \\ &= z_O e N_{O,ad(M)} k_I^0 \exp\left(-\frac{\Delta G_I}{k_B T}\right)\exp\left(-\frac{\alpha z_O e}{k_B T}\eta\right) \\ &\quad - z_O e N_{O,ox} k_{II}^0 \exp\left(-\frac{\Delta G_{II}}{k_B T}\right)\exp\left(-\frac{(1-\alpha)z_O e}{k_B T}\eta\right). \end{aligned} \quad (26)$$

The oxygen exchange current at the interface between the OE and the oxide $I_{ion,BV,OE}$ in (15) is calculated by

$$\begin{aligned} I_{ion,BV,OE} &= A J_{O,OE\rightarrow Ox} \\ &= -A z_O e N_{O,OE} k_{I,OE}^0 exp\left(-\frac{\Delta G_{I,OE}}{k_B T}\right) \\ &\quad \cdot \exp\left(-\frac{\alpha_{OE} z_O e}{k_B T}V_{Schottky,OE}\right) \cdot F_{limit,OE,I} \\ &\quad + A z_O e N_{O,plug} k_{II,OE}^0 exp\left(-\frac{\Delta G_{II,OE}}{k_B T}\right) \\ &\quad \cdot \exp\left(\frac{(1-\alpha_{OE}) z_O e}{k_B T}V_{Schottky,OE}\right) \cdot F_{limit,OE,II}. \end{aligned} \quad (27)$$

The oxygen concentration in the plug $N_{O,plug}$ results from the total oxygen concentration $N_{O,oxide,max}$ of the oxide material and the oxygen vacancy concentration in the plug to

$$N_{O,plug} = N_{O,oxide,max} - N_{plug}. \quad (28)$$

The limiting factors $F_{limit,OE,I(II)}$ are window functions constraining the state variables to their limits. They are defined according to

$$F_{limit,OE,I} = \left[1 - \left(\frac{N_{min}}{N_{plug}}\right)^{10}\right] \cdot \left[1 - \left(\frac{N_{O,OE,min}}{N_{O,OE}}\right)^{10}\right] \quad (29)$$

TABLE I
SIMULATION PARAMETERS

Symbol	Value	Symbol	Value
l_{cell}	5 nm	ε	$17 \cdot \varepsilon_0$
l_{disc}	$l_{cell}/4$	$\varepsilon_{\phi B}$	$5.5 \cdot \varepsilon_0$
l_{plug}	$l_{cell} - l_{disc}$	$e\phi_{Bn0,AE}$	0.4 eV
R_{fill}	30 nm	$e\phi_{Bn0,OE}$	0.3 eV
$l_{OE,eff}$	1 nm	μ_{n0}	$5 \cdot 10^{-5}$ m^2/(Vs)
z_{Vo}	2	ΔE_{ac}	0.05 eV
z_O	-2	$N_{O,oxide,max}$	$5.6 \cdot 10^{28}$ m^{-3}
a	0.5 nm	N_{max}	$5 \cdot 10^{27}$ m^{-3}
v_0	$4 \cdot 10^{12}$ Hz	N_{min}	$1/(A \cdot l_{cell})$
ΔW_A	0.9 eV	$N_{O,OE,min}$	$1/(A \cdot l_{OE,eff})$
α_{OE}	0.5	$N_{disc,initial}$	N_{min}
$k_{I,OE}^0$	$1 \cdot 10^4$ m/s	$N_{plug,initial}$	N_{min}
$k_{II,OE}^0$	$2 \cdot 10^4$ m/s	$N_{O,OE,initial}$	$N_{O,OE,min}$
$\Delta G_{I,OE}$	1.3 eV	$R_{th,eff}$	$5 \cdot 10^7$ K/W
$\Delta G_{II,OE}$	1.05 eV	R_{series}	200 Ω
m_{eff}	$9.1 \cdot 10^{-31}$ kg	T_0	273 K

and

$$F_{limit,OE,II} = \left[1 - \left(\frac{N_{plug}}{N_{max}}\right)^{10}\right]. \quad (30)$$

Here, $N_{O,OE,min}$ is the minimum oxygen concentration in the OE and depends on the effective volume of the OE in which the oxygen is "stored" as listed in Table I. The minimum concentration $N_{mO,OE,min}$ is equal to the case that exactly one O atom in this volume.

The electric field E in (16) and (20) is defined according to

$$E = \left(V_{Schottky,AE} + V_{disc} + V_{plug} + V_{Schottky,OE}\right)/l_{cell}. \quad (31)$$

The local temperature T is calculated based on the power dissipation in the filament due to the Joule heating

$$T = \left(V_{disc} + V_{plug}\right) \cdot I \cdot R_{th,eff} + T_0 \quad (32)$$

where I is the electronic current, $R_{th,eff}$ is the effective thermal resistance, and T_0 is the initial temperature of ambient. The simulation model is implemented in MATLAB and Verilog-A, which runs within the CADENCE environment. Table I lists all simulations parameters used in this study.

To validate the electroforming compact model, simulations with parameters based on Pt/ZrO$_x$/Ta/Pt device are performed and compared to the experimental data published by Kindsmüller *et al.* [10]. In this study, a dependence of the electroforming voltage on the thickness of the ZrO$_x$ layer is observed. It shows that the forming voltage increases linearly with the oxide thickness. The Pt/ZrO$_x$ interface is regarded as the AE/oxide interface, and the Ta/ZrO$_x$ interface is the OE/oxide interface. For the electroforming simulation, the same layer thicknesses as in the experiment are used. Likewise, a voltage sweep rate is also applied with 1 V/s in the simulation. Note that we chose another polarity convention than in the experimental study setting the Ta/Pt electrode to GND and applying the negative voltage to the active Pt electrode. The forming voltage is defined as the voltage point at which a current level of 1 μA is reached. This criterion is the same in experiment and simulation.

Fig. 1(c) shows the simulated *I-V* characteristics (blue line) of the electroforming processes using a 5 nm-thick ZrO_x layer in comparison to the experimental data (gray line). The simulation result shows a good agreement with the measurement data at voltages $|V_{applied}| > |-1$ V$|$. At the other range of voltage ($|V_{applied} < |-1$ V$|$), the measurement data are within the resolution limit of the measurement setup leading to a plateau-like feature. At high voltages, the forming event appears as an abrupt increase of the current value.

We also studied the thickness dependence of the forming process in the simulation. The same range of the ZrO_x layer thicknesses was used as in experiment [10]. The simulation results feature that the forming voltage $|V_{Forming}|$ is increased with oxide thickness. The simulated trend of the forming voltage plotted in Fig. 1(d) also has a good agreement with the experimental measurement data.

III. ELECTROFORMING SIMULATION IN 1T1R CELL

In the memristive 1T1R memory array, each node cell consists of one transistor and one memristor connected serially. To simulate the electroforming in the 1T1R single cell, the JART VCM Forming model and a BSIM 4 transistor model for bulk CMOS are applied. Fig. 2(a) shows an illustration of the simulated 1T1R single cell. The voltage source for electroforming V_{WL} is connected with the OE of memristor via the word line resistance R_{WL}. The AE of memristor is directly connected to the drain of transistor. The source of transistor is connected to GND via the bit line resistance R_{BL}. The current flows through the word line resistance, the memristor, and the transistor channel over the bit line to GND. In addition, the voltage source for the transistor control V_{select} is connected to the gate of transistor. The memristive devices are arranged in a way that they form with a negative voltage applied to the word line to be consistent with the voltage convention in the previous section. In reality, the memristive device in the 1T1R cell would be placed "upside down." Then, a positive voltage needs to be applied to the OE in order to form the cell.

In this simulation, we have chosen the 45-nm CMOS technology node, where the transistor width and length are kept to be same as the node. In the memristor model, the maximum vacancy concentration of N_{max} listed in Table I is replaced by $8 \cdot 10^{27}$ m^{-3}. The transistor model includes a parasitic resistance factor, i.e., the junction resistance at the drain [24], [25]. Its value is smaller than the series resistance parameter R_{series}, which can be considered as a contact resistance in the VCM model. The influence of the junction resistance between VCM cell and transistor is neglected, but is supposed to be lower than the segment resistance.

Fig. 2(b) and (c) shows the simulated electrical characteristics of the memristor in a single 1T1R cell. In this simulation, each line series resistance for WL/BL was assumed to be 10 Ω and voltage sweep rate was 1 V/s for both memristor OE and transistor gate electrode. The channel current was limited by a gate voltage of 0.5 V. During the electroforming phase when the forming voltage 1.5 V was applied for 6.5 s to the VCM cell, the transient current level suddenly increased after 5 s. The vacancy concentration within each
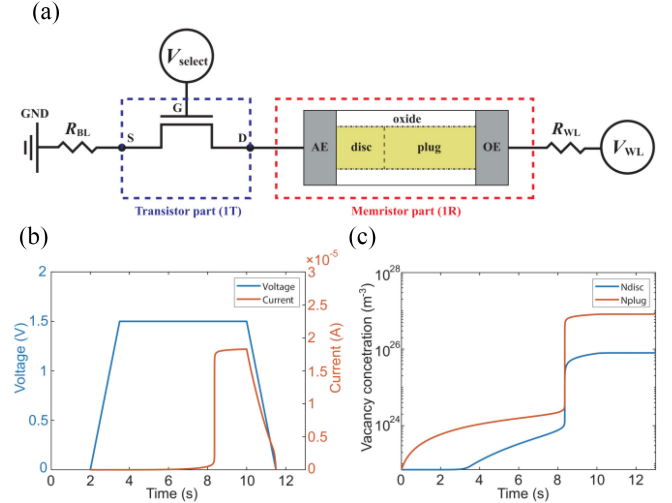

Fig. 2. (a) Illustration of the simulated 1T1R single cell, (b) the simulated I-V sweep curve, and (c) the vacancy concentration during electroforming.

layer of the filament also increased at the same time as shown in Fig. 2(c). While the disc concentration is almost constant at first, only the plug concentration increases. Then, the disc concentration starts increasing, but slower than plug concentration. After about 8 s, both concentrations increase abruptly also leading to the abrupt current increase in the *I-V* characteristic. This sudden increase is due to the positive feedback of Joule heating effect because of a thermal runaway similar to the case reported for the SET resistive switching transition from a high resistive to the low resistive status [26], [27]. With this simulation result, the electroforming process in the 1T1R single node cell is verified with the compact model simulation

IV. MEMRISTIVE 1T1R ARRAY CONFIGURATIONS

Three different types of 1T1R crossbar array with m word lines (WL) and n bit lines (BL) are feasible when the lines are only structured horizontally or vertically. Each array unit consists of a memristive VCM cells (1R), and a select transistor (1T) to prevent unintended sneak path currents and half-select issues [28]. The select lines (SLs) are connected to the transistor gates for activating the transistor of each 1T1R cell.

Fig. 3 shows each type of 1T1R array configuration. In case of the typical-type array in Fig. 3(a), the voltage for the electroforming of VCM devices is applied to the vertical WL, and the current flows through the WL and the unit cell over the BL to GND, when the transistor channel at the targeted cell is conducting. The SL is connected to the gate of the transistors along horizontal lines. The operation of each transistor is controlled by the voltage on the SL. In contrast to the typical array, the vertical-type array in Fig. 3(b) has vertical SLs for each transistor gate, and the voltage for the electroforming is applied to the horizontal WLs. In case of the pseudocrossbar array in Fig. 3(c), both the WL and the SL are aligned in parallel in horizontal direction. The devices on the same WL can be operated at once. In this way, the cell operation on the line cannot be controlled individually.
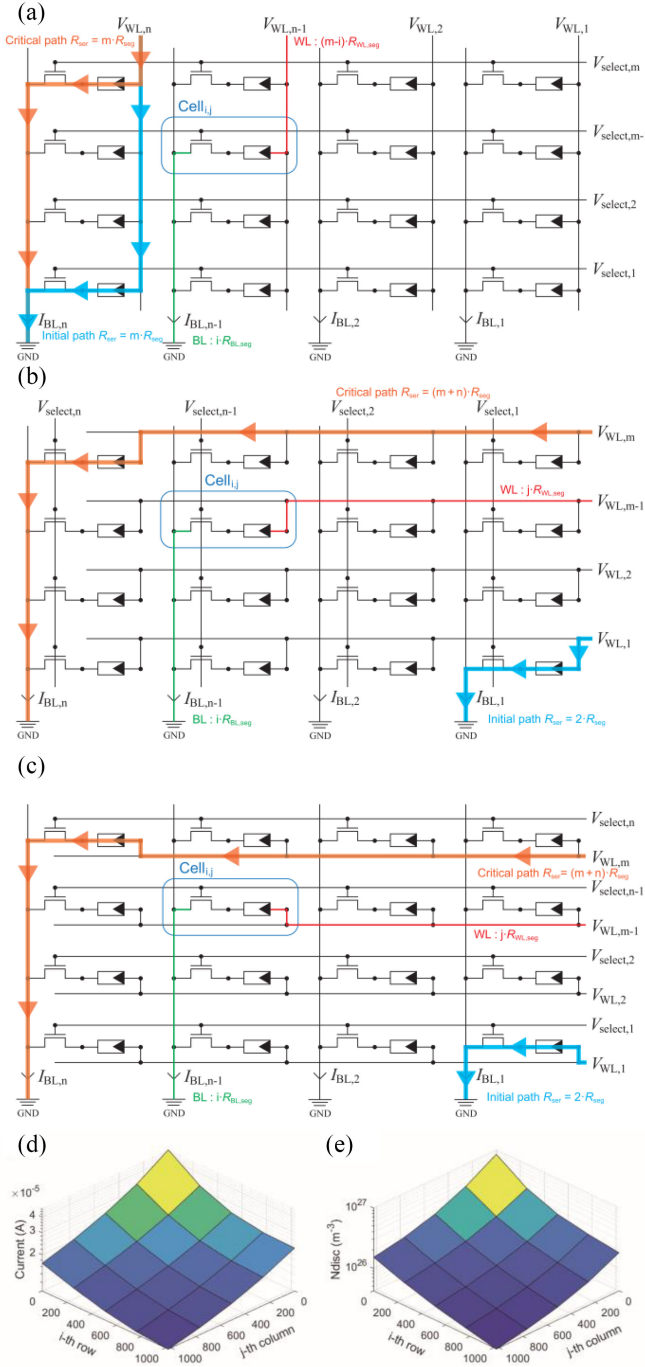
Fig. 3. Illustration of (a) typical-type, (b) vertical-type, and (c) pseudocross-bar 1T1R array for neuromorphic applications build with n columns and m rows and the voltage driver for corresponding word line $V_{\mathrm{WL},j}$, and transistor select signals $V_{\mathrm{select},i}$. The influence of the line resistance in each cell (m,n) is observed. (d) 3-D plot example for the read current level of the VCM cells after forming at each array point in case of the vertical-type array and (e) its vacancy concentration after the forming.

In the neuromorphic application system, an analog VMM with the crossbar array is presented by

$$\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \\ M_{31} & M_{32} \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix}. \tag{33}$$

M_{ij} is the synaptic weight of each array node, w_i is the input read signal for mapping, and z_i is the accumulative decipher signal with output.

In the 1T1R memristive device array, the analog conductance value of the memristor in each cell G_{ij} reflects the synaptic weight, the read voltage applied to the WL v_i is the input read signal, and the output current sensed at the BL I_j is the output signal. The relation with these elements is calculated as the VMM

$$I_j = \mathrm{SUM}_i\left(v_i \cdot G_{ij}\right). \tag{34}$$

Since the 1T1R array has different types of configurations, the most suited type of array should be chosen depending on the required array operations and applications. In case of the typical-crossbar array, the transistor in each cell can be opened for several clock cycles to achieve analog inputs, and the BL can be charged to different levels. This scheme requires a capacitive read out (voltage sensing). For a correct operation, the charging time of BL should be longer than the longest time one of the transistors remains open. Thus, it can make the computing time longer. In case of the vertical array, different analog voltages can be applied to the WL and the accumulated current can be read at the BL. The programming analog values are best performed on a single-cell level. However, it comes at the expense of an increased energy consumption to prevent write disturb. Otherwise, in case of the pseudocrossbar array, a full vector–matrix product can be performed in one signal cycle by reading the information on the BLs in parallel. During this operation, however, this array is a passive array, and sneak paths can make read failures. In addition, it is not clear if all BLs can be read in parallel anyway as the required read circuit might become too complex and large. Furthermore, the complex read circuit for the pseudocrossbar array can make the integration of neuromorphic system inefficient [17], [29].

In this research, the line series resistance of WLs and BLs is considered in the various array configuration. Each line segment resistance R_{seg} is assumed to be identical for the BL and the WL, i.e., $R_{\mathrm{BL,seg}} = R_{\mathrm{WL,seg}} = R_{\mathrm{seg}}$. Moreover, a quadratic configuration of the array with n = m is considered. The total series resistance R_{ser} on each cell can be different according to array type. The critical path as the longest way of current flow is colored as an orange line, and the initial path as the shortest way of current flow is colored as a sky blue line is drawn in Fig. 3(a)–(c). The R_{ser} for the initial/critical path of each arrays are also calculated.

In the typical array, each cell on the same column has a uniform R_{ser}, because it is calculated as $R_{\mathrm{ser}} = (m-i) \cdot R_{\mathrm{WL,seg}} + i \cdot R_{\mathrm{BL,seg}}$ when the cell (i, j) on the ith row and the jth column is formed. R_{ser} of critical path is $R_{\mathrm{ser}} = m \cdot R_{\mathrm{seg}}$, same as the case of the initial path. Therefore, there is no change on R_{ser}, and a minor effect of electroforming on the position of the cell is expected. Note that using different materials (and/or segment length) for WL and BL, the total line resistance will differ slightly, but the length of the critical path from input voltage to GND remains the same.

In case of the vertical array and pseudocrossbar array, the series resistance of each cell is calculated with $R_{\mathrm{ser}} = j \cdot R_{\mathrm{WL,seg}} + i \cdot R_{\mathrm{BL,seg}}$. R_{ser} can change dramatically

Fig. 4. Simulation results for the electroforming in the typical-type array. Current level after the forming with (a) 45- and (b) 90-nm transistor channel width. Vacancy concentration in the disc region after the forming with (c) 45- (d) 90-nm transistor channel width.
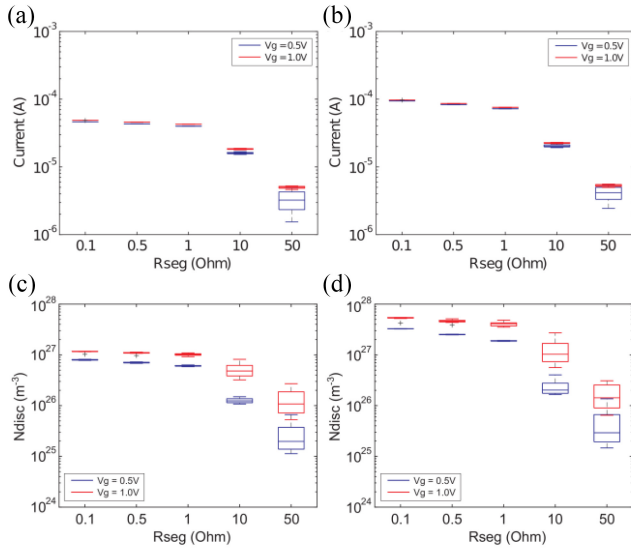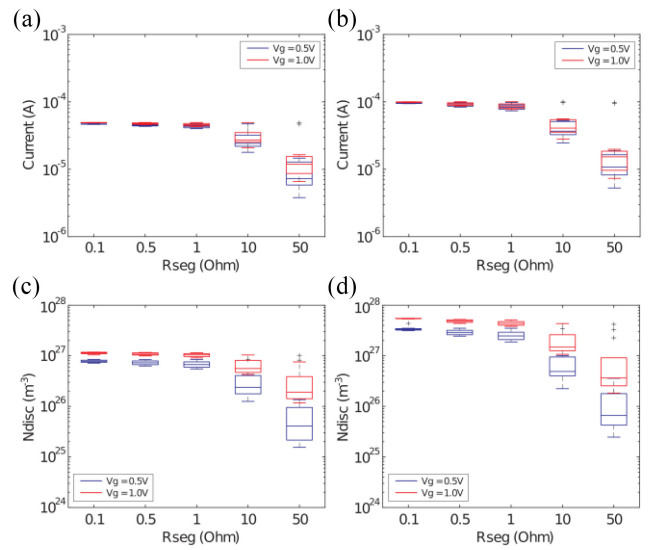

Fig. 5. Simulation results for the electroforming in the vertical-type array. Current level after the forming with (a) 45- and (b) 90-nm transistor channel width. Vacancy concentration in the disc region after the forming with (c) 45- and (d) 90-nm transistor channel width.

depending on position (i, j) in the array on each cell. The maximum R_{ser} is found with the critical path at position (m, n) as $R_{ser} = (m + n) \cdot R_{seg}$, and the minimum R_{ser} is found with the initial path at position (1, 1) as $R_{ser} = 2 \cdot R_{seg}$. With this difference of R_{ser}, we can expect a larger effect on the characteristics after forming in the vertical and pseudocrossbar array than typical-type array depending on the array cell position.

Fig. 3(d) and (e) shows an example of the simulated electrical characteristics distribution after the forming of each VCM cell in the vertical-type 1T1R array circuit. At point (1, 1) of the array, the cell has the highest value of current level after forming, because it has lowest series resistance. Especially, the vacancy concentrations after forming is also tilted with the line series resistance at each point. The results verify that the forming phenomena during the process are highly influenced by the line series resistance.

In the following, we translate the 3-D plots to 2-D box plots for better comparability. Each box in Figs. 4–6 will show the distribution of the characteristic value of all VCM cells in the array for each simulation. The highest value in the 3-D plot is positioned at the top line over the box [typically corresponding to cell (1,1)], and the lowest value is positioned at the bottom line below the box [corresponding to cell (m,n)]. The other values are distributed in the box, and the medium value is displayed at the middle line of the box.

V. ELECTROFORMING SIMULATION OF 1T1R ARRAY

A 1024×1024 1T1R memristive cell array is considered in this simulation. To form the cell (i, j), in the typical array case, $V_{select,i}$ is applied on the ith SL to open the transistor channel, the forming voltage is applied to $V_{WL,j}$ on jth WL, and the BL is set to ground state GND. On the contrary, in the vertical array, $V_{select,j}$ is applied on the jth SL to activate transistor, and the forming voltage is applied to $V_{WL,i}$ on the ith WL. In case of the pseudocrossbar array, $V_{select,i}$ is applied on ith SL and
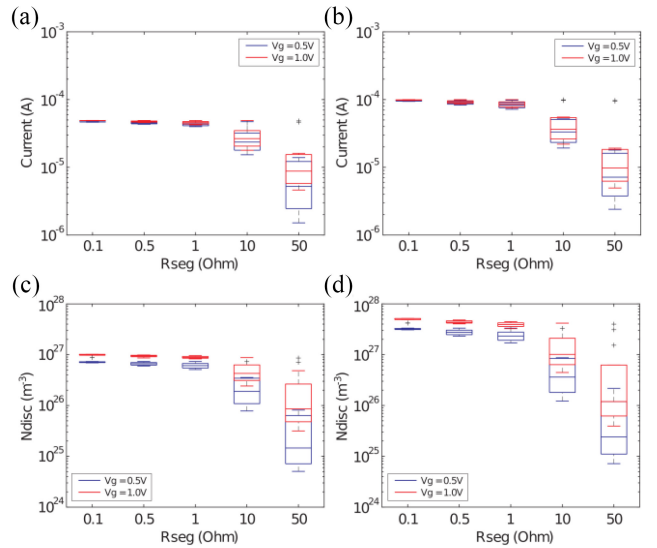
Fig. 6. Simulation results for the electroforming in the pseudocrossbar array. Current level after the forming with (a) 45- and (b) 90-nm transistor channel width. Vacancy concentration in the disc region after the forming with (c) 45- and (d) 90-nm transistor channel width.

the forming voltage is applied to $V_{WL,i}$ on the ith WL. The signals on the other lines are set to 0 V. The voltage pulse for electroforming consists of the forming phase and the read phase, both have a rectangular shape. In the forming phase, the voltage potential applied to the WL increases to 1.5 V with a sweep rate of 1 V/s. Then, the voltage is kept constant for 6.5 s and declines again to zero. During this phase, the voltage of 0.5/1 V is applied to SL and the transistor gates. Two different voltage levels are used to investigate the impact on the programmed states after electroforming. In the read phase, the signal of 0.3 V is applied to WL to read the current level. In addition, the vacancy concentration in the disc after forming at each cell is evaluated in this phase. In contrast to the forming

TABLE II
QUANTITATIVE RESULTS AFTER FORMING IN THE TYPICAL-TYPE ARRAY

Current level ([A], Transistor channel width = 45 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$4.627 \cdot 10^{-5}$	$4.641 \cdot 10^{-5}$	0.1	$4.846 \cdot 10^{-5}$	$4.885 \cdot 10^{-5}$
0.5	$4.309 \cdot 10^{-5}$	$4.344 \cdot 10^{-5}$	0.5	$4.572 \cdot 10^{-5}$	$4.609 \cdot 10^{-5}$
1	$3.977 \cdot 10^{-5}$	$4.018 \cdot 10^{-5}$	1	$4.249 \cdot 10^{-5}$	$4.302 \cdot 10^{-5}$
10	$1.528 \cdot 10^{-5}$	$1.681 \cdot 10^{-5}$	10	$1.788 \cdot 10^{-5}$	$1.885 \cdot 10^{-5}$
50	$1.545 \cdot 10^{-6}$	$4.867 \cdot 10^{-6}$	50	$4.537 \cdot 10^{-6}$	$5.253 \cdot 10^{-6}$
Vacancy Concentration ([m⁻³], Transistor channel width = 45 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$7.77 \cdot 10^{26}$	$8.19 \cdot 10^{26}$	0.1	$1.03 \cdot 10^{27}$	$1.18 \cdot 10^{27}$
0.5	$6.80 \cdot 10^{26}$	$7.27 \cdot 10^{26}$	0.5	$9.70 \cdot 10^{26}$	$1.13 \cdot 10^{27}$
1	$5.84 \cdot 10^{26}$	$6.32 \cdot 10^{26}$	1	$9.22 \cdot 10^{26}$	$1.10 \cdot 10^{27}$
10	$1.08 \cdot 10^{26}$	$1.50 \cdot 10^{26}$	10	$3.22 \cdot 10^{26}$	$8.17 \cdot 10^{26}$
50	$1.13 \cdot 10^{25}$	$6.64 \cdot 10^{25}$	50	$5.29 \cdot 10^{25}$	$2.27 \cdot 10^{26}$

Current level ([A], Transistor channel width = 90 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$9.398 \cdot 10^{-5}$	$9.451 \cdot 10^{-5}$	0.1	$9.688 \cdot 10^{-5}$	$9.733 \cdot 10^{-5}$
0.5	$8.286 \cdot 10^{-5}$	$8.361 \cdot 10^{-5}$	0.5	$8.603 \cdot 10^{-5}$	$8.685 \cdot 10^{-5}$
1	$7.184 \cdot 10^{-5}$	$7.280 \cdot 10^{-5}$	1	$7.514 \cdot 10^{-5}$	$7.632 \cdot 10^{-5}$
10	$1.927 \cdot 10^{-5}$	$2.188 \cdot 10^{-5}$	10	$2.198 \cdot 10^{-5}$	$2.308 \cdot 10^{-5}$
50	$2.442 \cdot 10^{-6}$	$5.432 \cdot 10^{-6}$	50	$4.965 \cdot 10^{-6}$	$5.586 \cdot 10^{-6}$
Vacancy Concentration ([m⁻³], Transistor channel width = 90 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$3.23 \cdot 10^{27}$	$3.28 \cdot 10^{27}$	0.1	$4.24 \cdot 10^{27}$	$5.47 \cdot 10^{27}$
0.5	$2.47 \cdot 10^{27}$	$2.55 \cdot 10^{27}$	0.5	$3.85 \cdot 10^{27}$	$5.13 \cdot 10^{27}$
1	$1.84 \cdot 10^{27}$	$1.92 \cdot 10^{27}$	1	$3.51 \cdot 10^{27}$	$4.83 \cdot 10^{27}$
10	$1.65 \cdot 10^{26}$	$4.02 \cdot 10^{26}$	10	$5.62 \cdot 10^{26}$	$2.72 \cdot 10^{27}$
50	$1.46 \cdot 10^{25}$	$1.36 \cdot 10^{26}$	50	$6.46 \cdot 10^{25}$	$3.09 \cdot 10^{26}$

TABLE III
QUANTITATIVE RESULTS AFTER FORMING IN THE VERTICAL-TYPE ARRAY

Current level ([A], Transistor channel width = 45 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$4.623 \cdot 10^{-5}$	$4.733 \cdot 10^{-5}$	0.1	$4.869 \cdot 10^{-5}$	$4.959 \cdot 10^{-5}$
0.5	$4.327 \cdot 10^{-5}$	$4.750 \cdot 10^{-5}$	0.5	$4.593 \cdot 10^{-5}$	$4.946 \cdot 10^{-5}$
1	$4.007 \cdot 10^{-5}$	$4.738 \cdot 10^{-5}$	1	$4.287 \cdot 10^{-5}$	$4.948 \cdot 10^{-5}$
10	$1.787 \cdot 10^{-5}$	$4.717 \cdot 10^{-5}$	10	$2.089 \cdot 10^{-5}$	$4.932 \cdot 10^{-5}$
50	$3.798 \cdot 10^{-6}$	$4.669 \cdot 10^{-5}$	50	$6.599 \cdot 10^{-6}$	$4.870 \cdot 10^{-5}$
Vacancy Concentration ([m⁻³], Transistor channel width = 45 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$7.15 \cdot 10^{26}$	$8.44 \cdot 10^{26}$	0.1	$1.04 \cdot 10^{27}$	$1.18 \cdot 10^{27}$
0.5	$6.27 \cdot 10^{26}$	$8.43 \cdot 10^{26}$	0.5	$9.94 \cdot 10^{26}$	$1.16 \cdot 10^{27}$
1	$5.50 \cdot 10^{26}$	$8.44 \cdot 10^{26}$	1	$9.07 \cdot 10^{26}$	$1.15 \cdot 10^{27}$
10	$1.25 \cdot 10^{26}$	$8.39 \cdot 10^{26}$	10	$4.26 \cdot 10^{26}$	$1.04 \cdot 10^{27}$
50	$1.55 \cdot 10^{25}$	$8.18 \cdot 10^{26}$	50	$1.17 \cdot 10^{26}$	$1.02 \cdot 10^{27}$

Current level ([A], Transistor channel width = 90 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$9.404 \cdot 10^{-5}$	$9.803 \cdot 10^{-5}$	0.1	$9.722 \cdot 10^{-5}$	10.045e-5
0.5	$8.361 \cdot 10^{-5}$	$9.807 \cdot 10^{-5}$	0.5	$8.693 \cdot 10^{-5}$	10.042e-5
1	$7.369 \cdot 10^{-5}$	$9.803 \cdot 10^{-5}$	1	$7.715 \cdot 10^{-5}$	10.039e-5
10	$2.459 \cdot 10^{-5}$	$9.742 \cdot 10^{-5}$	10	$2.802 \cdot 10^{-5}$	$9.982 \cdot 10^{-5}$
50	$5.276 \cdot 10^{-6}$	$9.486 \cdot 10^{-5}$	50	$7.331 \cdot 10^{-6}$	$9.740 \cdot 10^{-5}$
Vacancy Concentration ([m⁻³], Transistor channel width = 90 nm)					
V_g = 0.5 V			V_g = 1.0 V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$3.14 \cdot 10^{27}$	$3.50 \cdot 10^{27}$	0.1	$4.37 \cdot 10^{27}$	$5.52 \cdot 10^{27}$
0.5	$2.45 \cdot 10^{27}$	$3.50 \cdot 10^{27}$	0.5	$4.36 \cdot 10^{27}$	$5.23 \cdot 10^{27}$
1	$1.88 \cdot 10^{27}$	$3.50 \cdot 10^{27}$	1	$3.82 \cdot 10^{27}$	$5.11 \cdot 10^{27}$
10	$2.23 \cdot 10^{26}$	$3.45 \cdot 10^{27}$	10	$1.07 \cdot 10^{27}$	$4.33 \cdot 10^{27}$
50	$2.46 \cdot 10^{25}$	$3.27 \cdot 10^{27}$	50	$1.83 \cdot 10^{26}$	$4.19 \cdot 10^{27}$

phase, the voltage of 1.5 V is applied on the SL to fully open the transistor channel in the cell during the read phase. In this simulation, 45/90 nm was chosen for the transistor channel width condition, and a constant length 45 nm was applied. In addition, maximum vacancy concentration N_{max} in the JART VCM forming model was kept $8 \cdot 10^{27}$ m^{-3}, same as for the 1T1R single cell simulation.

Fig. 4 shows the simulated electrical characteristics of each cell in a typical 1T1R array. The implemented R_{seg} was chosen to 0.1, 0.5, 1, 10, and 50 Ω for investigating the impact of line resistance on cell characteristics after the forming. The quantitative maximum/minimum value of simulated results on each condition is represented in Table II. Fig. 4 shows that the current level and the vacancy concentration in the disc N_{disc} after the forming strongly decreases for higher R_{seg}, and for lower V_g. Especially, the meaning that N_{disc} is changed with R_{seg} and V_g indicates that the forming process on each cell was significantly influenced by R_{ser}. The distribution of the characteristic values is also getting larger with higher R_{seg}. When the transistor width is 45 nm, the N_{disc} value after forming is limited even though N_{max} is set to $8 \cdot 10^{27}$ m^{-3}. This limit can be released with increasing transistor width to 90 nm, and N_{disc} increases and approaches N_{max} for low R_{seg} and higher V_g range.

Fig. 5 shows the characteristics in the vertical 1T1R array. Similar trends of characteristics with R_{seg} and V_g dependence are also shown in the vertical 1T1R array simulation. The quantitative maximum/minimum value of simulated results are represented in Table III. In contrast to the case for the typical 1T1R array, the distribution range of the characteristics is much larger, and also widens for the higher R_{seg}. The vertical 1T1R array has a larger range of R_{ser} depending on the array point, since the length of the critical paths varies. Thus, the characteristics of each cell after the forming are more influenced by R_{ser} in the vertical-type array. N_{disc} after the forming also remains below N_{max} for 45-nm transistor channel width in the vertical 1T1R array. This, however, is inflated to N_{max} for 90-nm transistor channel width.

Fig. 6 shows the electrical characteristics in the pseudocrossbar array. The quantitative maximum/minimum value of simulated results is represented in Table IV. Also, in this case, the current level after electroforming and the vacancy concentration in disc decrease for higher R_{seg}, and for lower V_g. The trends of the characteristic values and the phenomena with limited N_{disc} for 45-nm transistor channel width are also similar as for the vertical-type array. In addition, the distribution range of the characteristic parameters is much larger than the typical- and the vertical-type array.

(a)   (b)

(c)   (d)

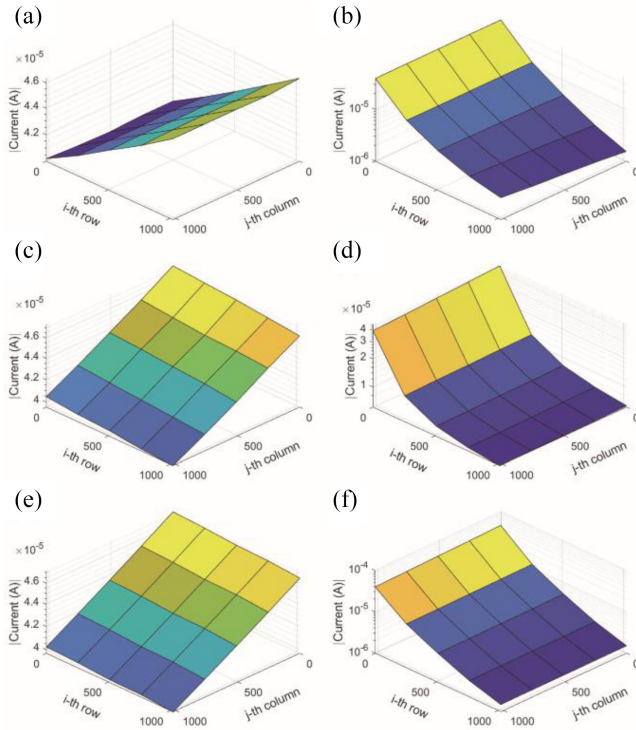(e)   (f)

Fig. 7. Simulation results with the asymmetric line segment resistance for the read current level of the 1T1R VCM cells after forming at each array point with (a) $R_{\mathrm{seg,BL}} = 0.1\Omega$, (b) $R_{\mathrm{seg,BL}} = 50\Omega$ in the typical-type array, (c) $R_{\mathrm{seg,BL}} = 0.1\Omega$, (d) $R_{\mathrm{seg,BL}} = 50\ \Omega$ in the vertical-type array, (e) $R_{\mathrm{seg,BL}} = 0.1\Omega$, and (f) $R_{\mathrm{seg,BL}} = 50\Omega$ in the pseudocrossbar array.

TABLE IV
QUANTITATIVE RESULTS AFTER FORMING IN THE PSEUDOCROSSBAR
ARRAY

Current level ([A], Transistor channel width = 45 nm)					
$V_g = 0.5$ V			$V_g = 1.0$ V		
R_{seg}	min	max	R_{seg}	min	Max
0.1	$4.630\cdot10^{-5}$	$4.733\cdot10^{-5}$	0.1	$4.876\cdot10^{-5}$	$4.930\cdot10^{-5}$
0.5	$4.319\cdot10^{-5}$	$4.729\cdot10^{-5}$	0.5	$4.576\cdot10^{-5}$	$4.916\cdot10^{-5}$
1	$3.984\cdot10^{-5}$	$4.735\cdot10^{-5}$	1	$4.246\cdot10^{-5}$	$4.915\cdot10^{-5}$
10	$1.533\cdot10^{-5}$	$4.715\cdot10^{-5}$	10	$1.787\cdot10^{-5}$	$4.902\cdot10^{-5}$
50	$1.515\cdot10^{-6}$	$4.647\cdot10^{-5}$	50	$4.625\cdot10^{-6}$	$4.843\cdot10^{-5}$
Vacancy Concentration ([m^{-3}], Transistor channel width = 45 nm)					
$V_g = 0.5$ V			$V_g = 1.0$ V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$6.91\cdot10^{26}$	$7.35\cdot10^{26}$	0.1	$8.79\cdot10^{26}$	$1.02\cdot10^{27}$
0.5	$5.99\cdot10^{26}$	$7.35\cdot10^{26}$	0.5	$8.63\cdot10^{26}$	$9.87\cdot10^{26}$
1	$5.10\cdot10^{26}$	$7.35\cdot10^{26}$	1	$8.28\cdot10^{26}$	$9.58\cdot10^{26}$
10	$7.80\cdot10^{25}$	$7.30\cdot10^{26}$	10	$2.42\cdot10^{26}$	$8.77\cdot10^{26}$
50	$5.06\cdot10^{24}$	$7.11\cdot10^{26}$	50	$3.16\cdot10^{25}$	$8.60\cdot10^{26}$

Current level ([A], Transistor channel width = 90 nm)					
$V_g = 0.5$ V			$V_g = 1.0$ V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$9.405\cdot10^{-5}$	$9.773\cdot10^{-5}$	0.1	$9.708\cdot10^{-5}$	$9.986\cdot10^{-5}$
0.5	$8.292\cdot10^{-5}$	$9.773\cdot10^{-5}$	0.5	$8.601\cdot10^{-5}$	$9.984\cdot10^{-5}$
1	$7.190\cdot10^{-5}$	$9.767\cdot10^{-5}$	1	$7.512\cdot10^{-5}$	$9.980\cdot10^{-5}$
10	$1.928\cdot10^{-5}$	$9.709\cdot10^{-5}$	10	$2.197\cdot10^{-5}$	$9.924\cdot10^{-5}$
50	$2.403\cdot10^{-6}$	$9.459\cdot10^{-5}$	50	$4.954\cdot10^{-6}$	$9.684\cdot10^{-5}$
Vacancy Concentration ([m^{-3}], Transistor channel width = 90 nm)					
$V_g = 0.5$ V			$V_g = 1.0$ V		
R_{seg}	min	max	R_{seg}	min	max
0.1	$3.08\cdot10^{27}$	$3.33\cdot10^{27}$	0.1	$4.18\cdot10^{27}$	$5.18\cdot10^{27}$
0.5	$2.32\cdot10^{27}$	$3.33\cdot10^{27}$	0.5	$4.04\cdot10^{27}$	$4.81\cdot10^{27}$
1	$1.70\cdot10^{27}$	$3.33\cdot10^{27}$	1	$3.25\cdot10^{27}$	$4.47\cdot10^{27}$
10	$1.22\cdot10^{26}$	$3.29\cdot10^{27}$	10	$4.46\cdot10^{26}$	$4.17\cdot10^{27}$
50	$7.17\cdot10^{24}$	$3.10\cdot10^{27}$	50	$3.94\cdot10^{25}$	$3.99\cdot10^{27}$

In integrated memory cells, BL and WL may consist of different materials. Moreover, the pitch in lateral and horizontal direction may be different as BL and WL could be integrated in different metal layers of the integrated stack. Thus, in general, different segment resistances for BL and WL are expected. To further study the influence of the line series resistance in the arrays, we performed simulations with an asymmetric line segment resistance for WL and BL. In the simulation, $R_{\mathrm{seg,WL}}$ is fixed to 1 Ω, and $R_{\mathrm{seg,BL}}$ was chosen to 0.1 Ω (i.e., $R_{\mathrm{seg,WL}} > R_{\mathrm{seg,BL}}$) and 50 Ω (i.e., $R_{\mathrm{seg,WL}} < R_{\mathrm{seg,BL}}$). The transistor channel was 45 nm, and $V_g = 0.5$ V was chosen for the simulation condition.

Fig. 7(a) and (b) shows the simulated read current level after forming at each array point in the typical-type array. In Fig. 7(a) with $R_{\mathrm{seg,BL}} = 0.1\Omega$, the influence by the line series resistance for WL should be dominant. The current level after forming is getting higher with the increasing point number of row i, because the series resistance in the typical-type array is identified with $R_{\mathrm{ser}} = (m-i)\cdot R_{\mathrm{WL,seg}} + i\cdot R_{\mathrm{BL,seg}}$. In contrast, in Fig. 7(b) with $R_{\mathrm{seg,BL}} = 50\Omega$, the current level after forming is getting lower with the increasing point number of row i.

Fig. 7(c) and (d) shows the simulated read current level after forming in the vertical-type array. In this case, the series resistance in the vertical-type array is identified with $R_{\mathrm{ser}} = j\cdot R_{\mathrm{WL,seg}} + i\cdot R_{\mathrm{BL,seg}}$. In Fig. 7(c), with $R_{\mathrm{seg,BL}} = 0.1\Omega$, the influence by WL resistance is dominant, and the current level after forming is getting lower with the increasing point number of column j. In contrast, in Fig. 7(d) with

$R_{\mathrm{seg,BL}} = 50\Omega$, the BL line series resistance dominates. The current level after forming is getting lower with the increasing point number of row i.

The simulated read current level after forming in the pseudocrossbar array is shown in Fig. 7(e) and (f). The series resistance in the pseudocrossbar array is similar to the vertical-type array, and the influence of the line series resistance is comparable to the case of the vertical-type array.

VI. DISCUSSION

As the array size is getting larger for neuromorphic application, the impact of the line series resistance on each array cell becomes more severe [30]–[32]. The best way to minimize this impact is that the larger height and wider width of lines are used for array design. This might however not be an acceptable solution due to the scaling issue. Another approach is the control of the final state by the applied gate voltage or implemented transistor channel width.

Each type of array offers it advantages and disadvantages. As the critical path and the initial path are identical for the typical 1T1R array, it provides a better control on the forming state. This can be observed when comparing the scatter in the box plots. Even when the series resistance is clearly influencing the final characteristic, the variation over the array is

smaller than in the other two array types. The smaller variation in the formed state potentially reduces the device-to-device variability across the array during switching [30], [33]. For a pure memory operation, this type of array is certainly a better choice, however, this suffers from the drawback discussed above during the VMM operations. An analog VMM can only be achieved by time coding of the input vector and measuring the charge over time. In this case, a constant read voltage is used, but the transistors are opened/closed for a certain number of cycles corresponding to the analog input value. This will cost more time. If the memory cell, however, shows a nonlinearity in the *I-V* characteristic using this scheme might be anyway better suited for the accuracy of the VMM operation. Otherwise, the currents would not scale linearly anymore with the analog read voltage. Additional issue with using analog voltage inputs is the read disturb. As the switching kinetics are highly nonlinear, the VCM cell will switch at any voltage, but at orders of magnitude different time scale. This means increasing the read voltage may lead to undesirable changes in the stored synaptic weight.

In the present study, we did not consider the inherent variability of the VCM cells [34], as the focus of this study was on the understanding of the interplay between the VCM cell and the array. Device-to-device variability of the VCM cells, however, is an important issue that needs to be considered. There are three ways of including the variability in the compact model. The first approach takes the similar way as in this article from Bengel *et al.* [35]. In this case, the parameters of the model are taken randomly from a truncated Gaussian distribution. Alternatively, one can consider corner cases, meaning the fastest and slowest forming device. As shown in [35], this approach already gives the expected range of switching variability. In another work from Wiefels *et al.* [36], it was shown how to include the read instability in the JART VCM compact model. In principle, the forming model could be extended in the same manner as in these papers. A third approach, including the variability in the model during the forming process, would be to include a noise source as additional term for the change of the state variables or the temperature as shown by Guan *et al.* [37]. The variability issue will be also included in the future version of the JART VCM forming compact model.

VII. Conclusion

In this research, a highly predictable electroforming compact model for the VCM-based memristive device was developed and applied for the study of 1T1R array application for various configuration. The compact model was fitted with the ZrO$_x$-based VCM device parameters, and validated with its experimental measurement data. First, the detailed electroforming phenomena of the model were checked with the simulated electrical characteristics in the 1T1R single node cell.

With the simulation result in 1T1R array configurations, it was confirmed that the line series resistance for each array point takes a critical role to impact the cell characteristics after the electroforming. In case of a node point, which has the shortest path from voltage source to GND, the highest value

of current level and vacancy concentration after the forming is observed. The distribution of the characteristic values scales with the value of line segment resistance. In addition, the impact of line series resistance can be mitigated with the different gate voltage or channel width condition applied on the transistor part of the 1T1R cell. This simulation study gives a guideline for design parameters in various type of the 1T1R array configuration. From the view of the variability of the formed state, our study shows that the typical 1T1R array structure is the best choice as the length of the current paths is always the same, meaning the series resistance due to wire resistance is always identical.

References

[1] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, pp. 2632–2663, Jul. 2009.

[2] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nat. Nanotechnol.*, vol. 3, pp. 429–433, Jun. 2008.

[3] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nat. Nanotechnol.*, vol. 8, pp. 13–24, Jan. 2013.

[4] R. Waser, "Redox-based resistive switching memories," *J. Nanosci. Nanotechnol.*, vol. 12, pp. 7628–7640, Oct. 2012.

[5] I. Valov, "Interfacial interactions and their impact on redox-based resistive switching memories (ReRAMs)," *Semicond. Sci. Technol.*, vol. 32, Aug. 2017, Art. no. 93006.

[6] A. Marchewka, R. Waser, and S. Menzel, "Physical modeling of the electroforming process in resistive-switching devices," in *Proc. Int. Conf. Simul. Semicond. Process. Devices (SISPAD)*, Kamakura, Japan, Sep. 2017, pp. 133–136.

[7] J. G. Lee, J.-H. Myung, A. B. Naden, O. S. Jeon, Y. G. Shul, and J. T. S. Irvine, "Replacement of Ca by Ni in a perovskite titanate to yield a novel perovskite exsolution architecture for oxygen-evolution reactions," *Adv. Energy Mater.*, vol. 10, Mar. 2020, Art. no. 1903693.

[8] A. A. Sharma, M. Noman, M. Abdelmoula, M. Skowronski, and J. A. Bain, "Electronic instabilities leading to electroformation of binary metal oxide-based resistive switches," *Adv. Funct. Mater.*, vol. 24, pp. 5522–5529, Sep. 2014.

[9] D. Lee, J. Lee, M. Jo, J. Park, M. Siddik, and H. Hwang, "Noise-analysis-based model of filamentary switching ReRAM with ZrO$_x$/HfO$_x$ stacks," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 964–966, Jul. 2011.

[10] A. Kindsmüller, A. Meledin, J. Mayer, R. Waser, and D. J. Wouters, "On the role of the metal oxide/reactive electrode interface during the forming procedure of valence change ReRAM devices," *Nanoscale*, vol. 11, no. 39, pp. 18201–18208, 2019.

[11] M. Sowinska *et al.*, "Hard x-ray photoelectron spectroscopy study of the electroforming in Ti/HfO$_2$-based resistive switching structures," *Appl. Phys. Lett.*, vol. 100, Jun. 2012, Art. no. 233509.

[12] A. Hardtdegen, C. La Torre, F. Cüppers, S. Menzel, R. Waser, and S. Hoffmann-Eifert, "Improved switching stability and the effect of an internal series resistor in HfO$_2$/TiO$_x$ bilayer ReRAM cells," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3229–3236, Aug. 2018.

[13] C. La Torre, A. F. Zurhelle, T. Breuer, R. Waser, and S. Menzel, "Compact modeling of complementary switching in oxide-based ReRAM devices," *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1268–1275, Mar. 2019.

[14] F. Cüppers *et al.*, "Exploiting the switching dynamics of HfO$_2$-based ReRAM devices for reliable analog memristive behavior," *APL Mater.*, vol. 7, Sep. 2019, Art. no. 91105.

[15] Y. Zhuo *et al.*, "A dynamical compact model of diffusive and drift memristors for neuromorphic computing," *Adv. Electron. Mater.*, to be published.

[16] C. La Torre, A. Kindsmüller, S. Son, R. Waser, V. Rana, and S. Menzel, "A compact model for the electroforming process of memristive devices," in *Proc. 24th IEEE Eur. Conf. Circuit Theory Des. (ECCTD)*, Sofia, Bulgaria, Sep. 2020, pp. 1–4.

[17] P. Yao *et al.*, "Fully hardware-implemented memristor convolutional neural network," *Nature*, vol. 577, pp. 641–646, Jan. 2020.

[18] W. Woods and C. Teuscher, "Approximate vector matrix multiplication implementations for neuromorphic applications using memristive crossbars," in *Proc. IEEE/ACM Int. Symp. Nanoscale Archit. (NANOARCH)*, 2017, pp. 103–108, doi: 10.1109/NANOARCH.2017.8053729.

[19] M. Bocquet *et al.*, "Robust compact model for bipolar oxide-based resistive switching memories," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 674–681, Mar. 2014.

[20] M. Alayan *et al.*, "Switching event detection and self-termination programming circuit for energy efficient ReRAM memory arrays," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 5, pp. 748–752, May 2019.

[21] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: Wiley, 2007.

[22] N. G. Nilsson, "An accurate approximation of the generalized Einstein relation for degenerate semiconductors," *Physica Status Solidi (A)*, vol. 19, pp. K75–K78, Sep. 1973.

[23] J. Fleig, "On the current-voltage characteristics of charge transfer reactions at mixed conducting electrodes on solid electrolytes," *Phys. Chem. Chem. Phys.*, vol. 7, no. 9, pp. 2027–2037, 2005.

[24] M. Dunga *et al.*, *BSIM4.6.1 MOSFET Model User's Manual*, Univ. California, Berkeley, CA, USA, 2007.

[25] J. S. Kauppila *et al.*, "A bias-dependent single-event compact model implemented into BSIM4 and a 90 nm CMOS process design kit," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3152–3157, Dec. 2009.

[26] K. Fleck, C. La Torre, N. Aslam, S. Hoffmann-Eifert, U. Böttger, and S. Menzel, "Uniting gradual and abrupt SET processes in resistive switching oxides," *Phys. Rev. Appl.*, vol. 6, Dec. 2016, Art. no. 64015.

[27] J. P. Strachan, D. B. Strukov, J. Borghetti, J. J. Yang, G. Medeiros-Ribeiro, and R. S. Williams, "The switching location of a bipolar memristor: Chemical, thermal and structural mapping," *Nanotechnology*, vol. 22, May 2011, Art. no. 254015.

[28] S. Kim, K.-H. Kim, and W. Lu, "Crossbar RRAM arrays: Selector device requirements during read operation," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1369–1376, May 2014.

[29] S. Yu, P.-Y. Chen, Y. Cao, L. Xia, Y. Wang, and H. Wu, "Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, 2015, pp. 451–454.

[30] A. Grossi *et al.*, "Relationship among current fluctuations during forming, cell-to-cell variability and reliability in RRAM arrays," in *Proc. IEEE Int. Memory Workshop (IMW)*, 2015, pp. 1–4.

[31] D. R. B. Ly, A. Grossi, C. Fenouillet-Beranger, E. Nowak, D. Querlioz, and E. Vianello, "Role of synaptic variability in resistive memory-based spiking neural networks with unsupervised learning," *J. Phys. D, Appl. Phys.*, vol. 51, Aug. 2018, Art. no. 444002.

[32] E. Perez, O. G. Ossorio, S. Dueñas, H. Castán, H. García, and C. Wenger, "Programming pulse width assessment for reliable and low-energy endurance performance in Al:HfO$_2$-based RRAM arrays," *Electronics*, vol. 9, p. 864, May 2020.

[33] S. Amer, M. S. Hasan, and G. S. Rose, "Analysis and modeling of electroforming in transition metal oxide-based memristors and its impact on crossbar array density," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 19–22, Jan. 2018.

[34] E. Perez, M. K. Mahadevaiah, E. P.-B. Quesada, and C. Wenger, "Variability and energy consumption tradeoffs in multilevel programming of RRAM arrays," *IEEE Trans. Electron Devices*, vol. 68, no. 6, pp. 2693–2698, Jun. 2021.

[35] C. Bengel *et al.*, "Variability-aware modeling of filamentary oxide-based bipolar resistive switching cells using SPICE level compact models," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4618–4630, Dec. 2020.

[36] S. Wiefels, C. Bengel, N. Kopperberg, K. Zhang, R. Waser, and S. Menzel, "HRS instability in oxide-based bipolar resistive switching cells," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4208–4215, Oct. 2020.

[37] X. Guan, S. Yu, and H.-S. P. Wong, "A SPICE compact model of metal oxide resistive switching memory with variations," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1405–1407, Oct. 2012.

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